RICHTEK® **RT5744/RT5746**

2.4MHz 4A/6A Step-Down Converter with I²C Interface

1 General Description

The RT5744 and RT5746 are step-down converters that deliver a digitally programmable output from an input voltage supply of 2.5V to 5.5V. The output voltage is programmed through an I²C interface that can operate up to 3.4MHz.

Using a proprietary architecture with synchronous rectification, the RT5744 and RT5746 are capable of delivering continuous 4A and 6A, maintaining that efficiency at load currents as low as 10mA. The regulator operates at a nominal fixed frequency of 2.4MHz, which reduces the external component counts. Additional output capacitance can be added to improve regulation during load transients without affecting stability.

At moderate and light loads, Pulse Frequency Modulation (PFM) is used to operate in power-saving mode with a typical quiescent current of 45μA at room temperature. Even with such a low quiescent current, the part exhibits excellent transient response during large load swings. At higher loads, the system automatically switches to fixed frequency control, operating at 2.4MHz. In shutdown mode, the supply current is typically 0.1μA, and is excellent in reducing power consumption. The PFM mode can be disabled if the fixed frequency is desired. The RT5744 and RT5746 are available in WL-CSP-14B 1.31x2.02 (BSC) package. The recommended junction temperature range is –40°C to 125°C. See Ordering Information for the key features of each part number.

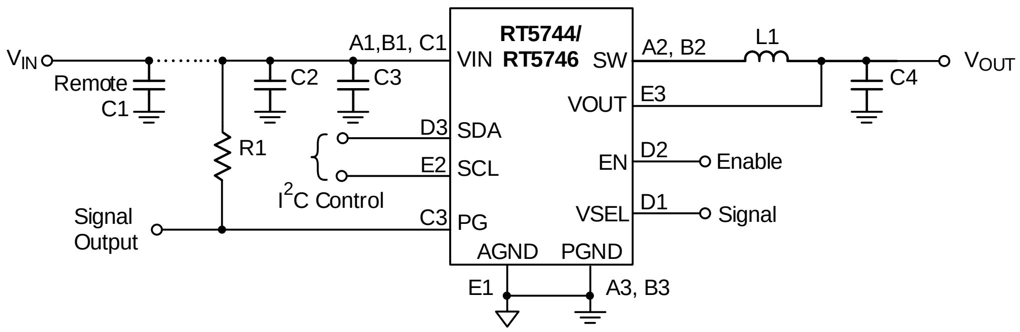
2 Features

- **Programmable Output Voltage Range from 0.27V to 1.4V, 6.25mV/bit**
- **Programmable Slew Rate for Voltage Transitions**
- **Steady 2.4MHz Switching Frequency**
- **Fast Load Transient**
- **Continuous Output Current Capability: 4A/6A**
- **2.5V to 5.5V Input Voltage Range**
- **Digitally Programmable Output Voltage**
- **I²C-Compatible Interface up to 3.4Mbps**
- **PFM Mode for High Efficiency at Light Load**
- **Quiescent Current in PFM Mode: 45μA (Typical)**
- **Input Undervoltage-Lockout (UVLO)**
- **Over-Temperature Protection and Overload Protection**
- **Power-Good Indicator**

3 Applications

- Application, Graphic, and DSP Processors: ARM™, Tegra™, OMAP™, NovaThor™, ARMADA™, Krait™, and more.
- Hard Disk Drives, LPDDR3, LPDDR4, LPDDR5
- Tablets, Netbooks, Ultra-Mobile PCs
- Smart Phones
- Gaming Devices

4 Simplified Application Circuit



5 Ordering Information

Part No.	Defaults Output Voltage		EN Delay Time	Slave Address	Package Type[1]
	VSEL0	VSEL1			
RT5744AP-A	0.8V	0.9V	0ms	0x52	P: WL-CSP-14B 1.31x 2.02 (BSC)
RT5744BP-A	0.8V	0.9V	0ms	0x51	
RT5744CP-A	0.5V	0.6V	0ms	0x51	
RT5744DP-A	0.75V	0.55V	0ms	0x53	
RT5746AP-A	1.05V	0.9V	0ms	0x52	

Note 1.

Richtek products are Richtek Green Policy compliant and marked with [1] indicates compatible with the current requirements of IPC/JEDEC J-STD-020.

6 Marking Information

RT5744AP-A

CD: Product Code
YMDAN: Date Code

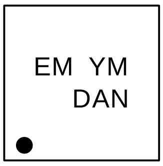
RT5746AP-A

CG: Product Code
YMDAN: Date Code

RT5744BP-A

CF: Product Code
YMDAN: Date Code

RT5744CP-A



EM: Product Code
YMDAN: Date Code

RT5744DP-A

EN: Product Code
YMDAN: Date Code

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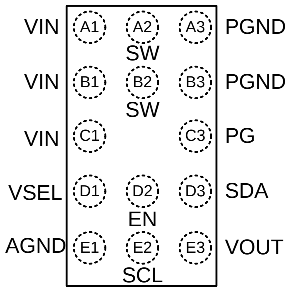
7 Pin Configuration

(TOP VIEW)

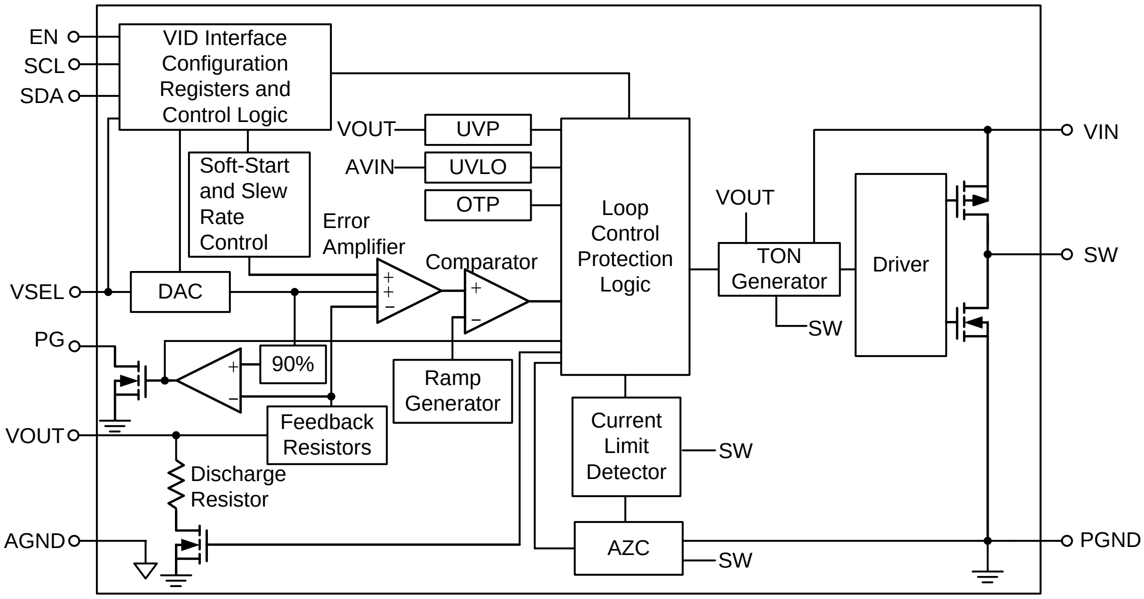


WL-CSP-14B 1.31x 2.02 (BSC)

8 Functional Pin Description

Pin No.	Pin Name	Pin Function
A1, B1, C1	VIN	Power input voltage. Connect to the input power source. Connect to CIN with a minimal path.
A2, B2	SW	Switching node. Connect to the inductor.
A3, B3	PGND	Power ground. The low-side MOSFET is referenced to this pin. The CIN and COUT should be returned with a minimal path to these pins.
C3	PG	Power-good indicator. The output of this pin is an open-drain with an external pull-up resistor. After soft startup, PG is pulled up when the FB voltage is within 90% of the reference voltage (typical). The PG status is low while EN is disabled. Note that when VIN is lower than 2.32V (typical), the PG pin will remain low to indicate that the power is not ready.
D1	VSEL	Output voltage and operation mode selection pin. When this pin is low, VOUT is set by the VSEL0 register. When this pin is high, VOUT is set by the VSEL1 register. Except the output voltage setting, the operation mode can also be configured and selected by the VSEL pin; for example, when 0x02 Bit 1 and Bit 0 are equal to 0, then VSEL0 = Auto PFM/PWM mode, and VSEL1 = Auto PFM/PWM mode. Refer to Functional Register Description for more details.
D2	EN	Enable control input. A logic-high enables the converter. A logic-low forces the device into shutdown mode, and all registers will reset to default values.
D3	SDA	I^2C serial data.
E1	AGND	Analog ground. All signals are referenced to this pin. Avoid routing high dV/dt AC currents through this pin.
E2	SCL	I^2C serial clock.
E3	VOUT	Output feedback sense pin. Output voltage is sensed through this pin. Connect to the output capacitor.

9 Functional Block Diagram



10 Absolute Maximum Ratings

(Note 2)

- Supply Input Voltage, VIN -- 0.3V to 7V
- SW Pin Switch Voltage, SW -- –1V to 7.3V

  < 10ns -- –4V to 8.5V
- VIN Pin to SW PIN -- 0.3V to 7V

  < 10ns -- –4V to 8.5V
- Other I/O Pin Voltages --- –0.3V to 7V
- Lead Temperature (Soldering, 10 sec.) --- 260°C
- Junction Temperature --- 150°C
- Storage Temperature Range -- –65°C to 150°C

Note 2. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

11 ESD Ratings

(Note 3)

- ESD Susceptibility

  HBM (Human Body Model)--- 2Kv

Note 3. Devices are ESD sensitive. Handling precautions are recommended.

12 Recommended Operating Conditions

(Note 4)

- Supply Input Voltage, VIN -- 2.5V to 5.5V
- Junction Temperature Range-- –40°C to 125°C

Note 4. The device is not guaranteed to function outside its operating conditions.

13 Thermal Information

(Note 5 and Note 6)

Thermal Parameter		WL-CSP-14B 1.31x2.02	Unit
θ_{JA}	Junction-to-ambient thermal resistance (JEDEC standard)	42	°C/W
$\theta_{JC(Top)}$	Junction-to-case (top) thermal resistance	0.2	°C/W
$\theta_{JC(Bottom)}$	Junction-to-case (bottom) thermal resistance	9.5	°C/W
$\theta_{JA(EVB)}$	Junction-to-ambient thermal resistance (specific EVB)	49.9	°C/W
$\Psi_{JC(Top)}$	Junction-to-top characterization parameter	1.1	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	27.7	°C/W

Note 5. For more information about thermal parameter, see the Application and Definition of Thermal Resistances report, AN061.

Note 6. $\theta_{JA(EVB)}$, $\Psi_{JC(TOP)}$, and Ψ_{JB} are simulated on a high effective-thermal-conductivity four-layer test board which is in size of 70mm x 50mm; furthermore, all layers with 1 oz. Cu. Thermal resistance/parameter values may vary depending on the PCB material, layout, and test environmental conditions.

14 Electrical Characteristics

(V_{IN} = 3.6V, T_A = 25°C, unless otherwise specified.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Operating Quiescent Current PWM	I_{Q_PWM}	I_{LOAD} = 0, mode Bit = 1 (Forced PWM) (Note 7)	--	15	--	mA
Operating Quiescent Current PFM	I_{Q_PFM}	I_{LOAD} = 0A	--	45	--	μA
Operating Low Power Mode Quiescent Current PFM	$I_{Q\_PFM\_LPM}$	I_{LOAD} = 0A and Enable LPM (Note 7)	--	36	--	μA
H/W Shutdown Supply Current	$I_{SHDN\_H/W}$	EN = GND	--	0.1	3	μA
S/W Shutdown Supply Current	$I_{SHDN\_S/W}$	EN = V_{IN}, BUCK_ENx = 0, 2.5V ≤ V_{IN} ≤ 5.5V	--	2	12	μA
Undervoltage-Lockout Threshold	V_{UVLO}	VIN rising	--	2.32	2.45	V
Undervoltage-Lockout Hysteresis	V_{UVLO_HYS}		--	350	--	mV
On-Resistance of High-Side MOSFET	R_{DSON_H}	V_{IN} = 5V	--	30	--	mΩ
On-Resistance of Low-Side MOSFET	R_{DSON_L}	V_{IN} = 5V	--	17	--	mΩ
Input Voltage Logic-High	V_{IH}	2.5V ≤ V_{IN} ≤ 5.5V	1.1	--	--	V
Input Voltage Logic-Low	V_{IL}	2.5V ≤ V_{IN} ≤ 5.5V	--	--	0.4	
EN Input Bias Current	I_{EN}	EN input tied to GND or V_{IN}	--	0.01	1	μA
Output Voltage Accuracy	V_{OUT_ACC}	2.8V ≤ V_{IN} ≤ 4.8V, $I_{OUT(DC)}$ = 0 to 4A, V_{OUT} > 0.6V, Auto PFM/PWM (Note 7)	–2	--	3	%
		2.8V ≤ V_{IN} ≤ 4.8V, $I_{OUT(DC)}$ = 0 to 4A, V_{OUT} ≤ 0.6V, Auto PFM/PWM (Note 7)	–12	--	18	mV
		2.8V ≤ V_{IN} ≤ 4.8V, $I_{OUT(DC)}$ = 0 to 4A, V_{OUT} > 0.6V, Forced PWM (Note 7)	–2	--	2	%
		2.8V ≤ V_{IN} ≤ 4.8V, $I_{OUT(DC)}$ = 0 to 4A, V_{OUT} ≤ 0.6V, Forced PWM (Note 7)	–12	--	12	mV
Load Regulation	V_{LOAD_REG}	$I_{OUT(DC)}$ = 1 to 4A, V_{OUT} > 0.6V, (Note 7)	--	0.1	--	%/A
		$I_{OUT(DC)}$ = 1 to 4A, V_{OUT} ≤ 0.6V, (Note 7)	--	0.2	--	

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Line Regulation	V_{LOAD_REG}	2.5V ≤ V_{IN} ≤ 5.5V, V_{OUT} > 0.4V, $I_{OUT(DC)}$ = 2A (Note 7)	--	0.2	--	%/V
		2.5V ≤ V_{IN} ≤ 5.5V, V_{OUT} ≤ 0.4V, $I_{OUT(DC)}$ = 2A (Note 7)	--	0.3	--	
Load Transient Response	V_{LOAD_TRAN}	I_{LOAD} step 0.01A to 1.5A, t_R = t_F = 500ns, V_{OUT} = 1.125V (Note 7)	--	±45	--	mV
		I_{LOAD} step 0.1A to 1.8A, t_R = t_F = 1μs, V_{IN} = 3.8V, V_{OUT} = 0.9V (Note 7)	--	±56	--	
		I_{LOAD} step 0.01A to 0.8A, t_R = t_F = 1μs, L = 0.33μH, C_{OUT} = 22μF x 2 (Note 7)	--	45	--	
Line Transient Response	V_{LINE_TRAN}	V_{IN} = 3V to 3.6V, t_R = t_F = 10μs, I_{OUT} = 100mA, Forced PWM mode (Note 7)	--	±40	--	mV
High-Side Switch Current Limit	I_{LIM_H}	RT5744	5.5	6	6.5	A
		RT5746	7	7.7	8.5	A
Low-Side Switch Current Limit	I_{LIM_L}	RT5744	4	4.5	5	A
		RT5746	6	6.5	7	A
Over-Temperature Protection Threshold	T_{OTP}		--	150	--	°C
Over-Temperature Protection Threshold Hysteresis	T_{OTP_HYS}		--	15	--	°C
Input Overvoltage Rising Threshold	$V_{IN\_OVP\_R}$	Rising threshold	--	6.15	--	V
Input Overvoltage Falling Threshold	$V_{IN\_OVP\_F}$	Falling threshold	5.5	5.73	--	V
Power-Good Voltage Threshold	V_{PG}		--	90	--	%
Power-Good Voltage Hysteresis	V_{PG_HYS}		--	10	--	%
Switching Frequency	f_{SW}	V_{OUT} = Default RT5744A: 0.8V RT5744B: 0.8V RT5744C: 0.5V RT5744D: 0.75V RT5746A: 1.05V (Note 8)	2100	2400	2700	kHz
Minimum Off-Time	t_{OFF_MIN}		--	170	--	ns
DAC Resolution		(Note 7)	--	8	--	bits
DAC Differential Nonlinearity		(Note 7)	--	--	0.5	LSB

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
I^2C Interface (Note 7)						
SCL Clock Rate	f_{SCL}	Standard mode	--	--	100	kHz
		Fast mode	--	--	400	kHz
		Fast mode Plus	--	--	1	MHz
		High speed mode, load 100pF max	--	--	3.4	MHz
(Repeated) Start Hold Time	$t_{HD;STA}$	Standard mode	4	--	--	μs
		Fast mode	0.6	--	--	
		Fast mode Plus	0.26	--	--	
		High speed mode	0.16	--	--	
SCL Clock Low Period	t_{LOW}	Standard mode	4.7	--	--	μs
		Fast mode	1.3	--	--	
		Fast mode Plus	0.5	--	--	
		High speed mode	0.16	--	--	
SCL Clock High Period	t_{HIGH}	Standard mode	4	--	--	μs
		Fast mode	0.6	--	--	
		Fast mode Plus	0.26	--	--	
		High speed mode	0.06	--	--	
(Repeated) Start Setup Time	$t_{SU;STA}$	Standard mode	4.7	--	--	μs
		Fast mode	0.6	--	--	
		Fast mode Plus	0.26	--	--	
		High speed mode	0.16	--	--	
SDA Data Hold Time	$t_{HD;DAT}$	Standard mode	5	--	--	μs
		Fast mode	0	--	--	
		Fast mode Plus	0	--	--	
		High speed mode	0.01	--	--	
SDA Setup Time	$t_{SU;DAT}$	Standard mode	250	--	--	ns
		Fast mode	100	--	--	
		Fast mode Plus	50	--	--	
		High speed mode	30	--	--	
STOP Condition Setup Time	$t_{SU;STO}$	Standard mode	4	--	--	μs
		Fast mode	0.6	--	--	
		Fast mode Plus	0.26	--	--	
		High speed mode	0.16	--	--	
Bus Free Time between Stop and Start	t_{BUF}	Standard mode	4.7	--	--	μs
		Fast mode	1.3	--	--	
		Fast mode Plus	0.5	--	--	

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Rise Time of SDA and SCL Signals	t_R	Standard mode	--	--	1000	ns
		Fast mode	20	--	300	
		Fast mode Plus	--	--	120	
		High speed mode (SDA) load 100pF max	10	--	80	
		High speed mode (SCL) load 100pF max	10	--	40	
Fall Time of SDA and SCL Signals	t_F	Standard mode	--	--	300	ns
		Fast mode	20 x (VDD/5.5V)	--	300	
		Fast mode Plus	20 x (VDD/5.5V)	--	120	
		High speed mode (SDA) load 100pF max	10	--	80	
		High speed mode (SCL) load 100pF max	10	--	40	
SDA Output Low Sink Current	I_{OL_I2C}	SDA voltage = 0.4V	2	--	--	mA

Note 7. Guaranteed by design.

Note 8. Measured switching frequency may not meet the declared range due to different operation modes and output voltages. For operating in PSM, the f_{SW} varies according to the operating condition. For V_{OUT} < 0.5V, the f_{SW} may be reduced if the duty cycle is too small.

15 Typical Application Circuit

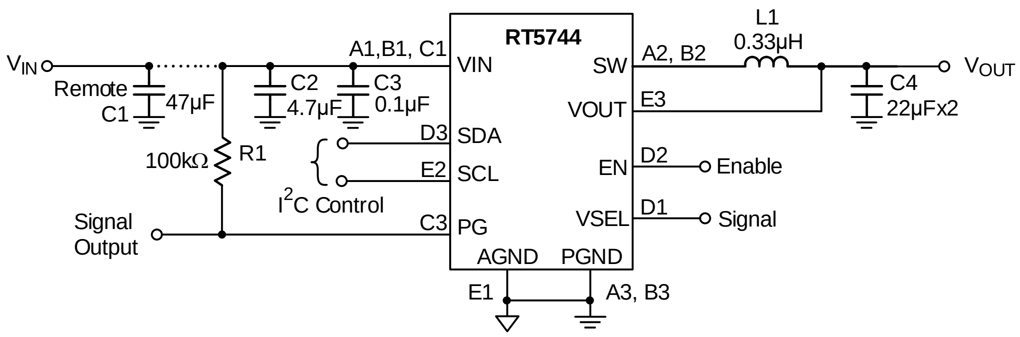


Figure 1. Typical Application Circuit for the RT5744

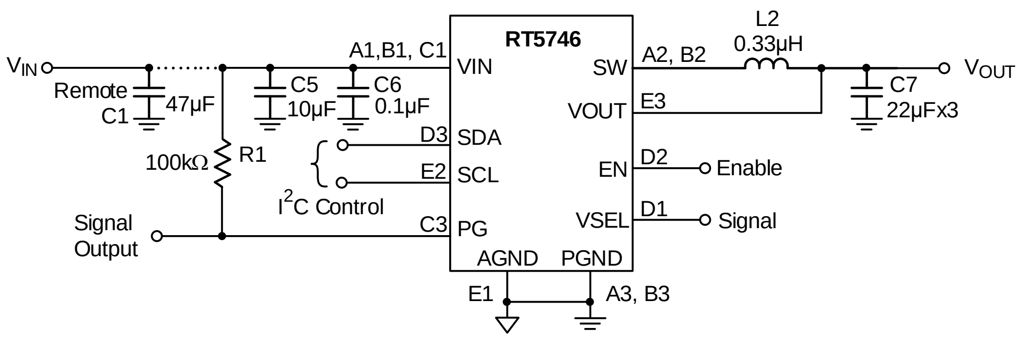


Figure 2. Typical Application Circuit for the RT5746

Table 1. Recommended External Components for 4A/6A Maximum Load Current

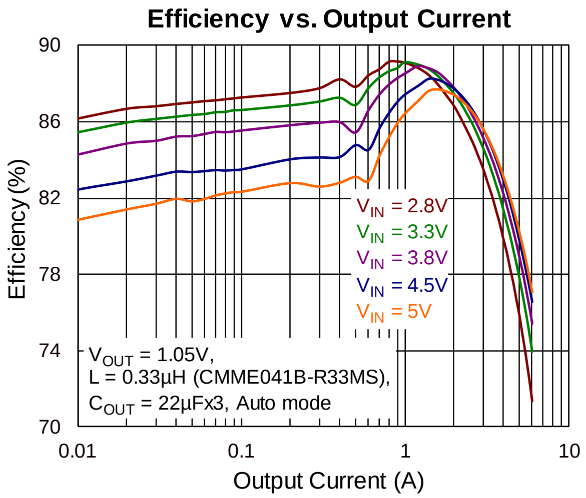
Component	Description	Vendor P/N
L1	330nH (I_{DC} = 4.8A, I_{SAT} = 6.3A, 15mΩ)	DFE201612E-R33M=P2 (Murata)
	470nH (I_{DC} = 4.9A, I_{SAT} = 6.7A, 17mΩ)	DFE252012F-R47M=P2 (Murata)
C2	4.7μF, 10V, X5R, 0402	GRM155R61A475MEAA (Murata)
C3 (Note 9)	100nF, 6.3V, X5R, 0201	GRM033R60J104KE19D (Murata)
C4	22μF x 2, 6.3V, X5R, 0603	GRM188R60J226MEA0D (Murata)
		C1608X5R0J226M080AC (TDK)
L2 (Note 11)	330nH (I_{DC}=12A, I_{SAT}=13.5A, 10.8mΩ)	CMME041B-R33MS (Cyntec)
	220nH (I_{DC}=13A, I_{SAT}=15.5A, 7.2mΩ)	CMME041B-R22MS (Cyntec)
C5	22μF, 6.3V, X5R, 0603	GRM188R60J226MEA0D (Murata)
C6 (Note 9)	100nF, 6.3V, X5R, 0201	GRM033R60J104KE19D (Murata)
C7 (Note 11)	22μF x 3, 6.3V, X5R, 0603	GRM188R60J226MEA0D (Murata)
		C1608X5R0J226M080AC (TDK)
	47μF x 3, 6.3V, X5R, 0603	GRM188R60J476ME01 (Murata)

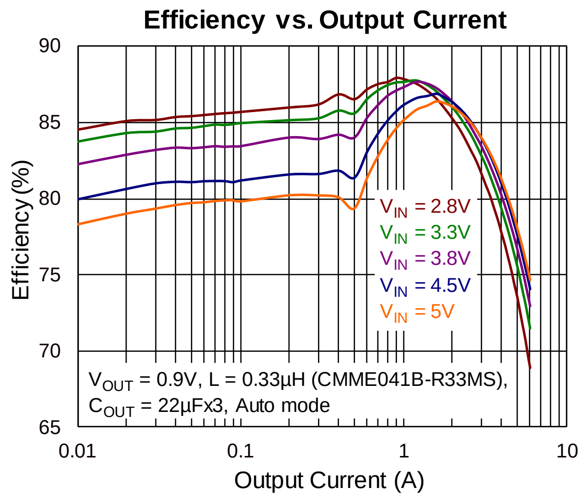
Note 9. The decouple capacitors C3 and C6 are recommended to reduce any high-frequency component on VIN bus. C3 and C6 are optional and used to filter any high frequency components on the VIN bus.

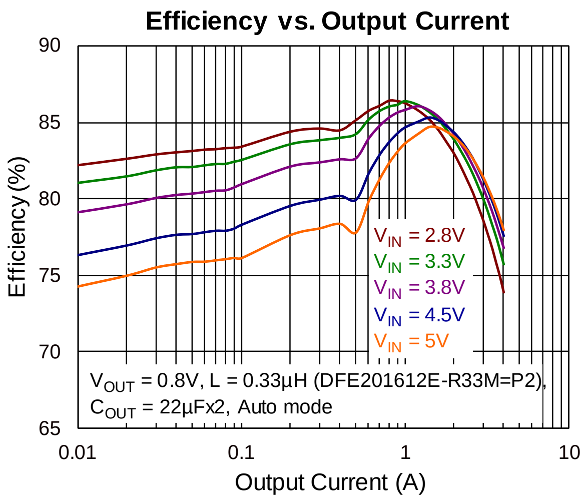
Note 10. All the input and output capacitors are the suggested values, referring to the effective capacitances, subject to any de-rating effects, like a DC bias.

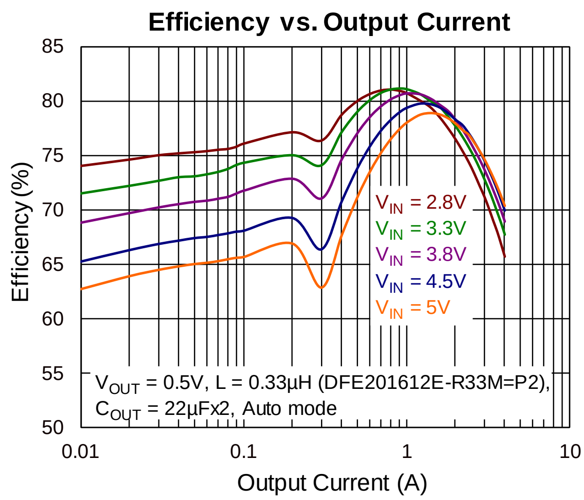
Note 11. For general purpose applications, L2 = 330nH and C7 = 22μF x 3pcs are recommended. For fast load transient requirements, it is recommended to use L2 = 220nH and C7 = 47μF x 3pcs.

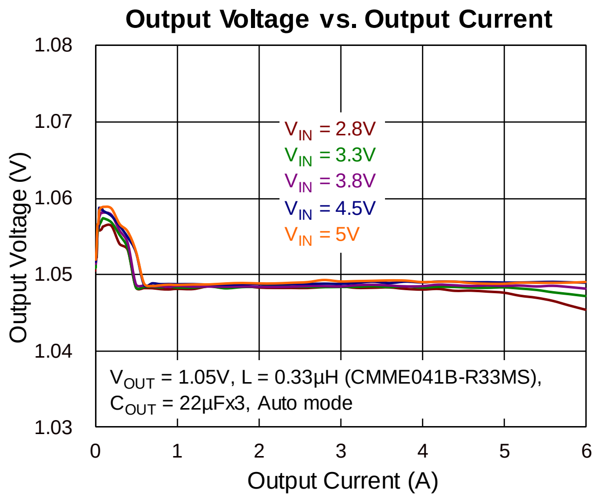
16 Typical Operating Characteristics

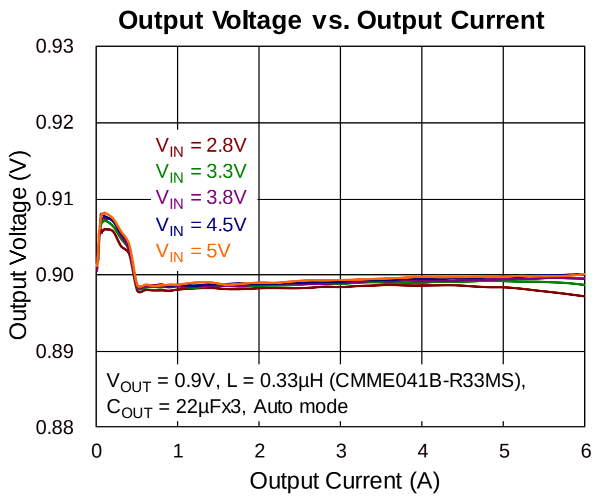




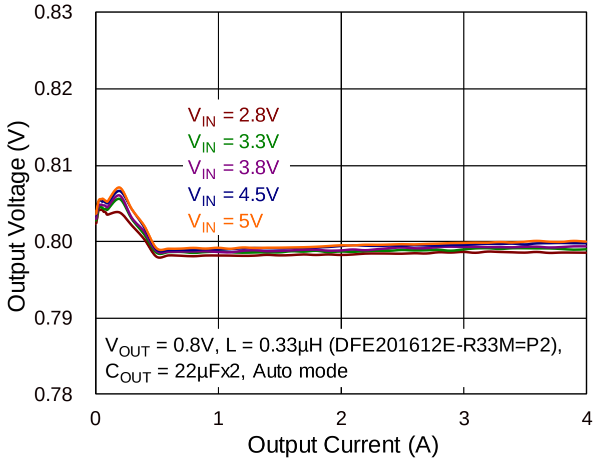








Output Voltage vs. Output Current



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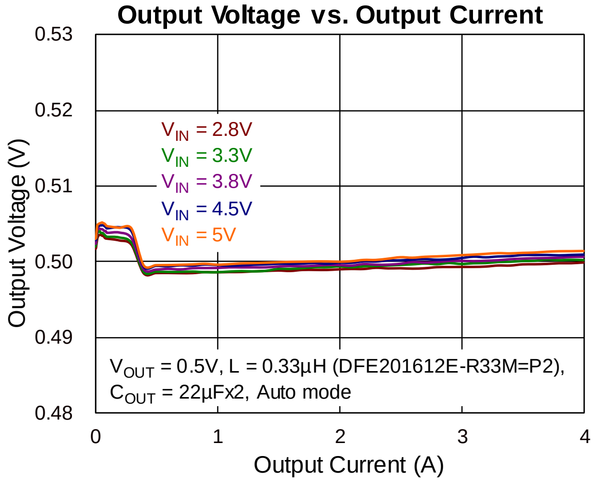
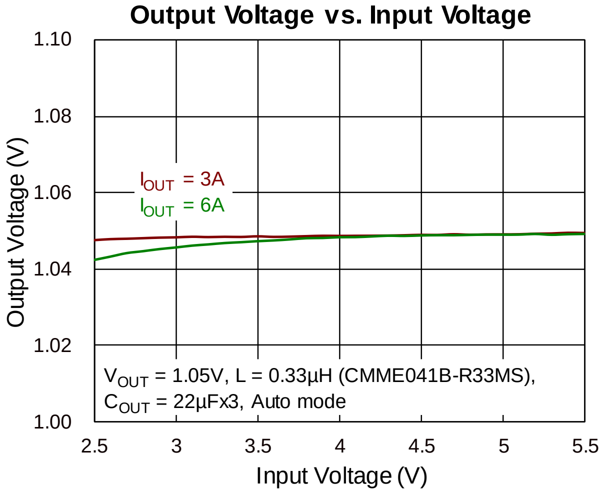
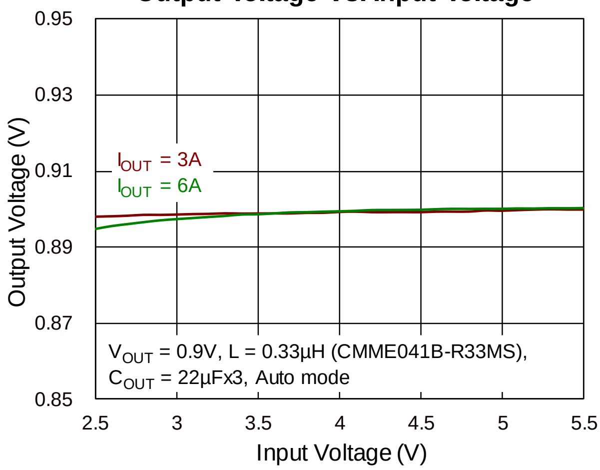


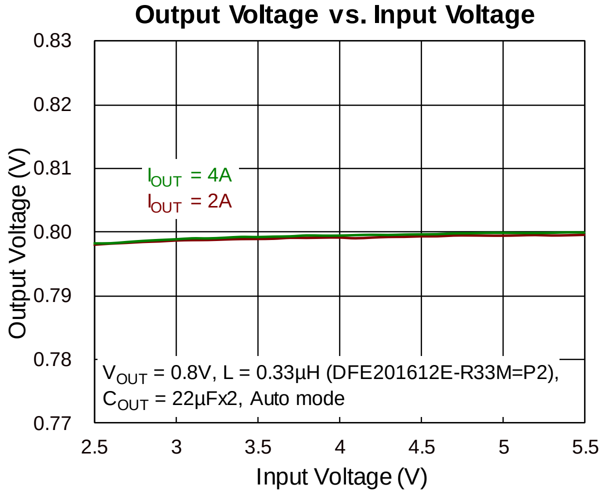
Output Voltage vs. Input Voltage



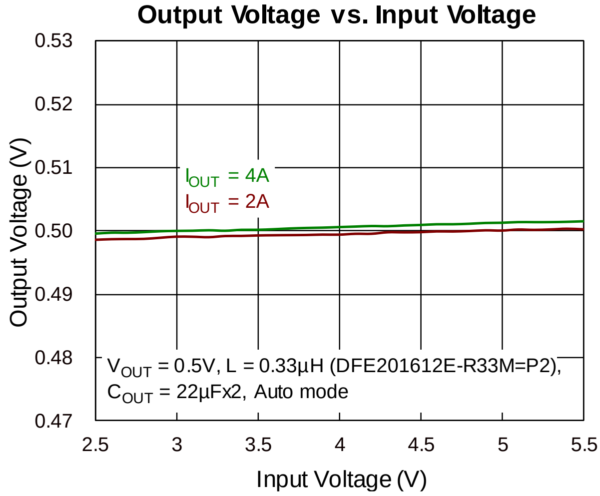
Output Voltage vs. Input Voltage



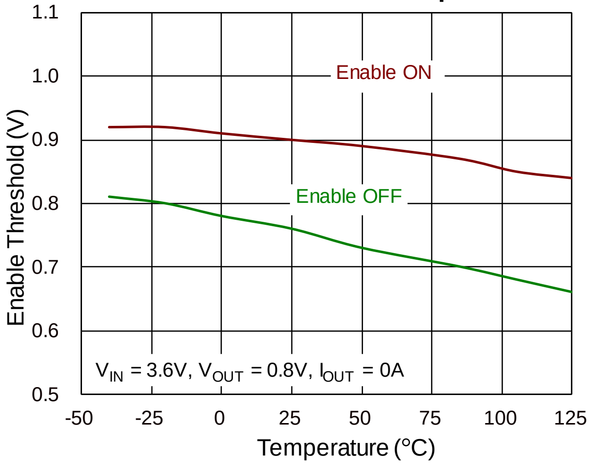
Output Voltage vs. Input Voltage



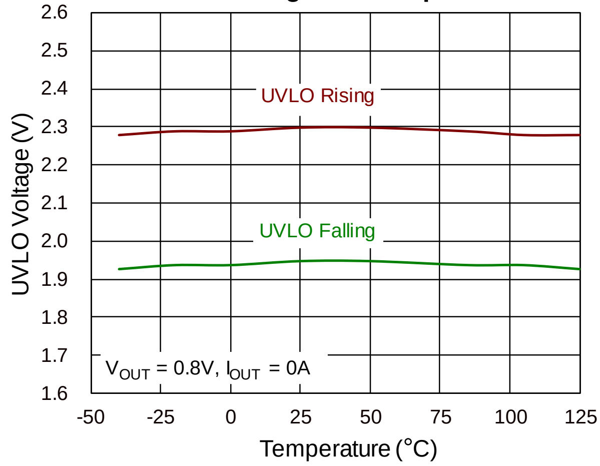
Output Voltage vs. Input Voltage



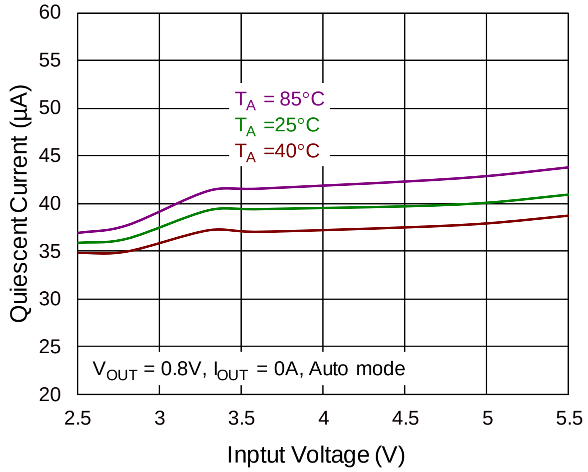
Enable Threshold vs. Temperature



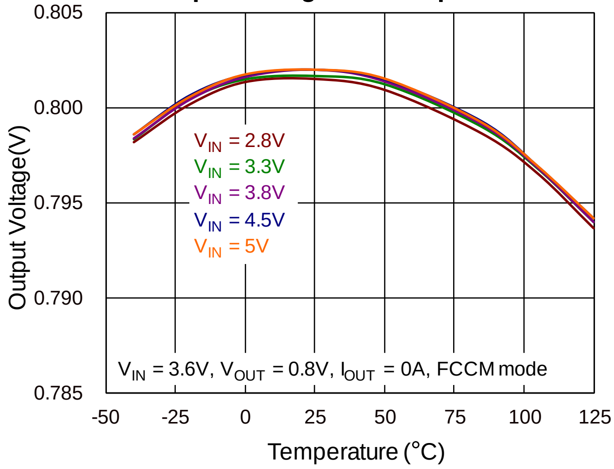
UVLO Voltage vs. Temperature



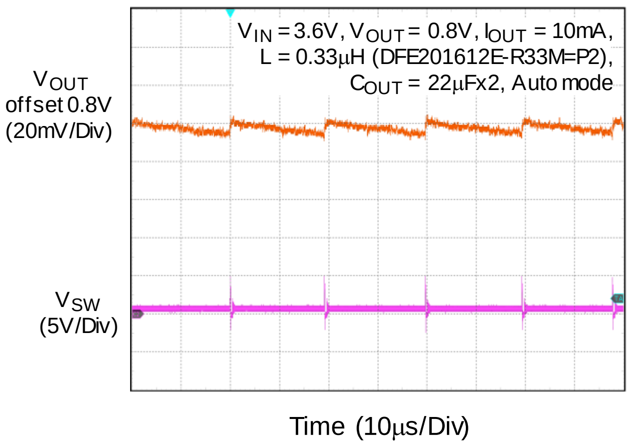
Quiescent CurrentInput vs. Input Voltage



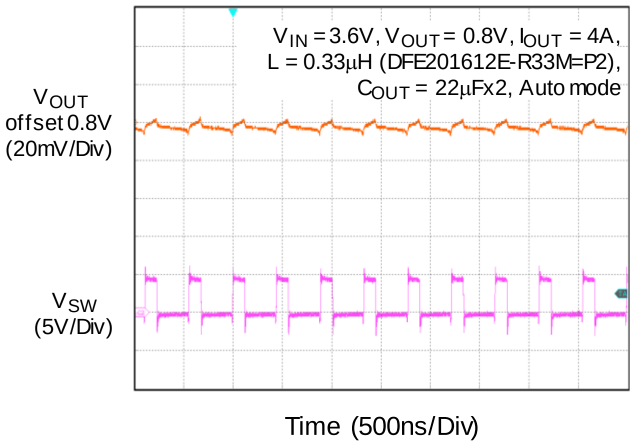
Output Voltage vs. Temperature



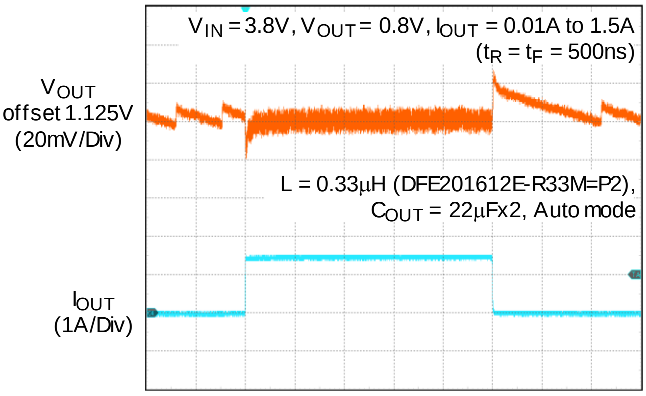
Output Ripple Voltage



Output Ripple Voltage

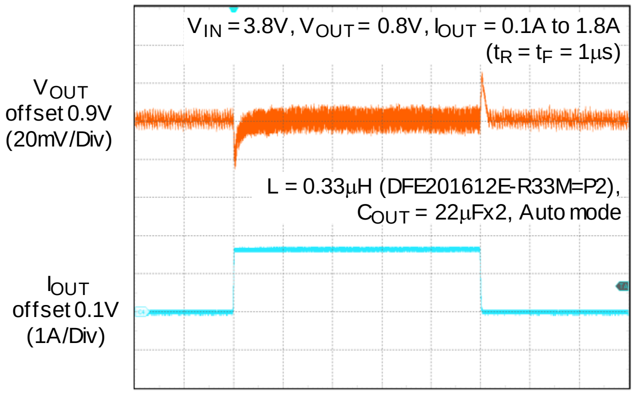


Load Transient Response



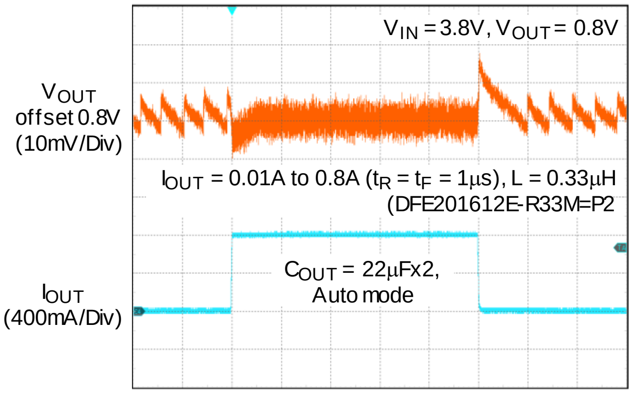
Time (40μs/Div)

Load Transient Response



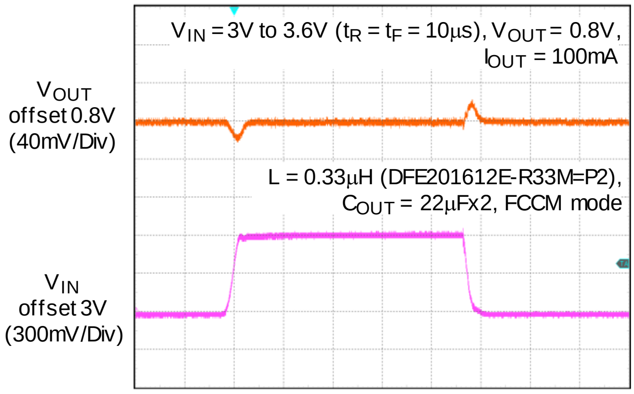
Time (40μs/Div)

Load Transient Response



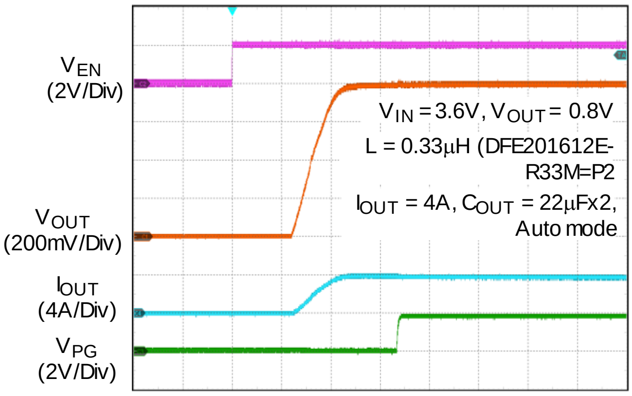
Time (40μs/Div)

Line Transient Response



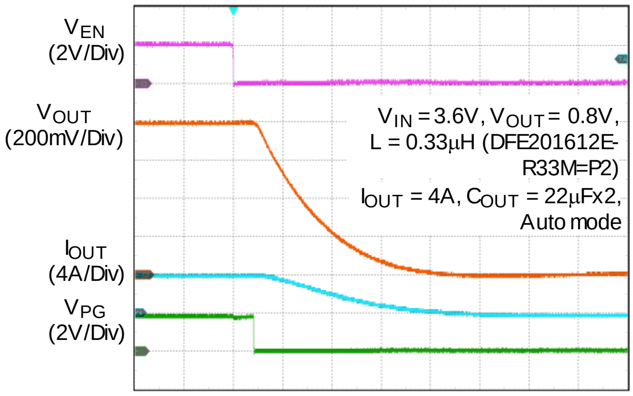
Time (50μs/Div)

Power On from EN



Time (100μs/Div)

Power Off from EN



Time (5μs/Div)

17 Operation

The RT5744 and RT5746 are low-voltage synchronous step-down converters that can support input voltage ranging from 2.5V to 5.5V, and the output current can be up to 4A and 6A, respectively. The RT5744 and RT5746 use ACOT® mode control. To achieve good stability with low-ESR ceramic capacitors, the ACOT® uses a virtual inductor current ramp generated inside the IC. This internal ramp signal replaces the ESR ramp normally provided by the output capacitor's ESR. The ramp signal and other internal compensations are optimized for low-ESR ceramic output capacitors.

17.1 PWM Frequency and Adaptive On-Time Control

In steady-state operation, the feedback voltage (sensed from VOUT), with the virtual inductor current ramp added, is compared to the reference voltage (set by VSEL). When the combined signal is less than the reference voltage, the on-time one-shot is triggered, provided that the minimum off-time one-shot is cleared and the measured inductor current (through the synchronous rectifier) is below the current limit. The on-time one-shot turns on the high-side switch and the inductor current ramps up linearly. After the on-time period, the high-side switch is turned off, the synchronous rectifier is turned on, and the inductor current ramps down linearly. At the same time, the minimum off-time one-shot is triggered to prevent another immediate on-time during the noisy switching times and to allow the feedback voltage and current sense signals to settle. The minimum off-time is kept short so that rapidly-repeated on-times can raise the inductor current quickly when needed.

The on-time can be roughly estimated using the equation:

$$t_{ON} = \frac{V_{OUT}}{V_{IN}} \times \frac{1}{f_{SW}}$$

where f_{SW} is nominal 2.4MHz.

17.2 Undervoltage Lockout (UVLO)

The UVLO continuously monitors the voltage of VIN to make sure the device works properly. When the VIN is high enough to reach the high threshold voltage V_{UVLO} (typically 2.32V), the step-down converter softly starts or pre-biases to its regulated output voltage. When the VIN decreases to its low threshold $V_{UVLO} - V_{UVLO\_HYS}$ (350mV hysteresis), the device will shut down.

17.3 Enable and Soft-Start

When the EN pin is Low, the IC is shut down, all internal circuits are off, and the part draws very little current. In this state, I^2C cannot be written or read until the V_{IN} is above the V_{UVLO} and the V_{EN} is above the V_{IH} (1.1V). The registers will reset when the EN pin is Low or during a Power-On Reset (POR).

An internal current source charges an internal capacitor to build the soft-start ramp voltage. The typical soft-start time can be programmed by I^2C. When V_{IN} is above V_{UVLO} and the device is powered on through the EN pin (the EN delay time setting is 0ms), the output voltage will start to rise within 150μs (typical) as soon as the V_{EN} is above the V_{IH}. See Enable and Shutdown Control for more details.

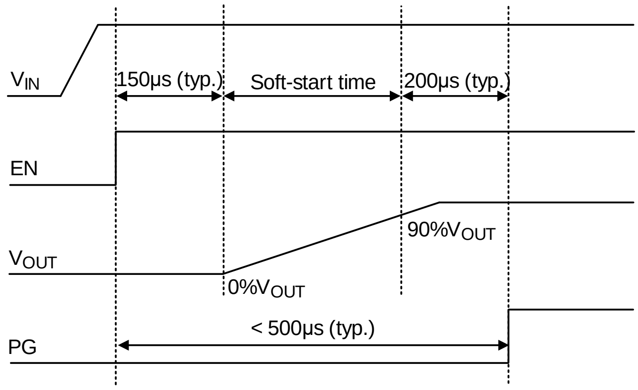


Figure 3. Start-Up Sequence without EN Delay

17.4 Power-Good Indicator

The RT5744 and RT5746 feature an open-drain power-good output (PG) to monitor the output voltage status. The output delay of comparator prevents false flag operation for short excursions in the output voltage, such as during line and load transients. Pull up PG with a resistor to V_{OUT} or an external voltage below 5.5V. When VIN voltage rises above V_{UVLO}, the power-good function is activated. After soft-start is finished, the PG pin is controlled by a comparator connected to the feedback signal V_{OUT}. If V_{OUT} rises above a power-good high threshold (V_{PG}) (typically 90% of the reference voltage), the PG pin will be in high impedance and V_{PG} will be held high. Moreover, when V_{IN} is above UVLO and the device is powered on through the EN pin (EN delay time setting is 0ms), the PG pin will assert high within 500μs (typical) as soon as the V_{EN} is above logic-high threshold.

When V_{OUT} falls below the power-good low threshold (V_{PG} – V_{PG_HYS}) (typically 80% of the reference voltage), the PG pin will be pulled low after a certain delay (3μs, typically). Once being started-up, if any internal protection is triggered, PG will be pulled low to GND. The internal open-drain pull-down device (10Ω, typically) will pull the PG pin low. Note that when Vin is lower than 2.32V (V_{UVLO}), the PG pin will keep low to indicate the power is not ready.

17.5 Output Undervoltage Protection (UVP) and Overcurrent Protection (OCP)

When the output voltage of the RT5744 and RT5746 are lower than 59% of the reference voltage after soft-start, the UVP is triggered.

The RT5744 and RT5746 sense the current signal when high-side and low-side MOSFETs turn on. As a result, the OCP is cycle-by-cycle limit. If the OCP occurs, the converter holds off the next pulse and turns on low-side switch until the inductor drops below the valley current limit, and then turns on high-side again to maintain the output voltage and supports the loading current to the output before triggering UVP.

If the OCP condition keeps and the load current is larger than the current that the converter can provide, the output voltage will decrease and drop below the UVP threshold, and the converter will keep switching for 16 consecutive cycles before it enters hiccup operation. The converter latches off 1.7ms when the output voltage is still lower than the UVP threshold, and the soft-start sequence begins again after the latching off time.

Note that, there is sensing propagation delay time before triggering OCP; hence, the OCP may take a few cycles to occur when the inductor current is near the OCP threshold. If the output voltage drops slowly before entering hiccup operation, the converter will extend the high-side switch on-time and turns on the low-side switch for only minimum off-time to provide large load current and catch up with the output voltage before detecting peak current limit OCP.

17.6 Over-Temperature Protection

The RT5744 and RT5746 have over-temperature protection (OTP) mechanism to prevent overheating due to excessive power dissipation. When the junction temperature exceeds the thermal shutdown threshold T_{OTP} (typically 150°C), the device will be shut down immediately. Once its junction temperature is below the recovery threshold $T_{OTP} - T_{OTP\_HYS}$ (15°C hysteresis), the device will resume normal operation with a complete soft-start.

18 Application Information

(Note 12)

The basic RT5744 and RT5746 application circuit are shown in Typical Application Circuit. The selection of external components is determined by the maximum load current and begins with the selection of the inductor value, operating frequency, and followed by C_{IN} and C_{OUT}.

18.1 Inductor Selection

The inductor value and operating frequency determine the ripple current according to a specific input and output voltage. The ripple current, ΔI_L, increases with a higher V_{IN} and decreases with a higher inductance, as shown in the following equation:

$$\Delta I_L = \left[\frac{V_{OUT}}{f \times L}\right] \times \left[1 - \frac{V_{OUT}}{V_{IN}}\right]$$

where f is the operating frequency and L is the inductance. A lower ripple current reduces not only ESR losses in the output capacitors, but also the output voltage ripple. A higher operating frequency combined with smaller ripple current is necessary to achieve high efficiency. Thus, a large inductor is required to attain this goal.

The largest ripple current occurs at the highest V_{IN}. A reasonable starting point for selecting the ripple current is $\Delta I_L = 0.3 \times I_{MAX}$ to $0.4 \times I_{MAX}$. To guarantee that the ripple current stays below a specified maximum, the inductor value should be chosen according to the following equation:

$$L = \left[\frac{V_{OUT}}{f \times \Delta I_{L(MAX)}}\right] \times \left[1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right]$$

18.2 Input and Output Capacitor Selection

An input capacitor, C_{IN}, is needed to filter out the trapezoidal current at the source of the high-side MOSFET.

To prevent large ripple current, a low ESR input capacitor sized for the maximum RMS current should be used. The RMS current is given by:

$$I_{RMS} = I_{OUT(MAX)} \times \frac{V_{OUT}}{V_{IN}} \times \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT(MAX)}/2$.

This simple worst-case condition is commonly used for design. Choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet the size or height requirements of the design. Ceramic capacitors have high ripple current, high voltage rating and low ESR, which makes them ideal for switching regulator applications.

However, they can also have a high voltage coefficient and audible piezoelectric effects. The high Q of ceramic capacitors with trace inductance can lead to significant ringing. When a ceramic capacitor is used at the input and the power is supplied by a wall adapter through long wires, a load step at the output can induce ringing at the input, V_{IN}. At best, this ringing can couple to the output and be mistaken as loop instability. At worst, a sudden inrush of current through the long wires can potentially cause a voltage spike at V_{IN} large enough to damage the part. Thus, care must be taken to select a suitable input capacitor.

The selection of C_{OUT} is determined by the required ESR to minimize output voltage ripple. Moreover, the amount of bulk capacitance is also a key for C_{OUT} selection to ensure that the control loop is stable. Loop stability can be checked by viewing the load transient response.

The output voltage ripple, ΔV_{OUT}, is determined by:

$$\Delta V_{OUT} \le \Delta I_L \left[ESR + \frac{1}{8 \times f_{SW} \times C_{OUT}} \right]$$

18.3 Dynamic Voltage Scaling (DVS) Control

The RT5744 and RT5746 all series products have programmable output voltage range from 0.27V to 1.4V with 6.25mV/bit resolution. Note that, the output voltage can be set by the NSELx register bit and the output voltages are given by the following equation and example:

VOUT = 0.27V + NSELx x 6.25mV

For example:

If NSELx = 0111100 (60 decimal), then

VOUT = 0.27 + 60 x 6.25mV

= 0.27 + 0.375 = 0.645V.

The RT5744 and RT5746 also have external VSEL pin to select NSEL1(0x01) or NSEL0(0x00). Pulling VSEL to high is for VSEL1 and pulling VSEL to low is for VSEL0. Upon POR, VSEL0 and VSEL1 are reset to their default voltages.

The RT5744 and RT5746 can also control the DVS speed, regardless of the slew rate of voltage changes within the same NSELx or between VSEL0 and VSEL1. In the CONTROL1 register, the UP_SR bits control the up-speed. In the CONTROL2 register, DN_SR can control the down-speed. The default UP_SR is 12.5mV/μs while the default DN_SR is 3.125mV/μs. Refer to the Functional Register Description for more detailed slew rate settings.

18.4 Enable and Shutdown Control

The RT5744 and RT5746 series can power on or off through I^2C by setting the CONTROL2(0x06) EN_VSELx bit to High activating the part to begin the soft-start cycle. Moreover, the soft-start slew rate is programmable through the register 0x06[3:2]. The SS_SR default is 10mV/μs.

The RT5744 and RT5746 series also implements enable control by the external EN pin with enable and shutdown delay times. Note that the enable delay time is the factory setting, and the default value can be read from the CONTROL3 (0x07). As for the shutdown delay time, it can be either factory programmed or set by software, and the default value can be read from the CONTROL4 (0x08).

In the CONTROL1 (0x02) register, set the DISCHG bit to 1 can make V_{OUT} to discharge by an internal resistor when the converter is shut down through I^2C. If the DISCHG bit is set to 0, V_{OUT} will decrease depending on the load. Note that when the EN pin is set to low, the device will default to turning on the internal 10Ω discharge resistor.

18.5 Operation Mode Selection

The default operation mode of the RT5744 and RT5746 series is auto PFM/PWM mode (MODE_VSEL0 and MODE_VSEL1). In the CONTROL1 register, MODE_VSEL0 and MODE_VSEL1 can decide whether the converter is always at forced PWM mode or enters power saving mode under light load conditions.

In auto PFM/PWM mode, the auto zero current detector circuit senses the SW waveform to adjust the zero current threshold voltage. When the current of low-side MOSFET decreases to the zero current threshold, the low-side MOSFET turns off to prevent negative inductor current. In this way, the zero current threshold can be adjusted for different conditions to get better efficiency.

Note that when output voltage is changing from high to low, the RT5744 and RT5746 will make transition operation to forced PWM mode and the output voltage will decrease quickly.

18.6 Low Power Mode Operation

The RT5744 and RT5746 feature auto PFM/PWM mode to achieve power-saving operation. It generates a single switching pulse to ramp up the inductor current and recharges the output capacitor, followed by a skip pulse or a sleep period to cut down current demand from input source to obtain high efficient under light load conditions. The load current is supported by the output capacitor during this sleep period depending on the load current and the inductor peak current.

To minimize the battery energy consumption, the system requests further quiescent current reduction operation such as shipping mode or suspend operation. The RT5744 and RT5746 feature low power mode (LPM) operation, where several of the internal protection circuits (input OVP, UVP) are shutdown to achieve lowest 36μA operating quiescent current for ultra-light load condition. LPM operation can be enabled by setting LPM control register (0x0A bit 1) to 1 in the CONTROL5 register.

18.7 I^2C Time Out Function

The RT5744 and RT5746 have built-in I^2C time out function to make the RT5744 and RT5746 resume listening state during communication bus error situations.

When the RT5744 and RT5746 detect whether the SCL pin or SDA pin is pulled down for more than 30ms, the RT5744 and RT5746 will reset its I^2C interface. The I^2C time out function can be enabled or disabled by control register (0x0A bit 0). For more detail setting values, please refer to Functional Register Description.

18.8 I^2C Interface

The entire series of the RT5744 and RT5746 utilizes the I^2C interface for configuring various settings such as output voltage, Dynamic Voltage Scaling (DVS) slew rate, mode selection, VSEL function setting, and more. The register map provides details on each function's register and how to utilize these functions effectively.

The entire series of the RT5744 and RT5746 supports the fast mode I^2C interface (bit rate 400kb/s), and each part has its own slave address. The I^2C slave ID for the entire series of RT5744 and RT5746 is preconfigured by the factory and ranges from 0x50 to 0x57. For example, the default I^2C slave address of the RT5744A is 7'b1010010. The write or read bit stream (N ≥ 1) is shown below:

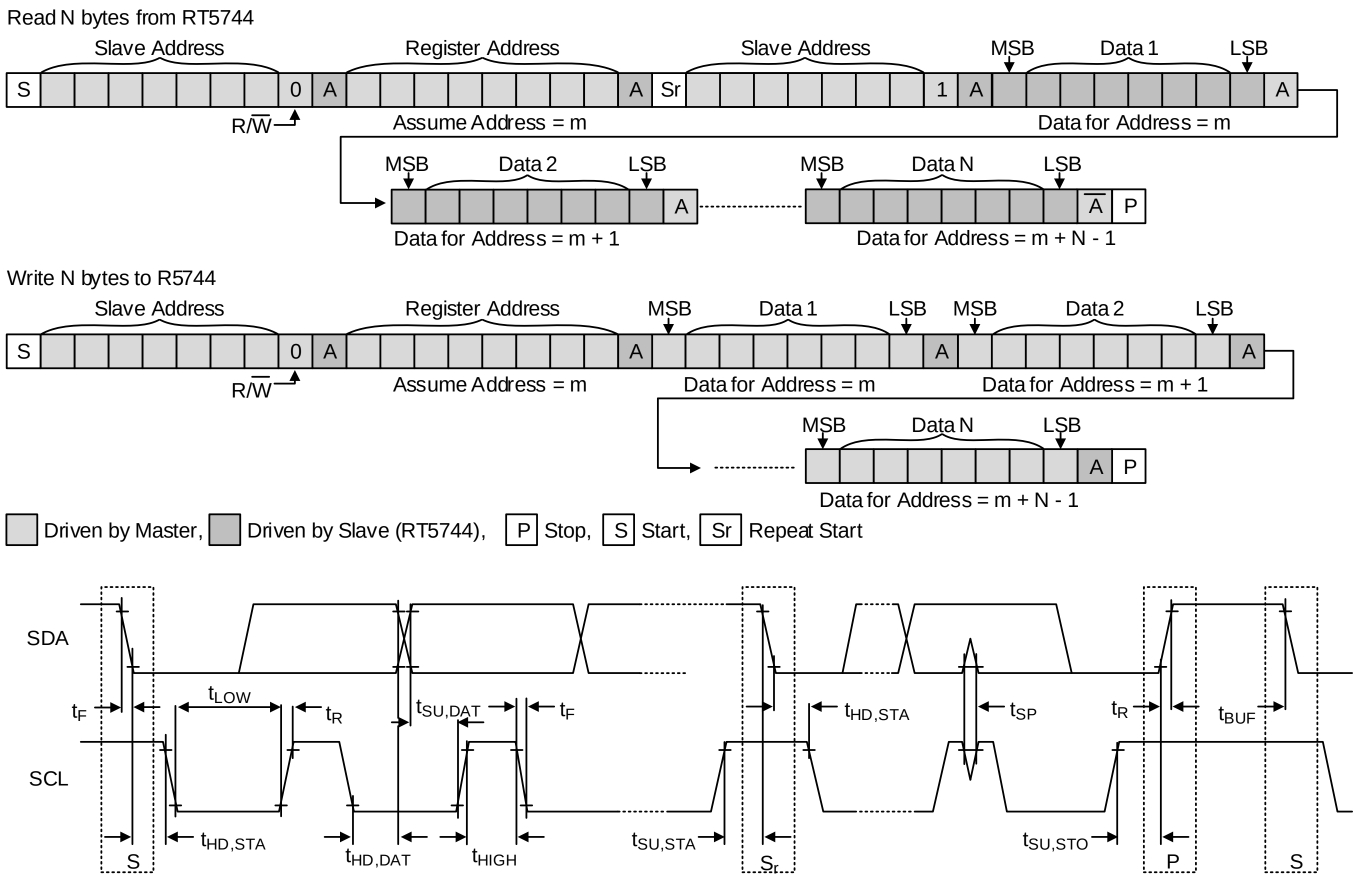


Figure 4. I^2C Read and Write Stream and Timing Diagram

The RT5744 and RT5746 also support high-speed mode (bit rate up to 3.4Mb/s) with access code 08H. Figure 5 and Figure 6 show detailed transfer format. Hs-mode can only commence after the following conditions (all of which are in F/S-mode):

- START condition (S)
- 8-bit master code (00001xxx)
- Not-acknowledge bit ($\overline{A}$)

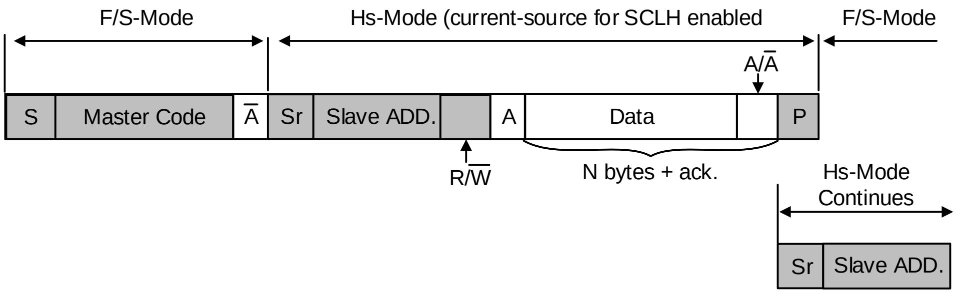


Figure 5. Data Transfer Format in HS-Mode

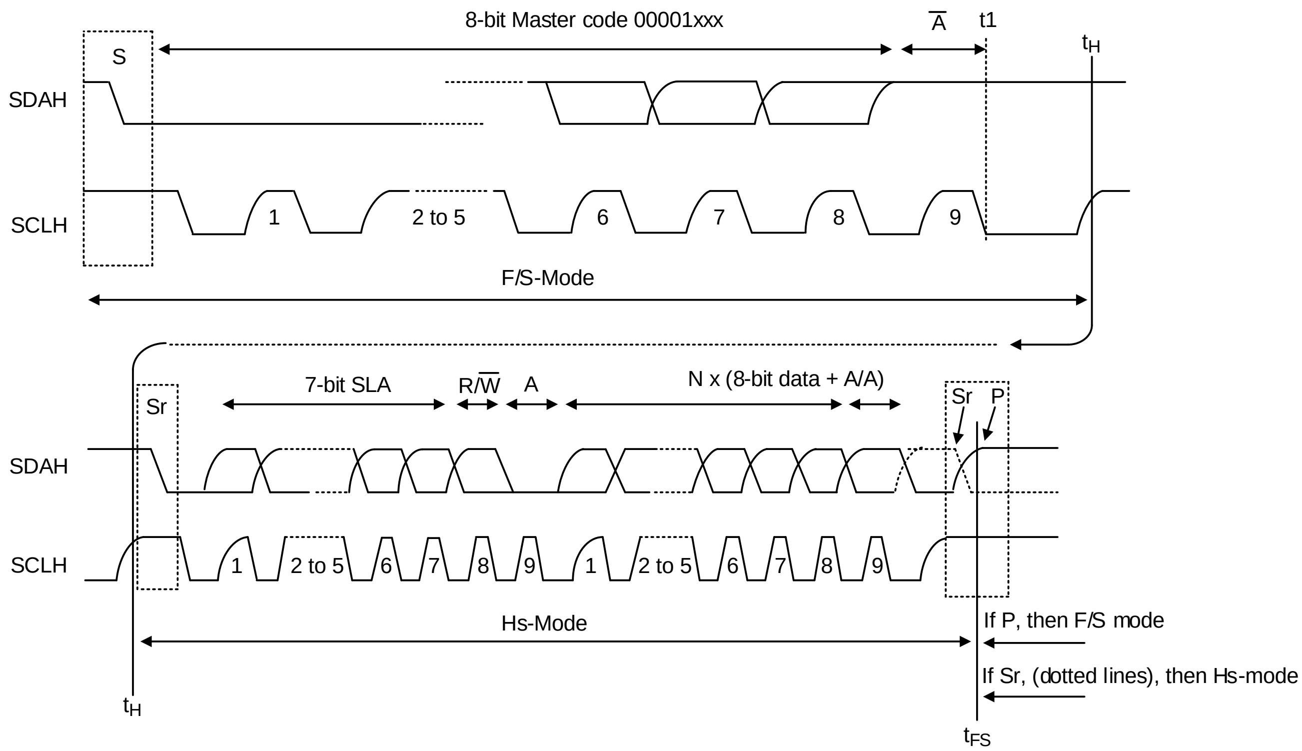


Figure 6. A Complete HS-Mode Transfer

18.9 Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula:

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, $\theta_{JA(EVB)}$, is highly package dependent. The thermal resistance, $\theta_{JA(EVB)}$, is 49.9°C/W on a high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as follows:

$P_{D(MAX)}$ = (125°C - 25°C)/(49.9°C/W) = 2W for a WL-CSP-14B 1.31x2.02 (BSC) package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, $\theta_{JA(EVB)}$. The derating curves in Figure 7 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

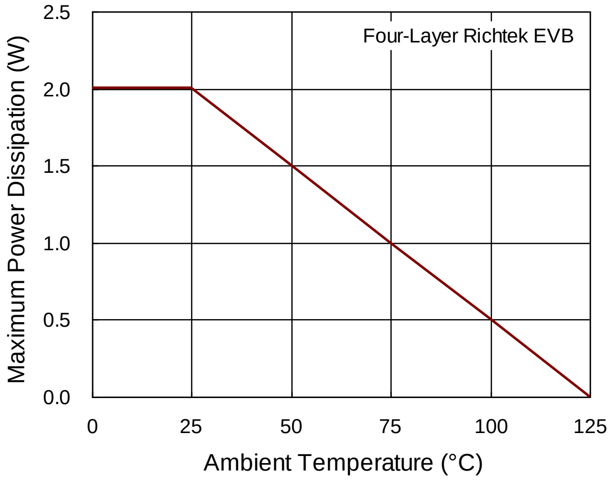


Figure 7. Derating Curve of Maximum Power Dissipation

18.10 Layout Considerations

For best performance of the RT5744 and RT5746, the following layout guidelines must be strictly followed.

- Input capacitor must be placed as close as possible to the IC to minimize the power loop area. A typical 0.1μF decouple capacitor is recommended to reduce power loop area and any high-frequency component on VIN.
- The SW node has high-frequency voltage swings and should be kept at a small area. Keep analog components away from the SW node to prevent stray capacitive noise pickup.
- Keep every power trace connected to pin as wide as possible for improving thermal dissipation.
- It is recommended to connect the AGND pin to the 2nd ground plane through a via from the top layer to the 2nd layer.
- Keep the current protection setting network as close as possible to the IC. The routing of the network should avoid coupling to high-voltage switching node.
- Connections from the drivers to the respective gates of the high-side or the low-side MOSFETs should be as short as possible to reduce stray inductance.

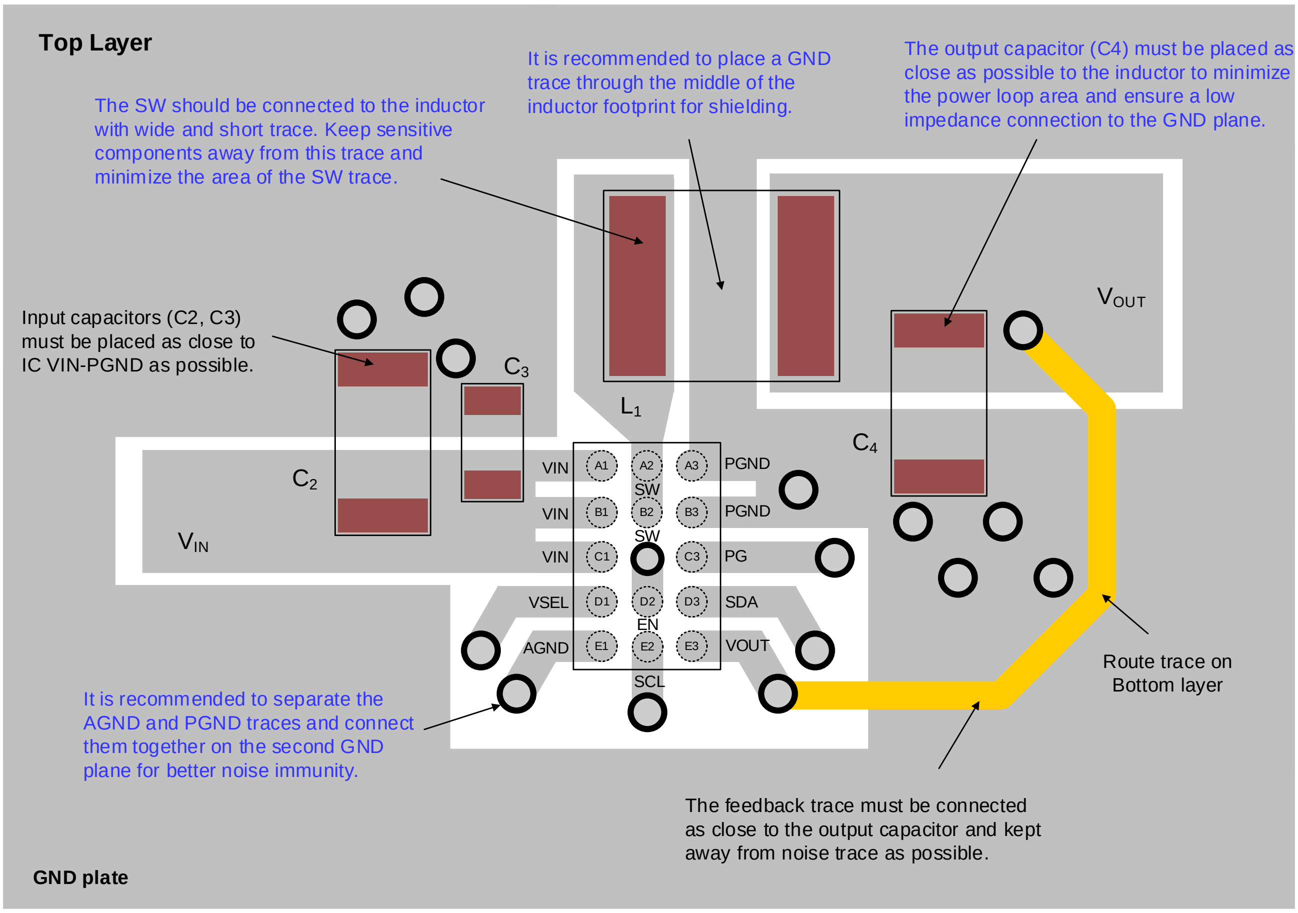
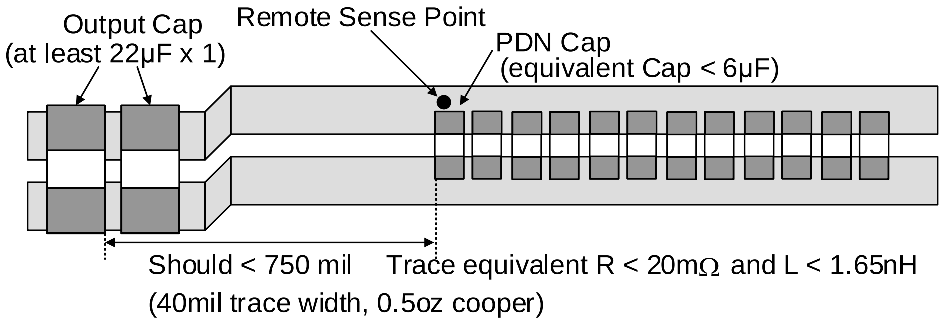
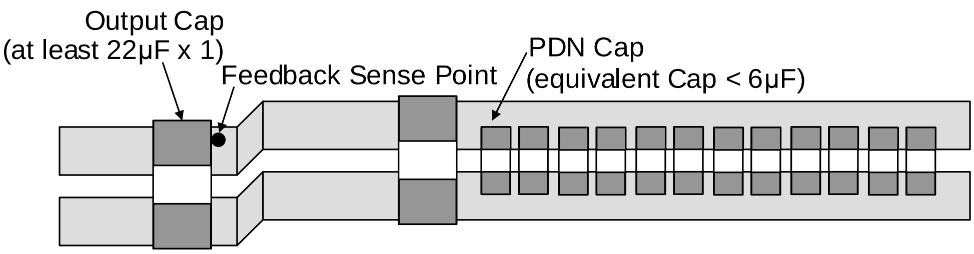


Figure 8. PCB Layout Guide

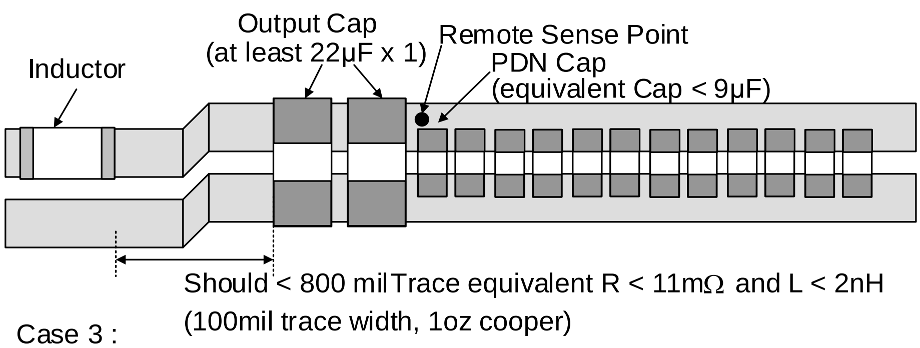
18.11 Layout Constraints for Remote Sense Applications



Case 1 :
If the remote sense point is located at PDN cap
, the distance between 1st 22μF cap and PDN cap should not exceed 750 mil.



Case 2 :
If the remote sense point is located at 1st 22μF cap
, there will be no constraint between 1st 22μF cap and PDN cap yet sacrifice AP transient performance with this configuration.



Case 3 :
If the remote sense point is located at PDN cap and there is long trace between 1st 22μF cap and inductor, the distance should not exceed 800mil.

Figure 9. Layout Constraints

Note 12. The information provided in this section is for reference only. The customer is solely responsible for the designing, validating, and testing your product incorporating Richtek's product and ensure such product meets applicable standards and any safety, security, or other requirements.

19 Functional Register Description

Table 2. VOUT Setting

VOUT (V)	Value	VOUT (V)	Value	VOUT (V)	Value	VOUT (V)	Value	VOUT (V)	Value
0.27	0x00	0.50125	0x25	0.7325	0x4A	0.96375	0x6F	1.195	0x94
0.27625	0x01	0.5075	0x26	0.73875	0x4B	0.97	0x70	1.20125	0x95
0.2825	0x02	0.51375	0x27	0.745	0x4C	0.97625	0x71	1.2075	0x96
0.28875	0x03	0.52	0x28	0.75125	0x4D	0.9825	0x72	1.21375	0x97
0.295	0x04	0.52625	0x29	0.7575	0x4E	0.98875	0x73	1.22	0x98
0.30125	0x05	0.5325	0x2A	0.76375	0x4F	0.995	0x74	1.22625	0x99
0.3075	0x06	0.53875	0x2B	0.77	0x50	1.00125	0x75	1.2325	0x9A
0.31375	0x07	0.545	0x2C	0.77625	0x51	1.0075	0x76	1.23875	0x9B
0.32	0x08	0.55125	0x2D	0.7825	0x52	1.01375	0x77	1.245	0x9C
0.32625	0x09	0.5575	0x2E	0.78875	0x53	1.02	0x78	1.25125	0x9D
0.3325	0x0A	0.56375	0x2F	0.795	0x54	1.02625	0x79	1.2575	0x9E
0.33875	0x0B	0.57	0x30	0.80125	0x55	1.0325	0x7A	1.26375	0x9F
0.345	0x0C	0.57625	0x31	0.8075	0x56	1.03875	0x7B	1.27	0xA0
0.35125	0x0D	0.5825	0x32	0.81375	0x57	1.045	0x7C	1.27625	0xA1
0.3575	0x0E	0.58875	0x33	0.82	0x58	1.05125	0x7D	1.2825	0xA2
0.36375	0x0F	0.595	0x34	0.82625	0x59	1.0575	0x7E	1.28875	0xA3
0.37	0x10	0.60125	0x35	0.8325	0x5A	1.06375	0x7F	1.295	0xA4
0.37625	0x11	0.6075	0x36	0.83875	0x5B	1.07	0x80	1.30125	0xA5
0.3825	0x12	0.61375	0x37	0.845	0x5C	1.07625	0x81	1.3075	0xA6
0.38875	0x13	0.62	0x38	0.85125	0x5D	1.0825	0x82	1.31375	0xA7
0.395	0x14	0.62625	0x39	0.8575	0x5E	1.08875	0x83	1.32	0xA8
0.40125	0x15	0.6325	0x3A	0.86375	0x5F	1.095	0x84	1.32625	0xA9
0.4075	0x16	0.63875	0x3B	0.87	0x60	1.10125	0x85	1.3325	0xAA
0.41375	0x17	0.645	0x3C	0.87625	0x61	1.1075	0x86	1.33875	0xAB
0.42	0x18	0.65125	0x3D	0.8825	0x62	1.11375	0x87	1.345	0xAC
0.42625	0x19	0.6575	0x3E	0.88875	0x63	1.12	0x88	1.35125	0xAD
0.4325	0x1A	0.66375	0x3F	0.895	0x64	1.12625	0x89	1.3575	0xAE
0.43875	0x1B	0.67	0x40	0.90125	0x65	1.1325	0x8A	1.36375	0xAF
0.445	0x1C	0.67625	0x41	0.9075	0x66	1.13875	0x8B	1.37	0xB0
0.45125	0x1D	0.6825	0x42	0.91375	0x67	1.145	0x8C	1.37625	0xB1
0.4575	0x1E	0.68875	0x43	0.92	0x68	1.15125	0x8D	1.3825	0xB2
0.46375	0x1F	0.695	0x44	0.92625	0x69	1.1575	0x8E	1.38875	0xB3
0.47	0x20	0.70125	0x45	0.9325	0x6A	1.16375	0x8F	1.395	0xB4
0.47625	0x21	0.7075	0x46	0.93875	0x6B	1.17	0x90	1.40125	0xB5
0.4825	0x22	0.71375	0x47	0.945	0x6C	1.17625	0x91		
0.48875	0x23	0.72	0x48	0.95125	0x6D	1.1825	0x92		
0.495	0x24	0.72625	0x49	0.9575	0x6E	1.18875	0x93		

Table 3. Register List

Address	Register Name	Default	Type	Note
0x00	NSEL0	0x55	RW	RT5744A/ RT5744B
		0x25		RT5744C
		0x4D		RT5744D
		0x7D		RT5746A
0x01	NSEL1	0x65	RW	RT5744A/ RT5744B
		0x35		RT5744C
		0x2D		RT5744D
		0x65		RT5746A
0x02	CONTROL1	0x90	RW	All devices.
0x03	ID1	0x01	RO	
0x04	ID2	0x00	RO	
0x05	MONITOR	0x00	RO	
0x06	CONTROL2	0x63	RW	
0x07	CONTROL3	0x00	RW	
0x08	CONTROL4	0x00	RW	
0x0A	CONTROL5	0x00	RW	

Table 4. NSEL0

Address: 0x00								
Bit	7	6	5	4	3	2	1	0
Field	VSEL0							
RT5744A	0	1	0	1	0	1	0	1
RT5744B	0	1	0	1	0	1	0	1
RT5744C	0	0	1	0	0	1	0	1
RT5744D	0	1	0	0	1	1	0	1
RT5746A	0	1	1	1	1	1	0	1
Type	RW							

Bit	Name	Description
7:0	VSEL0	VID Table satisfy (activate when the VSEL pin set to logic-low): SEL[7:0] = 10110101: V_{OUT} = 1.40125V … SEL[7:0] = 0000000:V_{OUT} = 0.27V 6.25mV step for 0.27~1.40125

Table 5. NSEL1

Address: 0x01								
Bit	7	6	5	4	3	2	1	0
Field	VSEL1							
RT5744A	0	1	1	0	0	1	0	1
RT5744B	0	1	1	0	0	1	0	1
RT5744C	0	0	1	1	0	1	0	1
RT5744D	0	0	1	0	1	1	0	1
RT5746A	0	1	1	0	0	1	0	1
Type	RW							

Bit	Name	Description
7:0	VSEL1	VID Table satisfy (activate when the VSEL pin set to logic-high): SEL[7:0] = 10110101: V_{OUT} = 1.40125V … SEL[7:0] = 0000000:V_{OUT} = 0.27V 6.25mV step for 0.27~1.40125

Table 6. CONTROL1

Address: 0x02								
Bit	7	6	5	4	3	2	1	0
Field	DISCHG	UP_SR			Reserved	SW_RESET	MODE_VSEL1	MODE_VSEL0
Default	1	0	0	1	0	0	0	0
Type	RW	RW			RV	RW	RW	RW

Bit	Name	Description
7	DISCHG	0: Disable internal output discharge resistor 1: Enable internal output discharge resistor
6:4	UP_SR	DVS Speed for UP DVS 000 = 25mV/μs 001 = 12.5mV/μs 010 = 6.25mV/μs 011 = 3.125mV/μs 100 = 1.5625mV/μs 101 = 0.78125mV/μs 110 = 0.39065mV/μs 111 = 0.1953125mV/μs
3	Reserved	Reserved bits
2	SW_RESET	Write 1 to reset, always read 0
1	MODE_VSEL1	Mode control (activate when the VSEL pin set to logic-high): 1: Forced PWM mode 0: Auto PFM/PWM mode
0	MODE_VSEL0	Mode control (activate when the VSEL pin set to logic-low): 1: Forced PWM mode 0: Auto PFM/PWM mode

Table 7. ID1

Address: 0x03								
Bit	7	6	5	4	3	2	1	0
Field	VENDOR_ID			Reserved	DIE_ID			
Default	0	0	0	0	0	0	0	1
Type	RO			RV	RO			

Bit	Name	Description
7:5	VENDOR_ID	Vendor_ID
4	Reserved	Reserved bits
3:0	DIE_ID	DIE_ID

Table 8. ID2

Address: 0x04								
Bit	7	6	5	4	3	2	1	0
Field	Reserved				DIE_REV			
Default	0	0	0	0	0	0	0	0
Type	RV				RO			

Bit	Name	Description
7:4	Reserved	Reserved bits
3:0	DIE_REV	Revision_ID

Table 9. MONITOR

Address: 0x05								
Bit	7	6	5	4	3	2	1	0
Field	PG	UVLO	OV	POS	NEG	RESET_STAT	OT	BUCK_STATUS
Default	0	0	0	0	0	0	0	0
Type	RO	RO	RO	RO	RO	RO	RO	RO

Bit	Name	Description
7	PG	1: Buck is enabled and soft-start is completed.
6	UVLO	1: Signifies the VIN is less than the UVLO threshold.
5	OV	1: Signifies the VIN is greater than the input OV threshold.
4	POS	1: Signifies a positive voltage transition is in progress
3	NEG	1: Signifies a negative voltage transition is in progress
2	RESET_STAT	1: Indicates that a register reset was performed.
1	OT	1: Signifies the thermal shutdown is active.
0	BUCK_STATUS	1: Buck enabled; 0: buck disabled.

Table 10. CONTROL2

Address: 0x06								
Bit	7	6	5	4	3	2	1	0
Field	DN_SR			Reserved	SS_SR		EN_VSEL1	EN_VSEL0
Default	0	1	1	0	0	0	1	1
Type	RW			RV	RW		RW	RW

Bit	Name	Description
7:5	DN_SR	DVS Speed for DN DVS 000 = 25mV/μs 001 = 12.5mV/μs 010 = 6.25mV/μs 011 = 3.125mV/μs 100 = 1.5625mV/μs 101 = 0.78125mV/μs 110 = 0.39065mV/μs 111 = 0.1953125mV/μs
4	Reserved	Reserved bits
3:2	SS_SR	DVS Speed for soft-start DVS 00 = 10mV/μs 01 = 5mV/μs 10 = 2.5mV/μs 11 = 1.25mV/μs
1	EN_VSEL1	Software power-on/off control register (activate when the VSEL pin set to logic-high): 0: Disable output 1: Enable output
0	EN_VSEL0	Software power-on/off control register (activate when the VSEL pin set to logic-low): 0: Disable output 1: Enable output

Table 11. CONTROL3

Address: 0x07								
Bit	7	6	5	4	3	2	1	0
Field	Reserved		EN_DLY					
Default	0	0	0	0	0	0	0	0
Type	RV		RW					

Bit	Name	Description
7:6	Reserved	Reserved bits
5:0	EN_DLY	Delay applied upon enable (ms) 000000b (0ms) to 111111b (63ms) (steps of 1ms)

Table 12. CONTROL4

Address: 0x08								
Bit	7	6	5	4	3	2	1	0
Field	Reserved		DIS_DLY					
Default	0	0	0	0	0	0	0	0
Type	RV		RW					

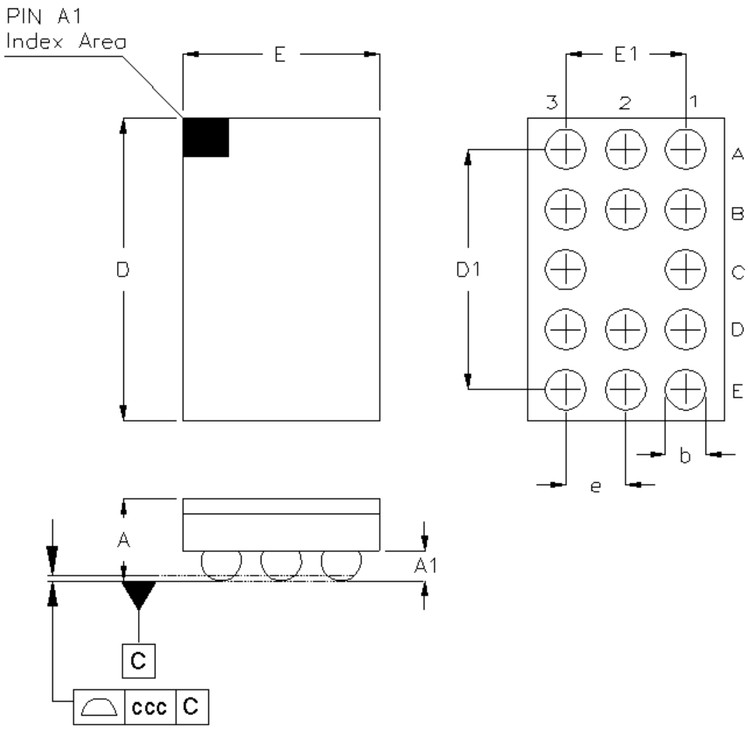
Bit	Name	Description
7:6	Reserved	Reserved bits
5:0	DIS_DLY	Delay applied upon disable (ms) 000000b (0ms) to 111111b (63ms) (steps of 1ms)

Table 13. CONTROL5

Address: 0x0A								
Bit	7	6	5	4	3	2	1	0
Field	Reserved						LPM	I^2C_TIME_OUT
Default	0	0	0	0	0	0	0	0
Type	RV						RW	RW

Bit	Name	Description
7:2	Reserved	Reserved bits
1	LPM	Low power mode (LPM) control register: 0: Disable low power mode function 1: Enable low power mode function for power saving
0	I^2C_TIME_OUT	I^2C time-out control register: 0: Disable I^2C time-out feature 1: Enable I^2C time-out feature to prevent from system hangout situation; the device will automatically reset the I^2C to restore communication.

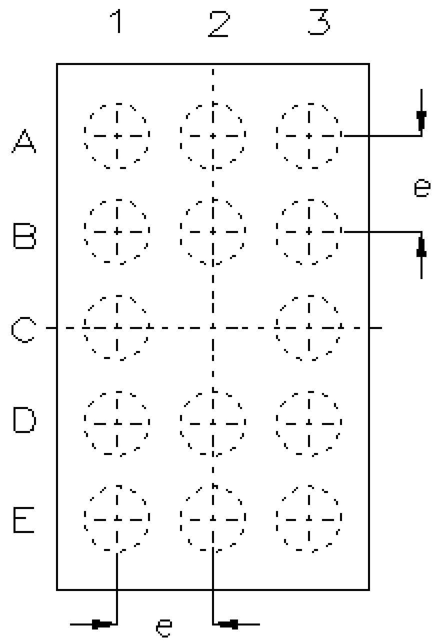
20 Outline Dimension

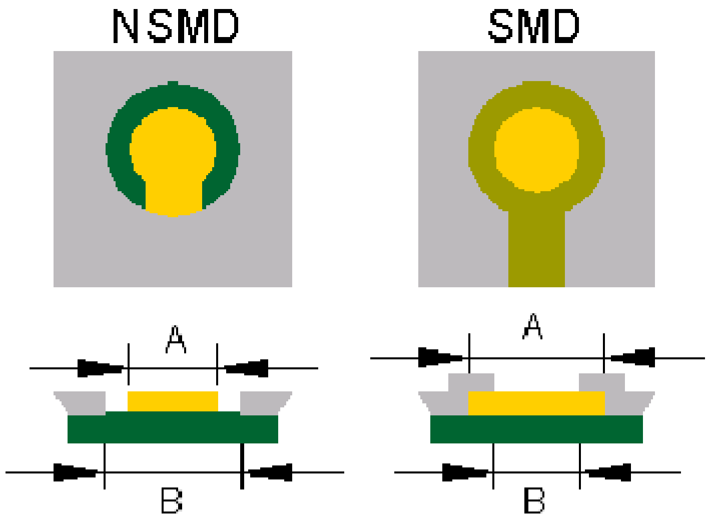


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.500	0.600	0.020	0.024
A1	0.170	0.230	0.007	0.009
b	0.240	0.300	0.009	0.012
D	1.980	2.060	0.078	0.081
D1	1.600		0.063	
E	1.270	1.350	0.050	0.053
E1	0.800		0.031	
e	0.400		0.016	
ccc	0.020		0.001	

14B WL-CSP 1.31x2.02 Package (BSC)

21 Footprint Information

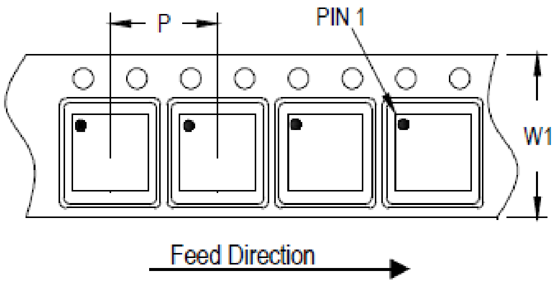


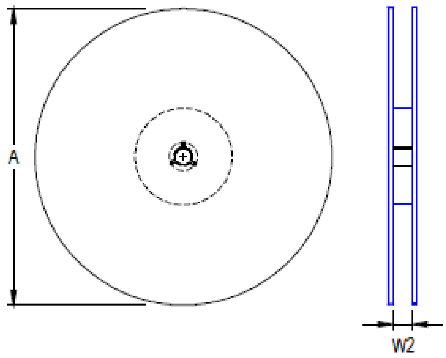


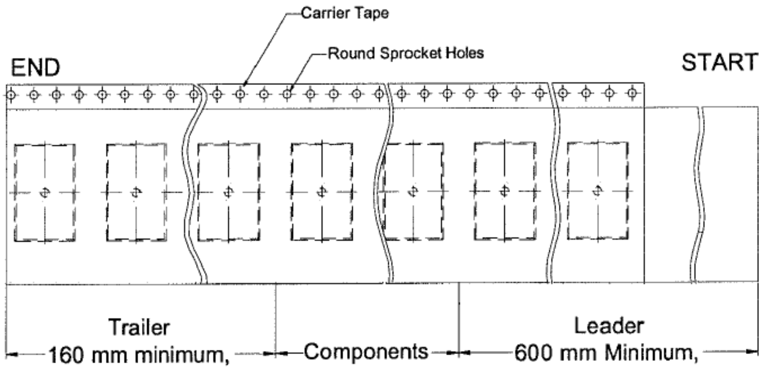
Package	Number of Pins	Type	Footprint Dimension (mm)			Tolerance
			e	A	B	
WL-CSP1.31x2.02-14(BSC)	14	NSMD	0.400	0.240	0.340	±0.025
		SMD		0.270	0.240	

22 Packing Information

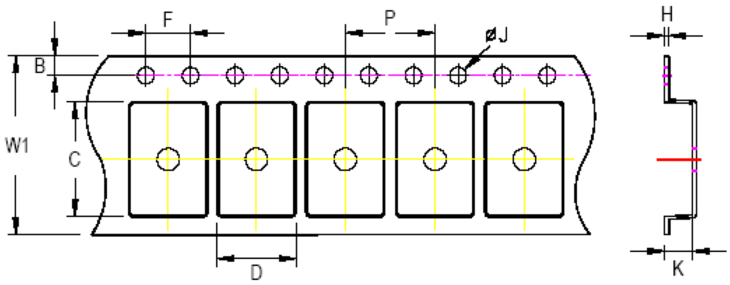
22.1 Tape and Reel Data







Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min/Max (mm)
			(mm)	(in)				
WL-CSP 1.31x2.02	8	4	180	7	3,000	160	600	8.4/9.9



C, D, and K are determined by component size. The clearance between the components and the cavity is as follows:

- For 8mm carrier tape: 0.5mm max.

Tape Size	W1	P		B		F		ØJ		K		H
	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Max
8mm	8.3mm	3.9mm	4.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	0.7mm	0.8mm	0.6mm

22.2 Tape and Reel Packing

Step	Photo/Description	Step	Photo/Description
1	 Reel 7”	**4**	 12 inner boxes per outer box
2	 Packing by Anti-Static Bag	**5**	 Outer box **Carton A**
3	 3 reels per inner box **Box A**	**6**	

Container / Package	Reel		Box			Carton		
	Size	Units	Item	Reels	Units	Item	Boxes	Unit
WL-CSP 1.31x2.02	7”	3,000	Box A	3	9,000	Carton A	12	108,000
			Box E	1	3,000	For Combined or Partial Reel.		

22.3 Packing Material Anti-ESD Property

Surface Resistance	Aluminum Bag	Reel	Cover tape	Carrier tape	Tube	Protection Band
Ω/cm^2	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**

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23 Datasheet Revision History

Version	Date	Description	Item
00	2023/11/22	Final	
01	2024/11/14	Modify	*General Description on page 1* *Features on page 1* *Ordering Information on page 2* *- Added RT5744C and RT5744D* *Marking Information on page 2* *- Added RT5744C and RT5744D* *Electrical Characteristics on page 6, 7, 8, 9* *- Added PG SPEC* *- Modified parameter and symbol* *- Added RT5744C and RT5744D in fsw* *Typical Application Circuit on page 10* *- Modified L1 and L2* *Operation on page 16, 17* *- Added Soft-Start section into Enable and Shutdown* *- Added Power GOOD section into Power-Good Indicator* *- Renamed title Over-Temperature Protection* *Application Information on page 18, 19, 20, 21, 23* *- Modified I^2C Interface Function section* *- Added Slew Rate Setting section into Dynamic Voltage Scaling (DVS) Control* *- Added Discharge Function section into title Enable and Shutdown Control* *- Modified Layout Consideration section* *Functional Register Description on page 26, 27, 28, 29, 30* *- Added RT5744C and RT5744D default value* *- Renamed register bit name PG* *Packing Information on page 37, 38, 39*