RICHTEK®

RT5717

Ultra-Low Quiescent Current RBCOT Buck Converter

1 General Description

The RT5717 is a high efficiency synchronous buck converter with typical 60nA ultra-low quiescent current.

It provides high efficiency at light loads down to 1μA. Its input voltage range is from 1.8V to 5.5V. The RT5717 provides 16 selectable output voltage levels by connecting a resistor between the RSEL pin and GND while delivering output current up to 0.75A/1.2A/1.5A.

The Ripple-Based Constant On-Time (RBCOT) control enhances load and line transient response, optimizing performance over a wide range of loads and output capacitors.

The RT5717 is available in XWL-CSP-6B 0.96x 1.245 (BSC) and WDFN-8JAL 2x1.5 (FC) packages. The recommended junction temperature range is –40°C to 125°C, and the ambient temperature range is –40°C to 85°C.

2 Ordering Information

RT5717□□-□□□

Packing Type
A: Standard

OCP Select
(Refer to Functional Table)

Voltage Output
(Refer to Functional Table)

Package Type(1)
P: XWL-CSP-6B 0.96x1.245 (BSC)
N: WDFN-8JAL 2x1.5 (FC) (W-Type)

Output Function
(For WDFN Package Only)
A: STOP
B: FAULT

Note 1.

Marked with (1) indicated: Richtek products are Richtek Green Policy compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.

3 Features

- **60nA Operating Quiescent Current**
- **25nA Shutdown Current**
- **Input Voltage Range: 1.8V to 5.5V**
- **16 Selectable Output Voltages via RSEL Pin**
- **RBCOT Control for Fast Transient Response**
- **Pulse Frequency Mode (PFM) and Pulse Width Modulation (PWM) Mode Option**
- **Up to 80% Efficiency at 1μA I_{OUT} (V_{IN} = 3.6V/V_{OUT} = 1.8V)**
- **Fault Stage Signal for MCU**
- **Output Voltage Discharge**
- **Undervoltage-Lockout Protection (UVLO)**
- **Overcurrent Protection (OCP)**
- **Over-Temperature Protection (OTP)**
- **Automatic Transition to Bypass Operation with 120nA Quiescent Current**

4 Applications

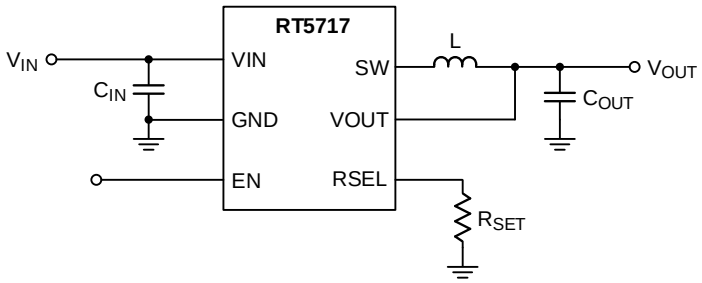
- Hand-Held Devices
- Asset Tracking Devices
- Battery Powered Equipment
- Wearable Devices
- Internet of Things
- Smart Meters, Smart Thermostats

5 Marking Information

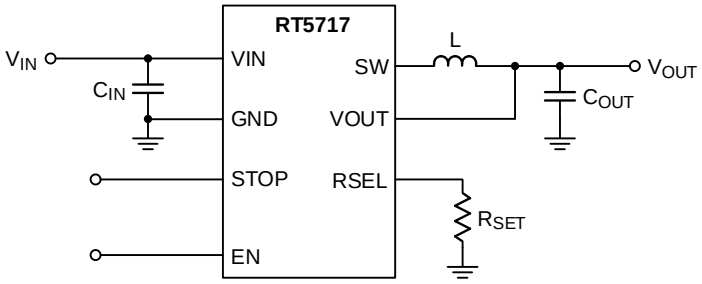
For marking information, contact our sales representative directly or through a Richtek distributor located in your area.

6 Simplified Application Circuit

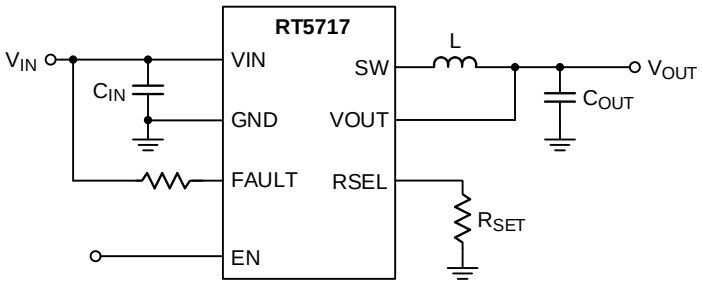
6.1 XWL-CSP-6B 0.96x1.245 (BSC)



6.2 WDFN-8JAL 2x1.5 (FC) Option 1: STOP Function



6.3 WDFN-8JAL 2x1.5 (FC) Option 2: FAULT Function



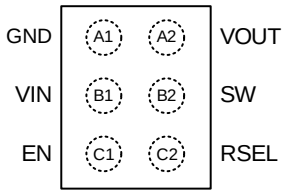
7 Functional Table

Output Voltage Setting Range		OCP Select	
A	Output-1, 0.5V to 4V	A	OCP Select 1 = 1.2A
B	Output-2, 0.8V to 1.55V in 50mV steps	B	OCP Select 2 = 2.04A
C	Output-3, 1.8V to 3.3V in 100mV steps	C	OCP Select 3 = 2.4A
D	Output-4, 1.8V to 3.6V		
F	Output-5, 0.54V to 3.7V		

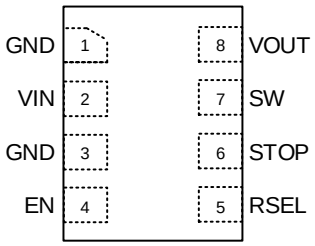
Table of Contents

8 Pin Configuration

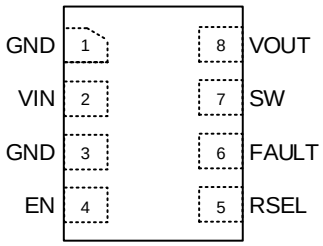
(TOP VIEW)



XWL-CSP-6B 0.96x1.245 (BSC)



WDFN-8JAL 2x1.5 (FC) (Option 1)



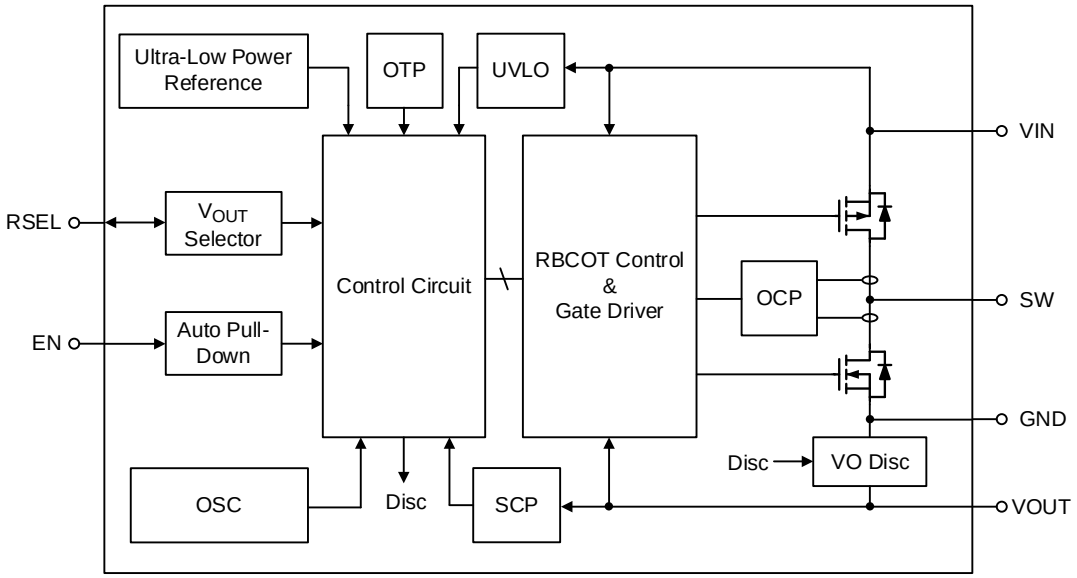
WDFN-8JAL 2x1.5 (FC) (Option 2)

9 Functional Pin Description

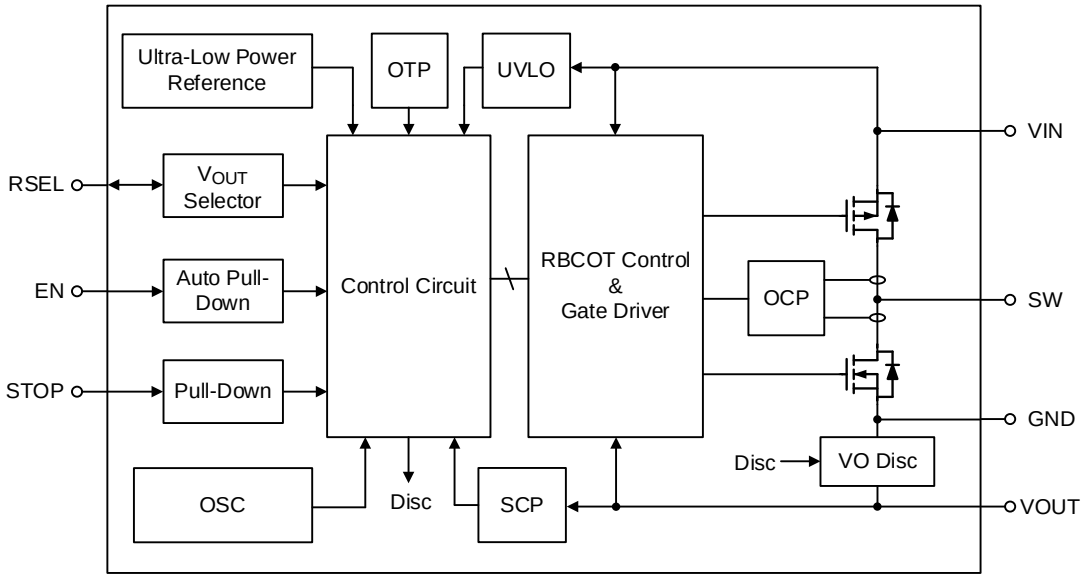
Pin No.		Pin Name	Pin Function
XWL-CSP-6B 0.96x1.245 (BSC)	WDFN-8JAL 2x1.5 (FC)		
A1	1, 3	GND	Device ground pin. This pin should be connected to the input and output capacitors with the shortest path.
A2	8	VOUT	Output voltage feedback pin. This pin should be connected close to the output capacitor terminal for better voltage regulation. A ceramic capacitor of sufficient value should be connected to this pin with the shortest path.
B1	2	VIN	Power input. A ceramic capacitor of sufficient value should be connected to this pin with the shortest path.
B2	7	SW	This pin is the connection between two built-in switches in the chip, which should be connected to the external inductor. The inductor should be connected to this pin with the shortest path.
C1	4	EN	Chip enable input pin. A high-level voltage enables the device, while a low-level voltage turns the device off. This pin must be terminated.
C2	5	RSEL	Connect a resistor to GND to set the V_{OUT} when the converter is enabled.
--	6	STOP (Option 1)	STOP switching pin. When this pin is logic high, the converter stops switching to provide a quiet supply rail. The output is powered from the charge available in the C_{OUT}. When this pin is logic low, the converter immediately resumes operation. The pin features an auto-pulldown circuit, which is disabled once a high level is detected at the input. The auto-pulldown circuit is activated again once a low level has been detected.
		FAULT (Option 2)	It is an open-drain output. The FAULT pin pulls low automatically if an OCP, SCP, OTP or UVLO event occurs.

10 Functional Block Diagram

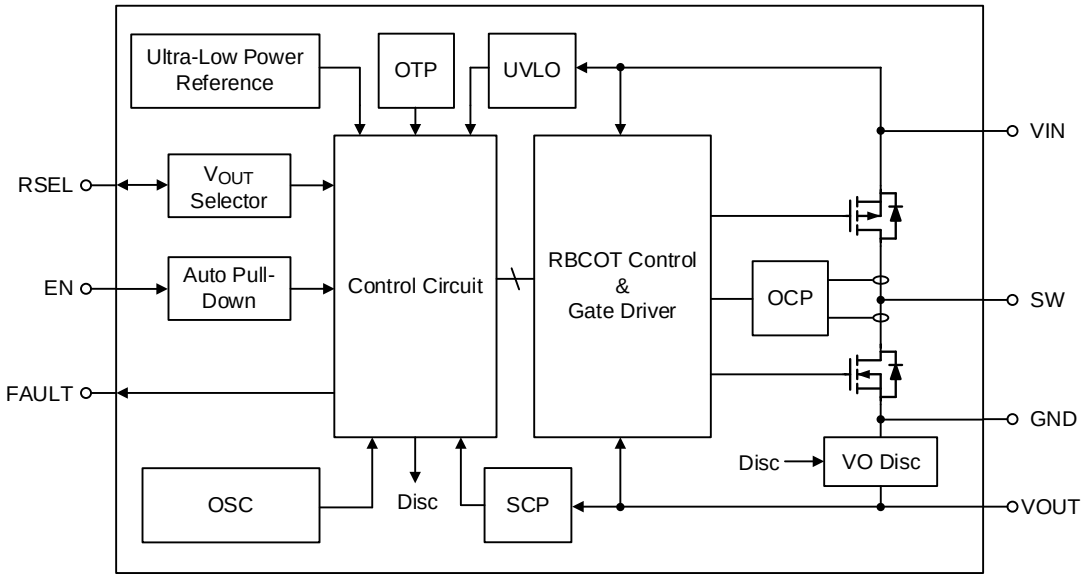
10.1 XWL-CSP-6B 0.96x1.245 (BSC)



10.2 WDFN-8JAL 2x1.5 (FC) Option 1: STOP Function



10.3 WDFN-8JAL 2x1.5 (FC) Option 2: FAULT Function



11 Absolute Maximum Ratings

(Note 2)

- VIN, VOUT, RSEL, FAULT, EN, STOP ---------- –0.3V to 6V
- SW (DC) ---------- –0.3V to V_{IN} + 0.3V
- SW (AC), Less than 10ns ---------- –2V to 7V
- Power Dissipation, P_D @ T_A = 25°C

  XWL-CSP-6B 0.96x1.245 (BSC) ---------- 1.26W

  WDFN-8JAL 2x1.5 (FC) ---------- 0.81W
- Package Thermal Resistance (Note 3 and Note 4)

  XWL-CSP-6B 0.96x1.245 (BSC), θ_{JA} ---------- 79.46°C/W

  WDFN-8JAL 2x1.5 (FC), θ_{JA} ---------- 123.73°C/W

  WDFN-8JAL 2x1.5 (FC), θ_{JC} ---------- 16.5°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 5)

  HBM (Human Body Model) ---------- ±2kV

Note 2. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 3. For XWL-CSP-6B 0.96x1.245 (BSC), θ_{JA} is simulated under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-9 thermal measurement standard.

Note 4. For WDFN-8JAL 2x1.5 (FC), θ_{JA} is simulated under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. θ_{JC} is simulated at the bottom of the package.

Note 5. Devices are ESD sensitive. Handling precautions are recommended.

12 Recommended Operating Conditions

(Note 6)

- Supply Input Voltage ---------- 1.8V to 5.5V
- External Maximum Parasitic Capacitance at RSEL Pin, C_{RSEL_MAX} ---------- 100pF
- External Voltage Selection Resistor, R_{SET} ---------- 0.909kΩ to 267kΩ
- RT5717 Output Current 1 (V_{IN} = 1.8V to 5.5V) ---------- 0mA to 750mA
- RT5717 Output Current 2 (V_{IN} = 2.2V to 5.5V) ---------- 0mA to 1200mA
- RT5717 Output Current 3 (V_{IN} = 2.3V to 5.5V) ---------- 0mA to 1500mA
- Ambient Temperature Range ---------- –40°C to 85°C
- Junction Temperature Range ---------- –40°C to 125°C

Note 6. The device is not guaranteed to function outside its operating conditions.

13 Electrical Characteristics

(V_{IN} = 3.6V, T_J = –40°C to 125°C, unless otherwise specified.)

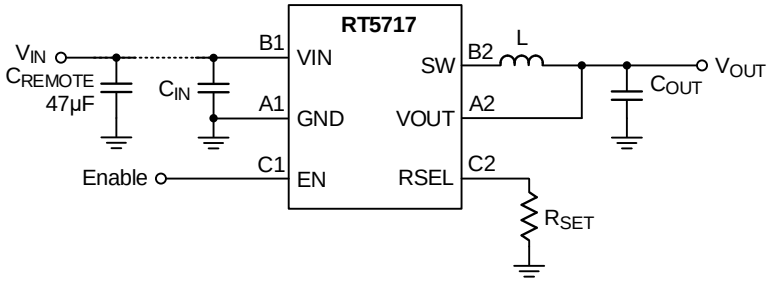
Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Buck Regulator							
Undervoltage-Lockout Rising Threshold	V_{UVLO_R}	Rising V_{IN}		--	1.73	--	V
Undervoltage-Lockout Falling Threshold	V_{UVLO_F}			--	1.68	--	V
Undervoltage-Lockout Deglitch Time	$t_{DEGLITCH\_UVLO}$			--	32	--	µs
Quiescent Current into VIN (Switching)	$I_{Q\_VIN\_SW}$	EN = V_{IN} = 3.6V, I_{OUT} = 0A, V_{OUT} = 1.8V		--	60	--	nA
		EN = V_{IN} = 3.6V, I_{OUT} = 0A, V_{OUT} = 1.2V		--	60	--	
Quiescent Current into VIN Pin (Non-Switching)	$I_{Q\_VIN\_NSW}$	EN = V_{IN} = 3.6V, I_{OUT} = 0A, V_{OUT} = 1.8V	WDFN-8JAL 2x1.5 (FC) (25°C)	--	36	100	nA
			XWL-CSP-6B 0.96x1.245 (BSC) (T_J = –40°C to 85°C)	--	36	360	
Quiescent Current into VOUT Pin (Non-Switching)	$I_{Q\_VOUT\_NSW}$	EN = V_{IN} = 3.6V, I_{OUT} = 0A, V_{OUT} = 1.8V	WDFN-8JAL 2x1.5 (FC) (25°C)	--	56	120	nA
			XWL-CSP-6B 0.96x1.245 (BSC) (T_J = –40°C to 85°C)	--	56	170	
		EN = V_{IN} = 3.6V, I_{OUT} = 0A, V_{OUT} = 3.3V, T_J = –40°C to 85°C		--	70	300	
		EN = V_{IN} = 3.6V, I_{OUT} = 0A, V_{OUT} < 1.5V		--	56	--	
Quiescent Current (Bypass Mode)	I_{Q_BYP}	V_{IN} = V_{OUT} = 3.3V		--	120	--	nA
Operating Quiescent current into VIN Pin	$I_{Q\_VIN\_STOP}$	V_{IN} = 3.6, V_{OUT} = 1.8V, STOP = High		--	20	--	µA

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Shutdown Current	I_{SHDN}	EN = GND, shutdown current into VIN, RSEL = GND, T_J = –40°C to 85°C	--	25	300	nA
Switching Frequency	f_{SW}	EN = V_{IN}, V_{OUT} = 1.8V (PWM)	--	1.5	--	MHz
Positive Inductor Peak Current Limit	I_{LIM_PEAK}	T_J = –40°C to 85°C, OCP Select 1 = 1.2A	1	1.2	1.4	A
		T_J = –40°C to 85°C, OCP Select 2 = 2.04A	1.84	2.04	2.24	
		T_J = –40°C to 85°C, OCP Select 3 = 2.4A	2.13	2.4	2.67	
Positive Inductor Valley Current Limit	I_{LIM_VALLEY}	T_J = –40°C to 85°C, OCP Select 1 = 1.2A	0.95	1.14	1.32	A
		T_J = –40°C to 85°C, OCP Select 2 = 2.04A	1.72	1.9	2.07	
		T_J = –40°C to 85°C, OCP Select 3 = 2.4A	1.93	2.26	2.47	
Negative Inductor Peak Current Limit	$I_{LIM\_PEAK\_NEG}$		--	–1.67	--	A
Current Limit Propagation Delay	t_{DLY_LIM}		--	170	--	ns
UGATE R_{ON}	R_{ON_H}	V_{IN} = 5V, I = 200mA	--	120	--	mΩ
LGATE R_{ON}	R_{ON_L}	V_{IN} = 5V, I = 200mA	--	50	--	mΩ
Leakage Current into the SW Pin	I_{LK_SW}	V_{SW} = 5.5V	--	10	--	nA
Output Discharge Resistor	R_{DISCHG}	EN = GND, sink current 35mA into the VOUT pin, V_{OUT} = 1.8V	--	50	--	Ω
Output Voltage Accuracy	V_{OUT_ACC}	PWM mode, I_{OUT} = 300mA, V_{OUT} = 0.5V to 1.5V	–22.5	--	22.5	mV
		PWM mode, V_{OUT} = 1.8V, I_{OUT} = 300mA	–1.5	--	1.5	%
Load Regulation	V_{LOAD_REG}	V_{IN} = 3.6V, V_{OUT} = 1.8V, PWM	–1.5	--	1.5	%
Line Regulation	V_{LINE_REG}	REG V_{OUT} = 1.8V, I_{OUT} = 100mA, PWM	--	0	--	%
Auto Bypass Mode Leave Detection Threshold	V_{TH_BYP+}	Rising V_{OUT}, bypass mode is left with V_{OUT} = V_{OUT} + V_{TH_BYP+}	--	80	--	mV
Auto Bypass Mode Enter Detection Threshold	V_{TH_BYP-}	Falling V_{IN}, bypass mode is entered with V_{IN} = V_{OUT} + V_{TH_BYP-}	--	30	--	mV
Over-Temperature Protection	T_{OTP}	V_{IN} = 3.6V, V_{OUT} = 1.8V	--	160	--	°C
Over-Temperature Protection Hysteresis	T_{OTP_HYS}		--	30	--	°C

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage Ripple	V_{OUT_RIPPLE}	L = 1μH, C_{OUT} = 10μF V_{IN} = 3.6V, V_{OUT} = 1.2V, PFM	--	50	--	mV
		L = 1μH, C_{OUT} = 10μF V_{IN} = 3.6V, V_{OUT} = 1.2V, PWM	--	10	--	
Timing						
Regulator Start-Up Delay Time	t_{DLY_EN}	V_{IN} = 3.6V, EN = GND to V_{IN}, V_{OUT} starts switching	--	0.68	--	ms
	t_{DLY_VIN}	V_{IN} = 0V to 3.6V (<100μs), EN = V_{IN}, V_{OUT} starts switching	--	4.95	--	ms
Soft-Start Time	t_{SS}	V_{IN} = 3.6V, V_{OUT} = 1.8V, C_{OUT} = 10μF, I_{OUT} = 0mA, EN = V_{IN}	--	1.3	--	ms
Logic Input (EN, STOP Inputs)						
Input Voltage Logic High	V_{IH}	V_{IN} = 1.8V to 5.5V	1.2	--	--	V
Input Voltage Logic Low	V_{IL}	V_{IN} = 1.8V to 5.5V	--	--	0.4	V
EN Pin Leakage Current	I_{LK_EN}	EN = V_{IN} = 5.5V	--	10	--	nA
Internal Pull-Down Resistance	R_{PD}	EN, STOP pin to GND	200	450	--	kΩ

14 Typical Application Circuit

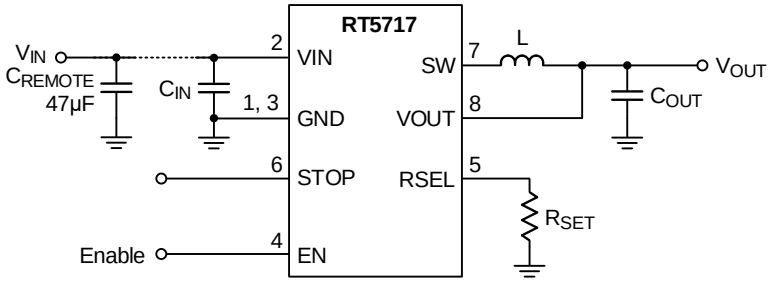
14.1 XWL-CSP-6B 0.96x1.245 (BSC)



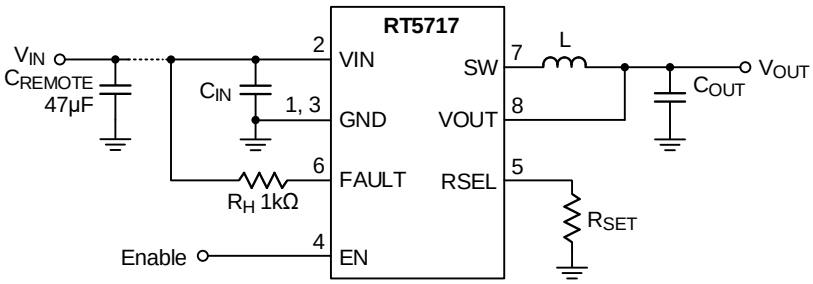
Reference	Part Number	Value	Package	Manufacturer
C_{IN}	GRM155R60J475ME47D	4.7µF/6.3V/X5R	0402	Murata
C_{OUT}	GRM155R60J106ME15	10µF/6.3V/X5R	0402	Murata
C_{REMOTE} (Note 7)	GRM21BR61A476ME15L	47µF/10V/X5R	0805	Murata
L	DFE201610E-1R0M	1µH	0806	Murata
R_{SET}	Resistor E96 series 1%, TC ±200ppm	See Table 1. Output Voltage Setting	--	--

Note 7. C_{REMOTE} is an additional input capacitor that is not essential for normal operation. However, it can be utilized to minimize input voltage ripple.

14.2 WDFN-8JAL 2x1.5 (FC) Option 1: STOP Function



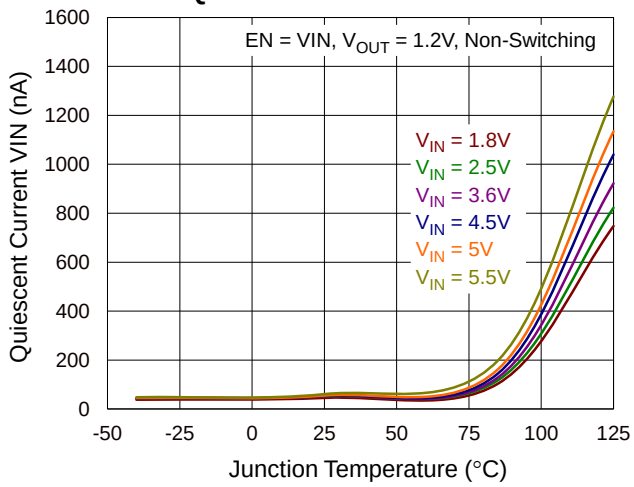
14.3 WDFN-8JAL 2x1.5 (FC) Option 2: FAULT Function



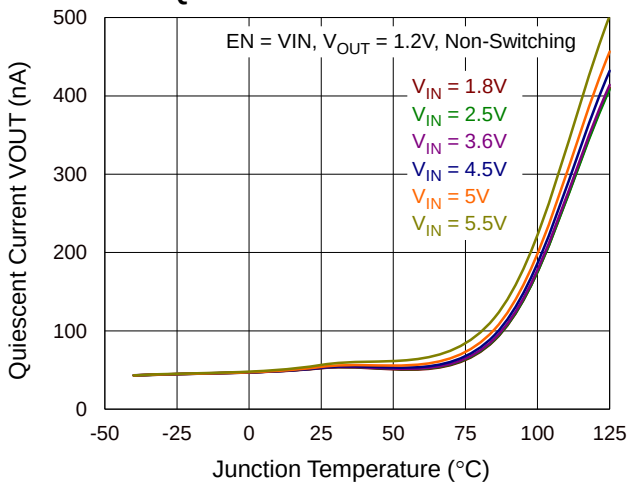
Reference	Part Number	Value	Package	Manufacturer
C_{IN}	GRM155R60J475ME47D	4.7µF/6.3V/X5R	0402	Murata
C_{OUT}	GRM155R60J106ME15	10µF/6.3V/X5R	0402	Murata
C_{REMOTE} (Note 7)	GRM21BR61A476ME15L	47µF/10V/X5R	0805	Murata
L	DFE201610E-1R0M	1µH	0806	Murata
R_{SET}	Resistor E96 series 1%, TC ±200ppm	See Table 1. Output Voltage Setting	--	--

15 Typical Operating Characteristics

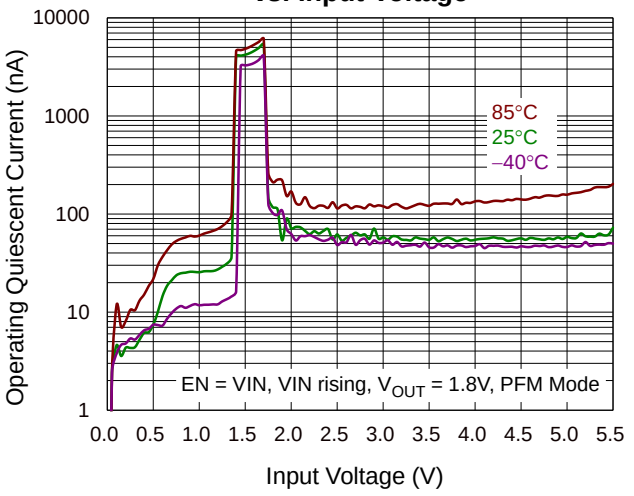
Quiescent Current into VIN



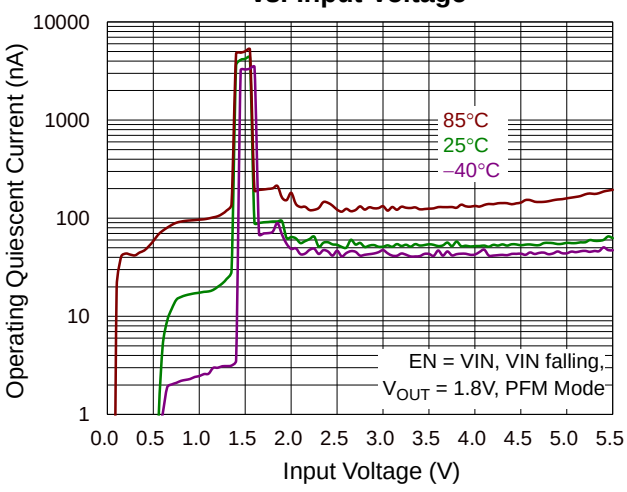
Quiescent Current into VOUT



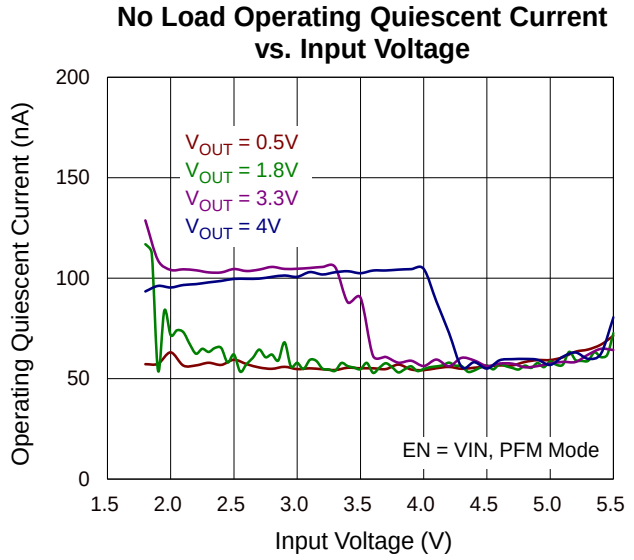
No Load Operating Quiescent Current vs. Input Voltage



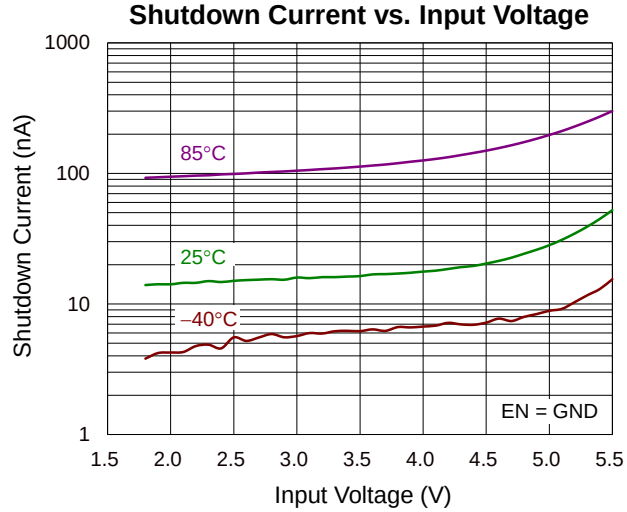
No Load Operating Quiescent Current vs. Input Voltage



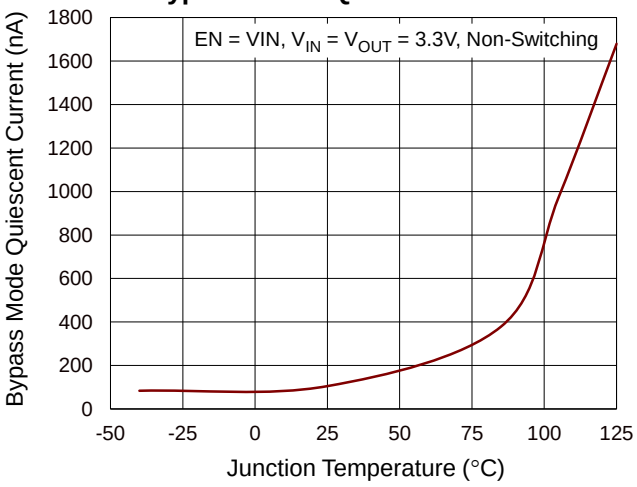
No Load Operating Quiescent Current vs. Input Voltage



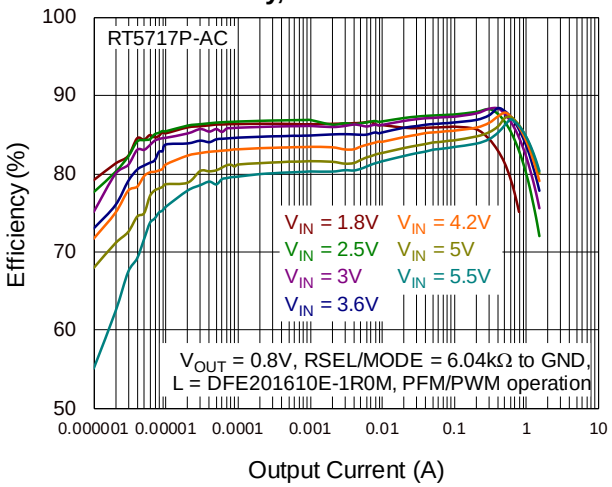
Shutdown Current vs. Input Voltage



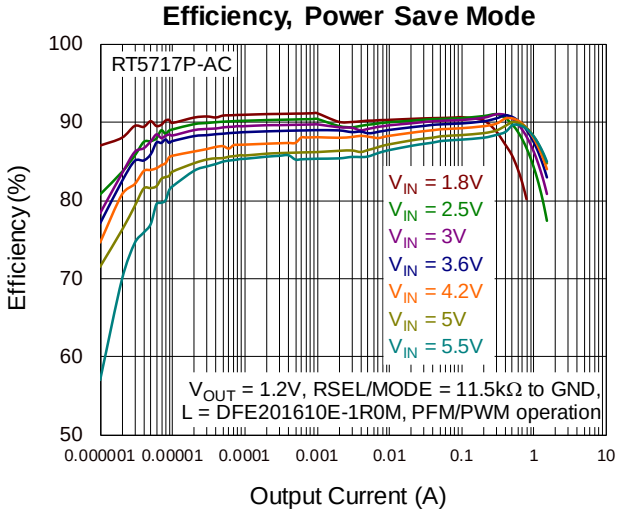
Bypass Mode Quiescent Current



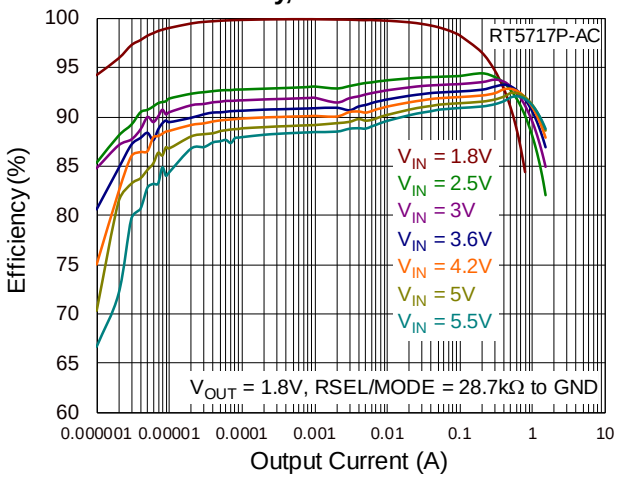
Efficiency, Power Save Mode



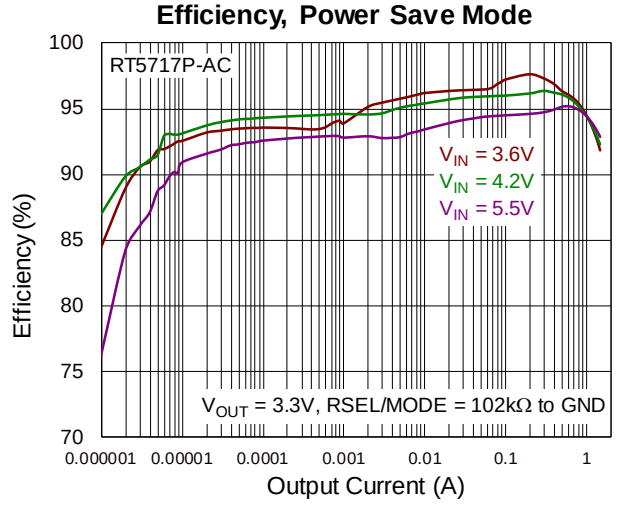
Efficiency, Power Save Mode



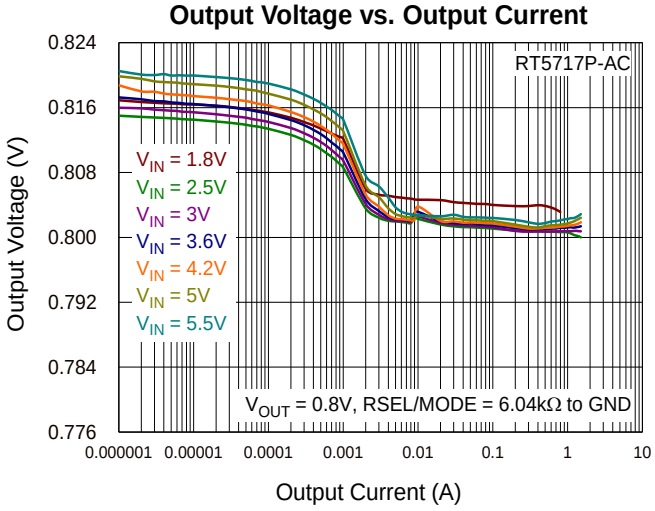
Efficiency, Power Save Mode



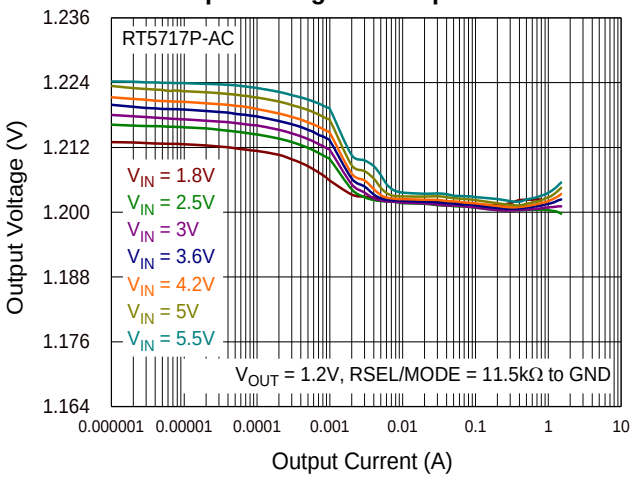
Efficiency, Power Save Mode



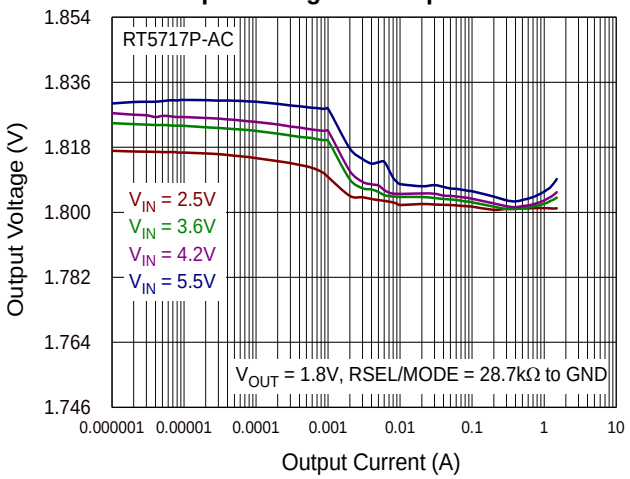
Output Voltage vs. Output Current



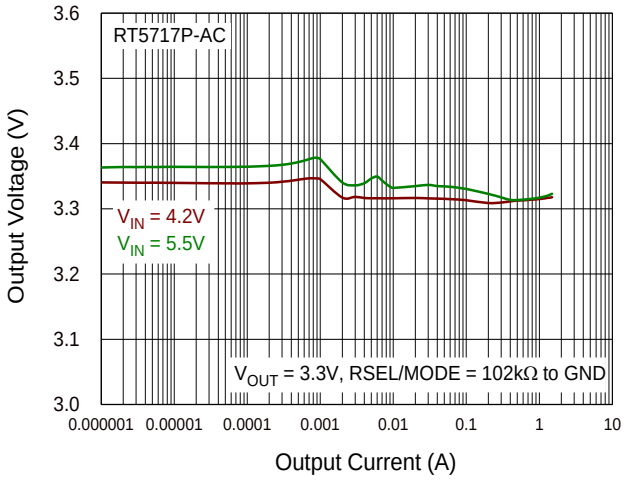
Output Voltage vs. Output Current



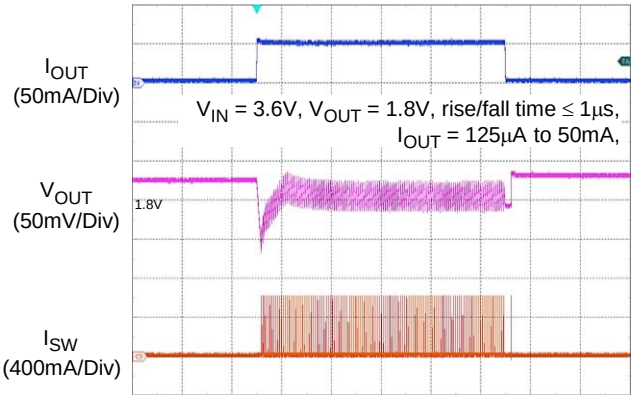
Output Voltage vs. Output Current



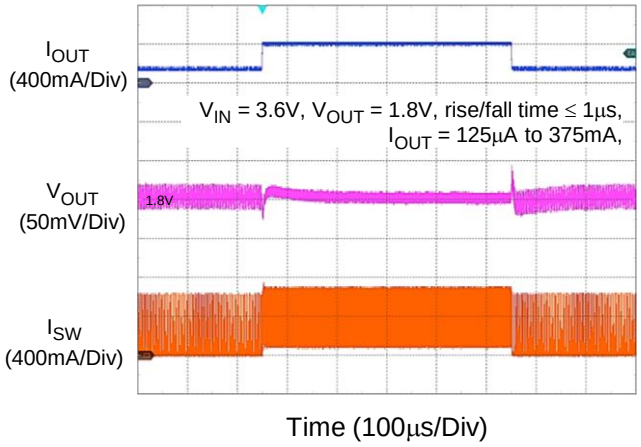
Output Voltage vs. Output Current



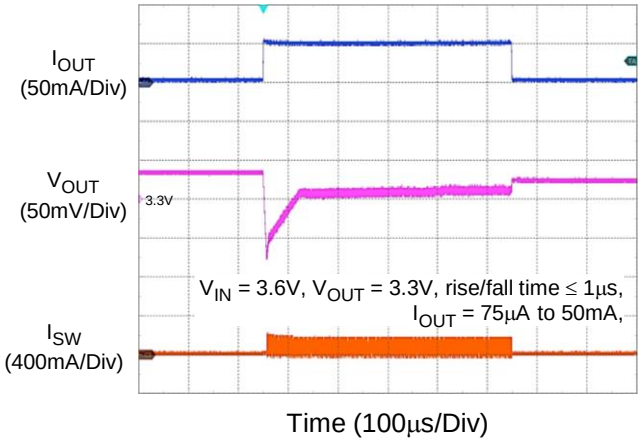
Load Transiet PSM Mode



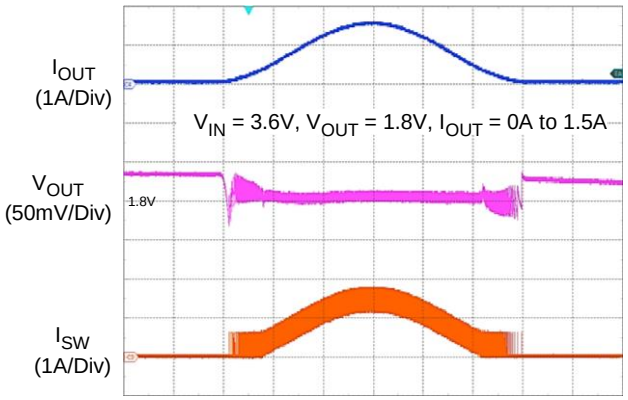
Load Transiet PSM Mode



Load Transiet PSM Mode

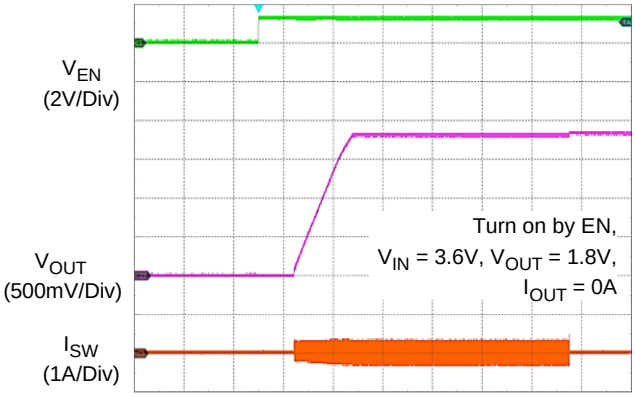


AC Load Sweep Power Save Mode



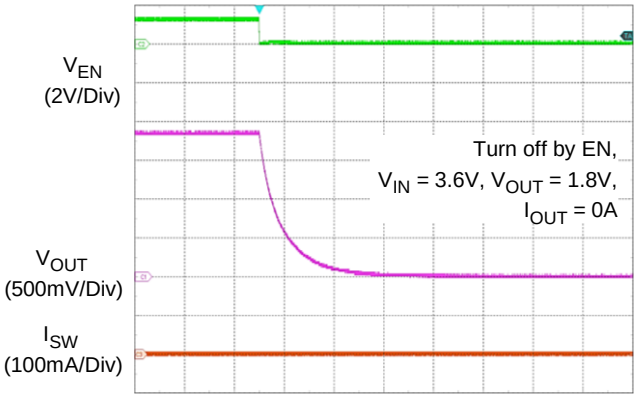
Time (200μs/Div)

Start-Up



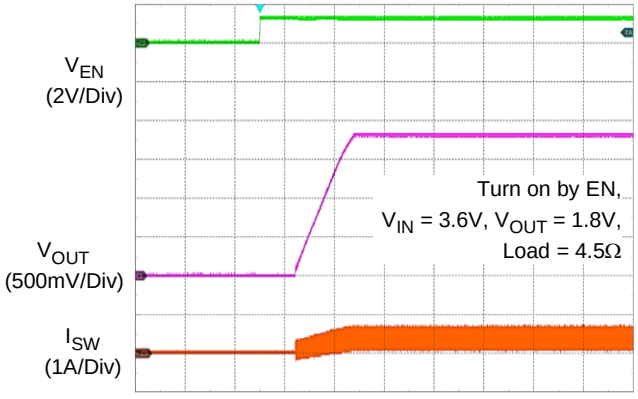
Time (1ms/Div)

Output Discharge



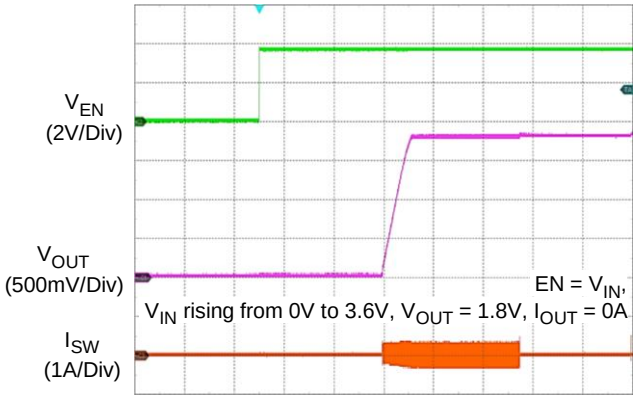
Time (400μs/Div)

Start-Up



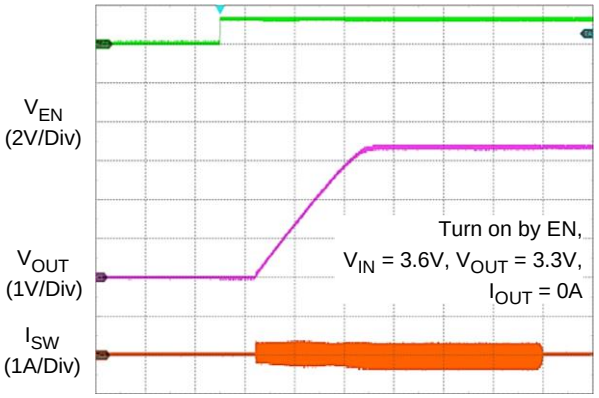
Time (1ms/Div)

Start-Up



Time (2ms/Div)

Start-Up



Time (1ms/Div)

16 Operation

The RT5717 is a Ripple-Based Constant-On-Time (RBCOT) switching buck converter with typical 60nA ultra-low quiescent current. The RT5717 provides over-temperature protection and overcurrent protection mechanisms to prevent the device from being damaged during abnormal operations. When the EN voltage is logic low, the IC will be shut down with 25nA shutdown current.

16.1 Enable

The device can be enabled or disabled by the EN pin. When the EN pin is higher than the logic-high threshold, the IC enters normal operation. When the EN pin is set to low, the device transitions to shutdown mode. In shutdown mode, the converter stops switching, the internal control circuitry turns off, and the discharge function is triggered. The EN low level time must be longer than 200μs for the internal circuit reset time.

16.2 Undervoltage-Lockout Protection

To protect the chip from operating at insufficient supply voltage, UVLO is required. When the input voltage is lower than the UVLO falling threshold, the device will be in lockout.

16.3 Bypass Mode Operation

The converter enters bypass mode operation once the input voltage decreases and the difference between the input and output voltage is lower than V_{TH_BYP-}. The output voltage follows the input voltage minus the voltage drop across the internal P-MOSFET and the inductor. Once the output voltage increases and reaches the bypass mode exit threshold, V_{TH_BYP+}, the converter returns to normal switching operation.

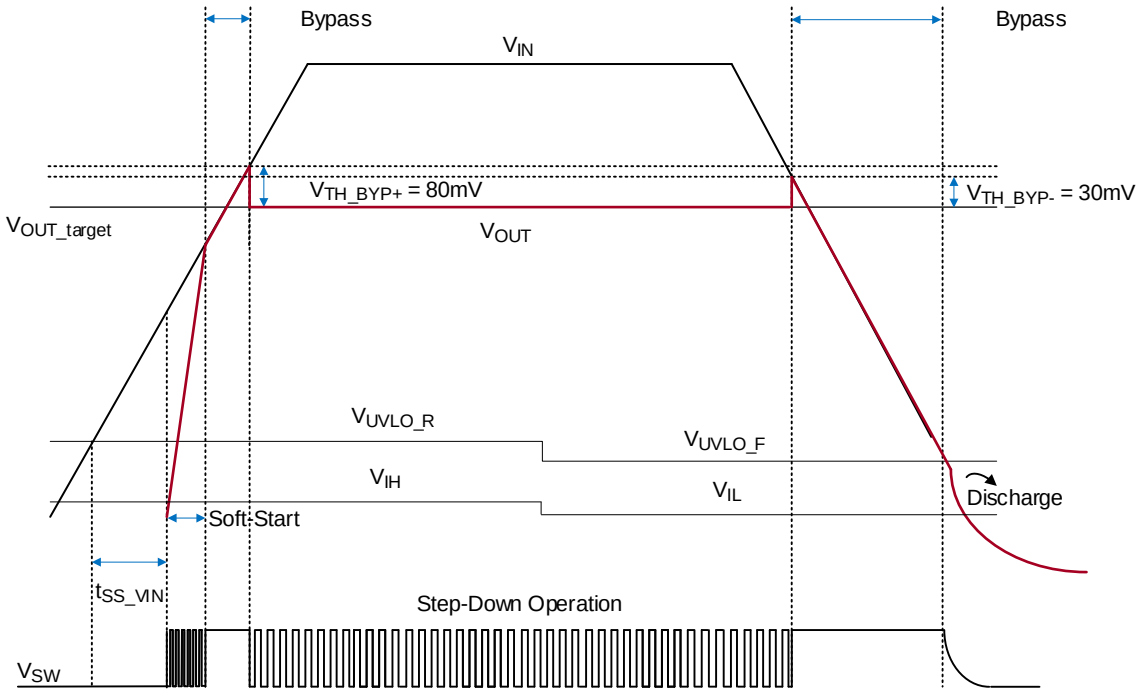


Figure 1. Auto Bypass Mode

16.4 Over-Temperature Protection

When the junction temperature exceeds the OTP threshold, the IC will shut down the switching operation. Once the junction temperature cools down and falls below the OTP lower threshold, the converter will automatically resume switching.

16.5 STOP

The device allows the user to temporarily stop the switching of the regulator using the STOP input pin. The function is only available on the WDFN-8JAL 2x1.5 (FC) package. When STOP = H, the device is forced to stop switching after the current switching cycle. When STOP = L, the device will resume switching operation without a start-up delay or soft-start. In STOP mode, the device typically consumes 20μA operating quiescent current from the input supply, and there is no switching noise, making it suitable for noise-sensitive applications.

16.6 FAULT

The FAULT pin is an output pin that turns low when the device enters protection states (OCP, SCP, OTP, UVLO). The FAULT pin will be high when the device is in normal operation.

16.7 Overcurrent Protection and Short Circuit Protection

The OCP and SCP functions are implemented by high-side MOSFET and low-side MOSFET. When the inductor current reaches the peak current-limit threshold, the high-side MOSFET will turn off. The low-side MOSFET turns on to discharge the inductor current until it falls below the valley current-limit threshold. After peak current limit is triggered, the maximum inductor current is determined by the inductor current rising rate and the response delay time of the internal network.

During the OCP and SCP period, the output voltage drops below the set threshold (0.2V typical), and the current limit value is reduced to a low current limit level to lower device loss, reduce heat, and prevent further damage to the chip.

Due to internal propagation delay (t_{DLY_LIM} = 170ns), the actual inductor current can exceed the static current limit during that time.

The dynamic current limit can be calculated as follows:

$$I_{current\ limit\ peak} = I_{LIM\_PEAK} + \frac{(V_{IN} - V_{OUT})}{L} \times t_{DLY\_LIM}$$

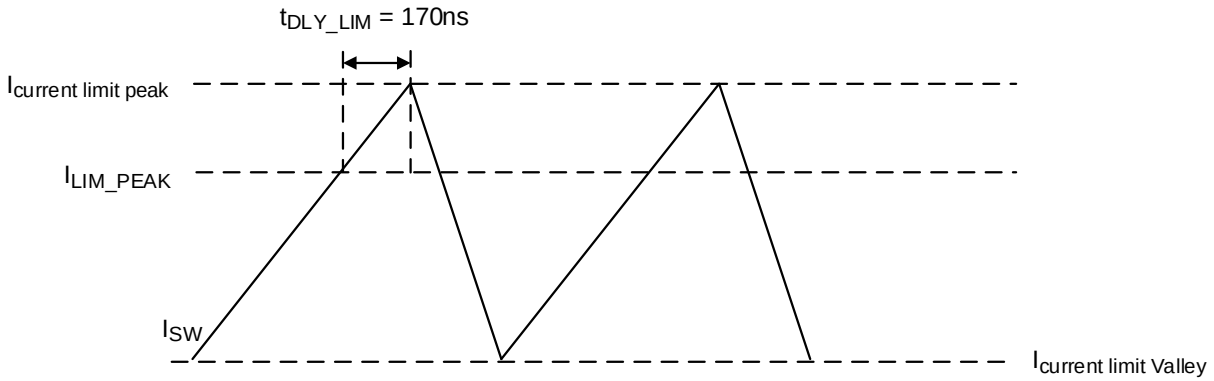


Figure 2. Current Limit

16.8 Output Voltage Selection

The RT5717 provides 16 selectable output voltages that can be set with a single external resistor connected between the RSEL pin and GND. The V_{OUT} select circuit starts to detect the value of the resistor when the converter is enabled, and the control circuit is powered up.

No parasitic current, capacitance between the RSEL pin and GND pin.

Table 1. Output Voltage Setting

Type	Output-1	Output-2	Output-3	Output-4	Output-5	RSEL (Ω)		
Level	0.5V to 4V	0.8V to 1.55V	1.8V to 3.3V	1.8V to 3.6V	0.54V to 3.6V	Min	Typ	Max
0	0.50	0.80	1.8	1.8	--	0	GND	0.01k
1	0.58	0.85	1.9	2.0	0.54	0.87k	0.909k	0.95k
2	0.60	0.90	2.0	2.2	0.56	1.67k	1.74k	1.81k
3	0.70	0.95	2.1	2.4	0.65	2.76k	2.87k	2.98k
4	0.75	1.00	2.2	2.5	0.70	4.15k	4.32k	4.49k
5	0.80	1.05	2.3	2.6	0.74	5.80k	6.04k	6.28k
6	1.10	1.10	2.4	2.7	1.00	8.11k	8.45k	8.79k
7	1.20	1.15	2.5	2.8	1.10	11.04k	11.5k	11.96k
8	1.50	1.20	2.6	2.9	1.40	15.17k	15.8k	16.43k
9	1.60	1.25	2.7	3.0	1.50	20.64k	21.5k	22.36k
10	1.80	1.30	2.8	3.1	1.65	27.55k	28.7k	29.85k
11	1.90	1.35	2.9	3.2	1.75	36.77k	38.3k	39.83k
12	2.10	1.40	3.0	3.3	1.95	50.21k	52.3k	54.39k
13	3.00	1.45	3.1	3.4	2.80	68.64k	71.5k	74.36k
14	3.30	1.50	3.2	3.5	3.05	97.92k	102k	106.08k
15	4.00	1.55	3.3	3.6	3.70	256.32k	267k	277.68k

17 Application Information

(Note 8)

The RT5717 is a high-efficiency synchronous buck converter with ultra-low quiescent current of typically 60nA. It supports an input voltage range from 1.8V to 5.5V and an output current of up to 750mA, 1.2A, or 1.5A.

It provides high efficiency at light loads down to 1μA. Internal compensation is integrated to minimize the external component count. Protection features include overcurrent protection, undervoltage protection, and over-temperature protection.

17.1 Inductor Selection

The recommended power inductor is 1μH.

The inductor saturation current rating needs to be carefully chosen to follow the overcurrent protection design considerations. In applications, it is necessary to select an inductor with low DCR to provide good performance and efficiency.

17.2 C_{IN} and C_{OUT} Selection

The input capacitance, C_{IN}, is needed to filter the trapezoidal current at the source of the top MOSFET. To prevent large ripple voltage, a low ESR input capacitor sized for the maximum RMS current should be used. RMS current is given by:

$$I_{RMS} = I_{OUT(MAX)} \times \frac{V_{OUT}}{V_{IN}} \times \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

This formula has a maximum at $V_{IN} = 2 \times V_{OUT}$, where $I_{RMS} = I_{OUT}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. It is advisable to choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet size or height requirements in the design.

The selection of C_{OUT} is determined by the Effective Series Resistance (ESR) that is required to minimize voltage ripple and load step transients, as well as the amount of bulk capacitance necessary to ensure that the control loop is stable. Loop stability can be checked by viewing the load transient response as described in a later section.

The output ripple, ΔV_{OUT}, is determined by:

$$\Delta V_{OUT} \leq \Delta I_L \left(ESR + \frac{1}{8 \times f_{SW} \times C_{OUT}} \right)$$

17.3 Power Sequence

There are three common power-on device scenarios:

1. EN is pulled high after V_{IN} has been established.
2. EN and V_{IN} are established at the same time.
3. V_{IN} is pulled high after EN has been established.

There will be two types of boot-up times. One is to enable the system after V_{IN} has been established, and after a period of t_{DLY_EN}, the device boots up. The other is that EN has been established before V_{IN} is pulled high, and after a period of delay, the device boots up.

There are two common power-off scenarios:

1. When V_{IN} is at a high level, and the EN is pulled low, and the device is powered off by EN.

2. When V_{IN} is pulled low, the device is powered off by UVLO after t_{UVLO_DT}.

To ensure complete discharge of the internal circuits when the device is powered off, it is recommended to power V_{IN} from 0V and have a >10ms interval between each power-up.

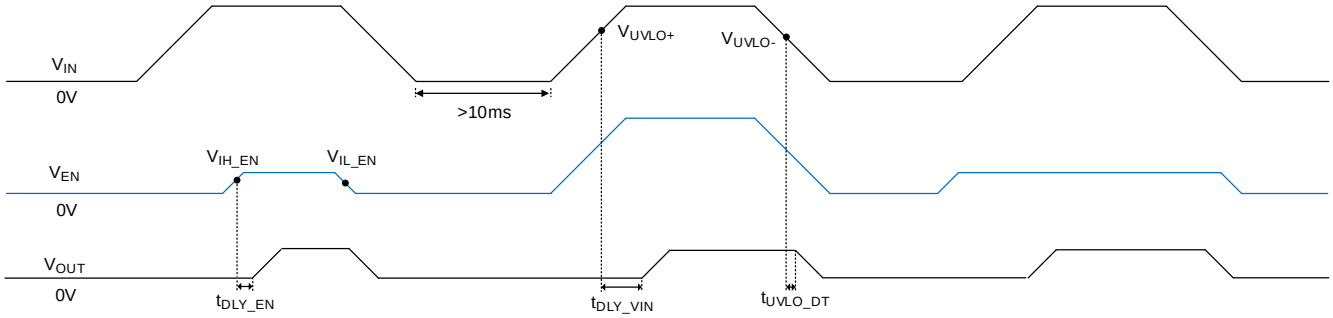


Figure 3. Power-On/Off Sequence

17.4 Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula:

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For an XWL-CSP-6B 0.96x1.245 (BSC) package, the thermal resistance, θ_{JA}, is 79.46°C/W on a standard JEDEC 51-9 high effective-thermal-conductivity four-layer test board. For a WDFN-8JAL 2x1.5 (FC) package, the thermal resistance, θ_{JA}, is 123.73°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below:

$P_{D(MAX)}$ = (125°C - 25°C) / (79.46°C/W) = 1.26W for a XWL-CSP-6B 0.96x1.245 (BSC) package.

$P_{D(MAX)}$ = (125°C - 25°C) / (123.73°C/W) = 0.81W for a WDFN-8JAL 2x1.5 (FC) package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curves in Figure 4 allow the designer to see the effect of rising ambient temperature on the maximum power dissipation.

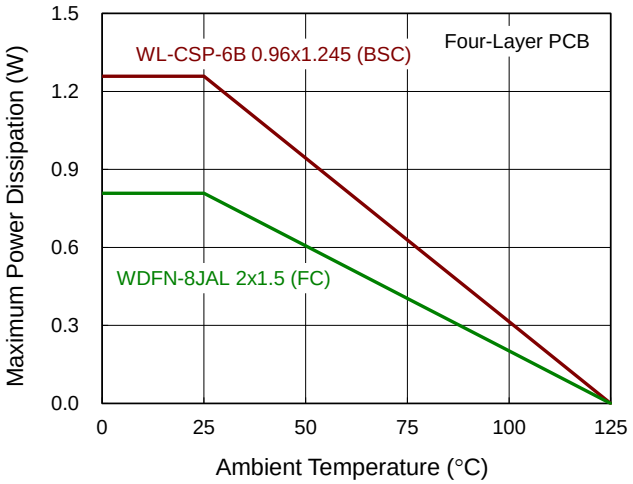


Figure 4. Derating Curves of Maximum Power Dissipation

17.5 Layout Considerations

For high-frequency switching power supplies, the PCB layout is crucial to get good regulation, high efficiency and stability. The following the guidelines can help achieve a better PCB layout.

- For good regulation, place the power components as close as possible. The traces should be wide and short, especially for the high-current loop.
- Shorten the SW node trace length and make it wide.

Table 2. Protection Trigger Condition and Behavior

Protection Type	Threshold Refer to Electrical Characteristics	Protection Method	Reset Method
OCP Select 1 for I_{OUT} = 750mA	I_{SW} > 1.2A (Typical)	Turn off UG MOS	I_{SW} < 1.14A (Typical)
OCP Select 2 for I_{OUT} = 1.2A	I_{SW} > 2.04A (Typical)		I_{SW} < 1.9A (Typical)
OCP Select 3 for I_{OUT} = 1.5A	I_{SW} > 2.4A (Typical)		I_{SW} < 2.26A (Typical)
UVLO	V_{IN} < 1.68V (Typical)	Shutdown	V_{IN} > 1.73V (Typical)
OTP	T_J > 160°C (Typical)	Shutdown	T_J < 130°C (Typical)

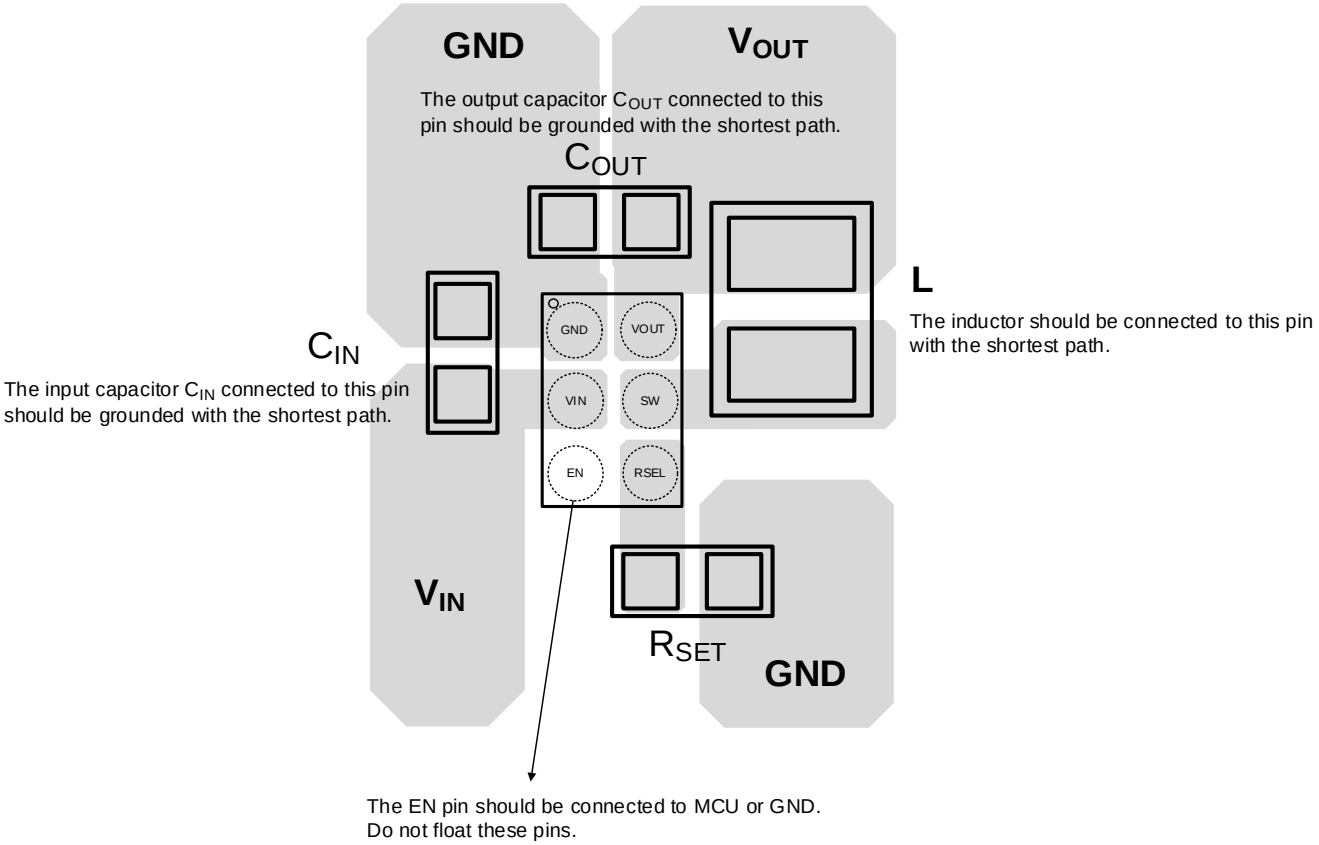


Figure 5. PCB Layout Guide for XWL-CSP-6B 0.96x1.245 (BSC) Package

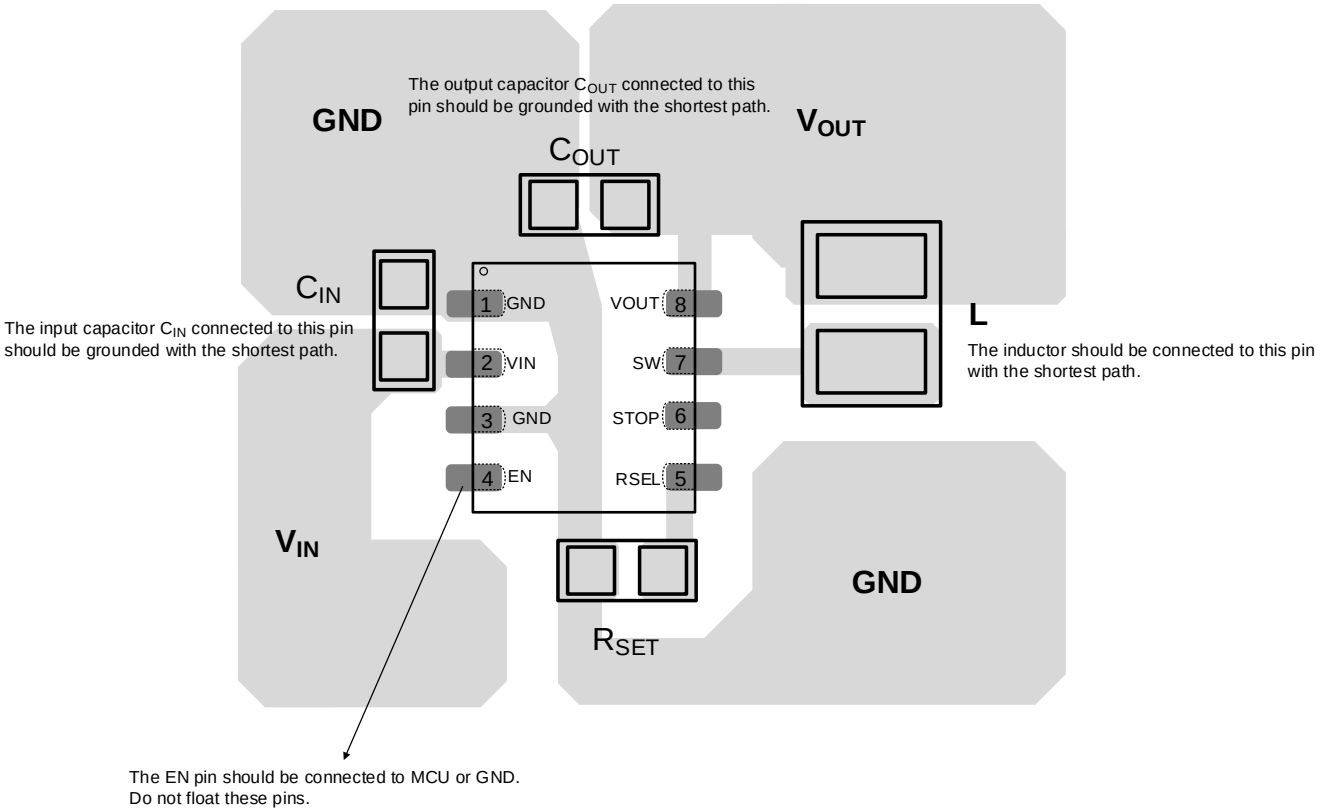


Figure 6. PCB Layout Guide for WDFN-8JAL 2x1.5 (FC) Package (Option 1)

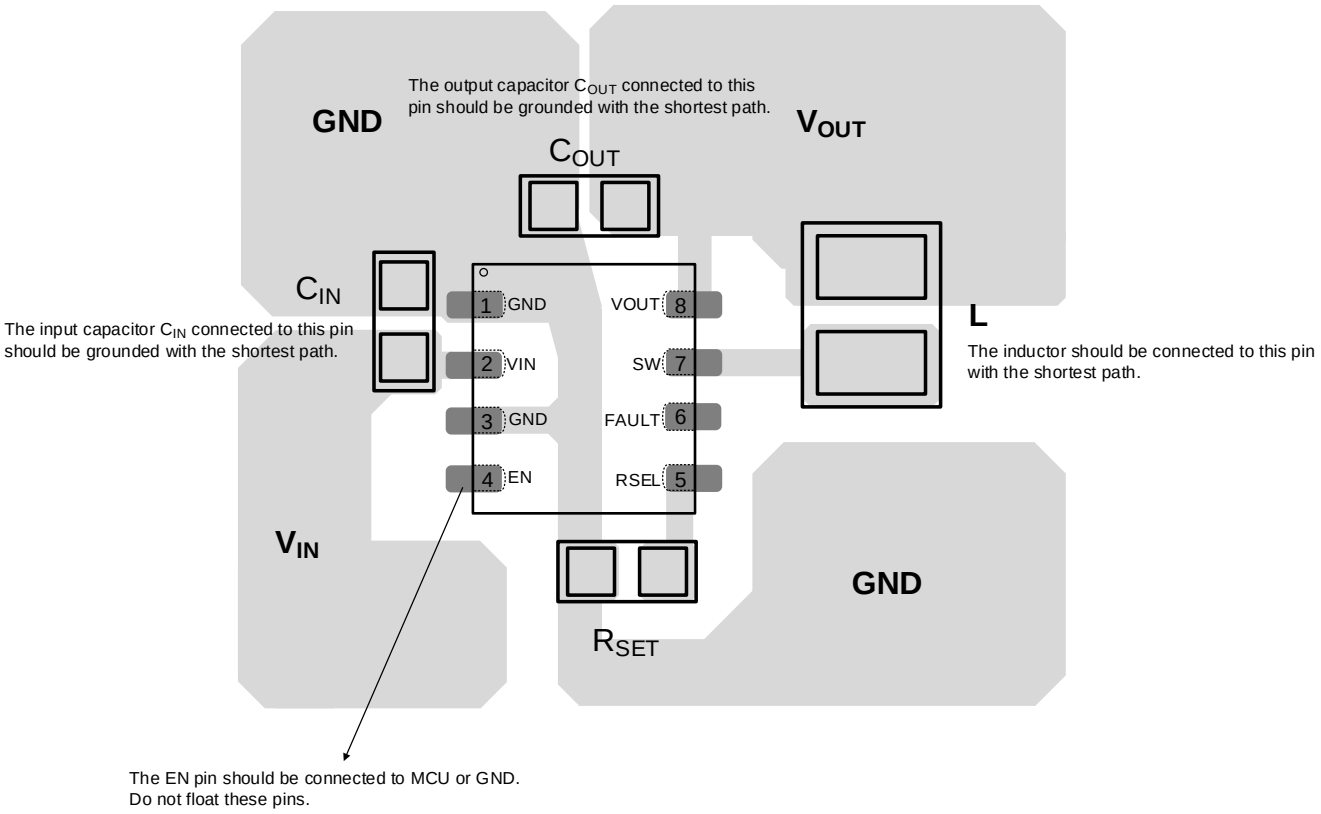
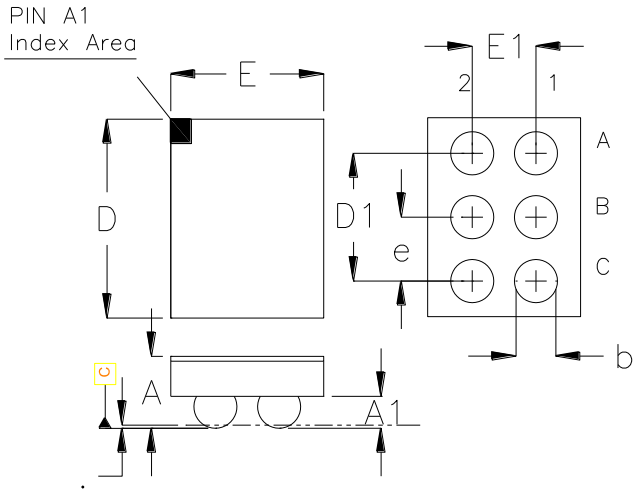


Figure 7. PCB Layout Guide for WDFN-8JAL 2x1.5 (FC) Package (Option 2)

Note 8. The information provided in this section is for reference only. The customer is solely responsible for designing, validating, and testing any applications incorporating Richtek's product(s). The customer is also responsible for applicable standards and any safety, security, or other requirements.

18 Outline Dimension

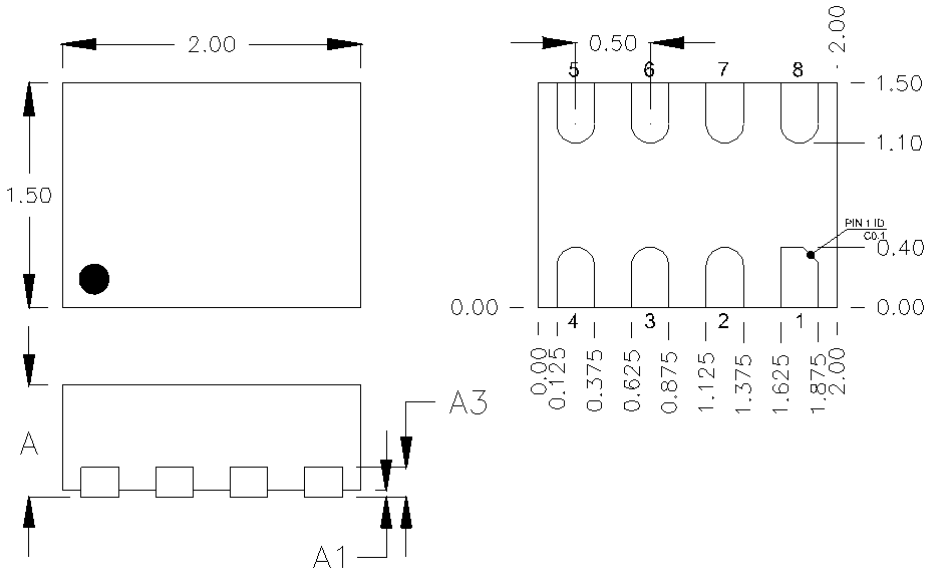
18.1 XWL-CSP-6B 0.96x1.245 (BSC)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.400	0.500	0.016	0.020
A1	0.170	0.230	0.007	0.009
b	0.240	0.300	0.009	0.012
D	1.215	1.275	0.048	0.050
D1	0.800		0.031	
E	0.930	0.990	0.037	0.039
E1	0.400		0.016	
e	0.400		0.016	
ccc	0.020		0.001	

6B XWL-CSP 0.96x1.245 Package (BSC)

18.2 WDFN-8JAL 2x1.5 (FC)



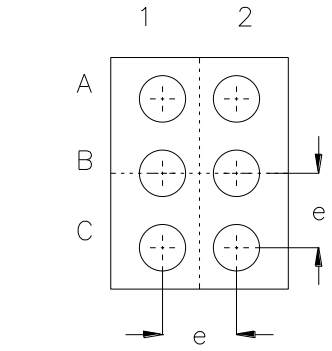
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010

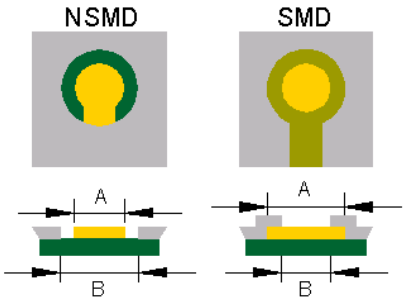
Tolerance (mm)
±0.050

W-Type 8JAL DFN 2x1.5 Package (FC)

19 Footprint Information

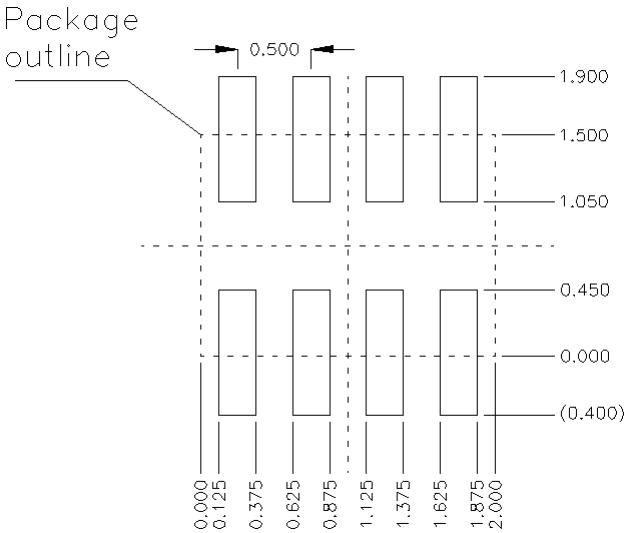
19.1 XWL-CSP-6B 0.96x1.245 (BSC)





Package	Number of Pin	Type	Footprint Dimension (mm)			Tolerance
			e	A	B	
XWL-CSP0.96x1.245-6(BSC)	6	NSMD	0.400	0.240	0.340	±0.025
		SMD		0.270	0.240	

19.2 WDFN-8JAL 2x1.5 (FC)

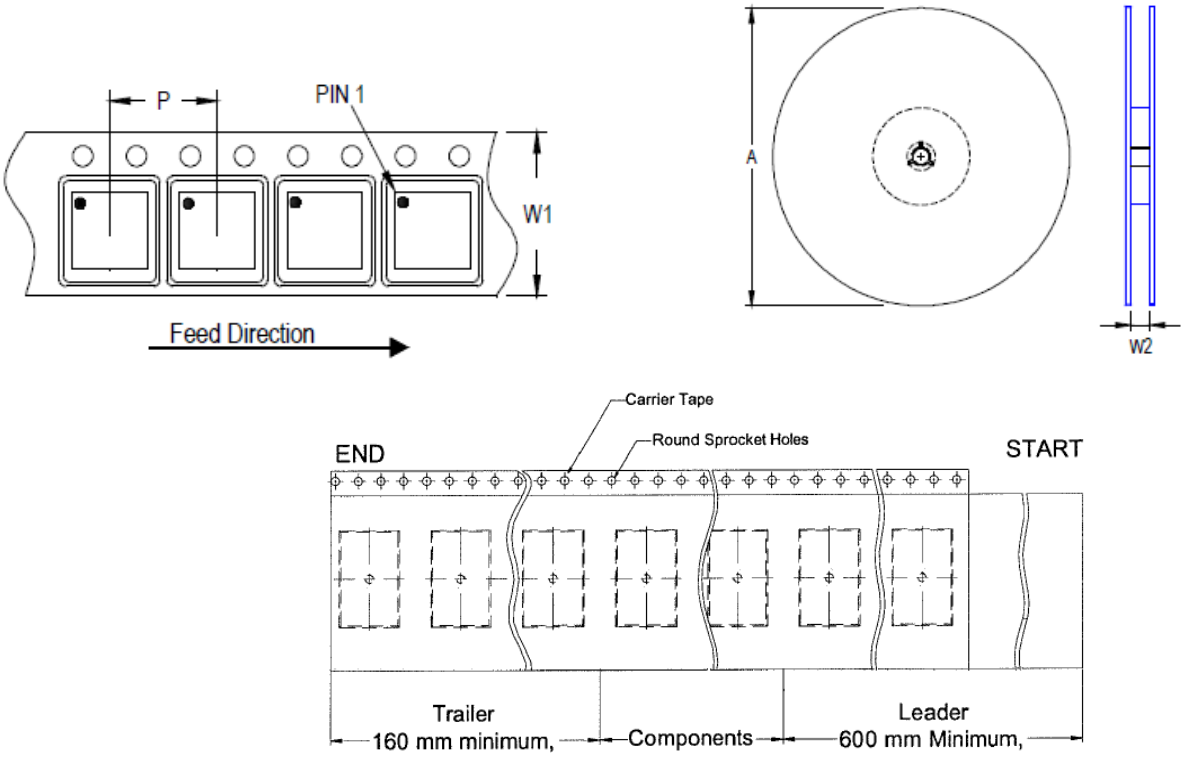


Package	Number of Pin	Tolerance
V/W/U/XDFN2x1.5-8JA(FC)	8	±0.05 mm

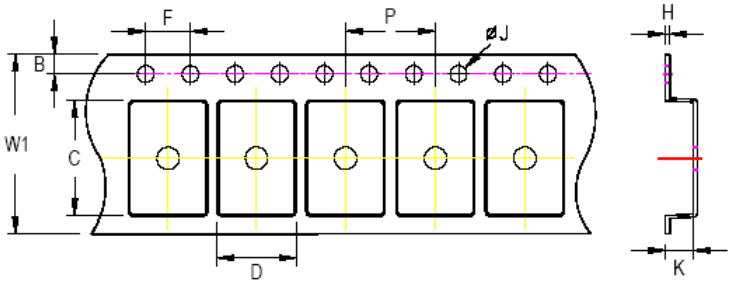
20 Packing Information

20.1 Tape and Reel Data

20.1.1 XWL-CSP-6B 0.96x1.245 (BSC)



Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min./Max. (mm)
			(mm)	(in)				
XWL-CSP 0.96x1.245	8	4	180	7	3,000	160	600	8.4/9.9

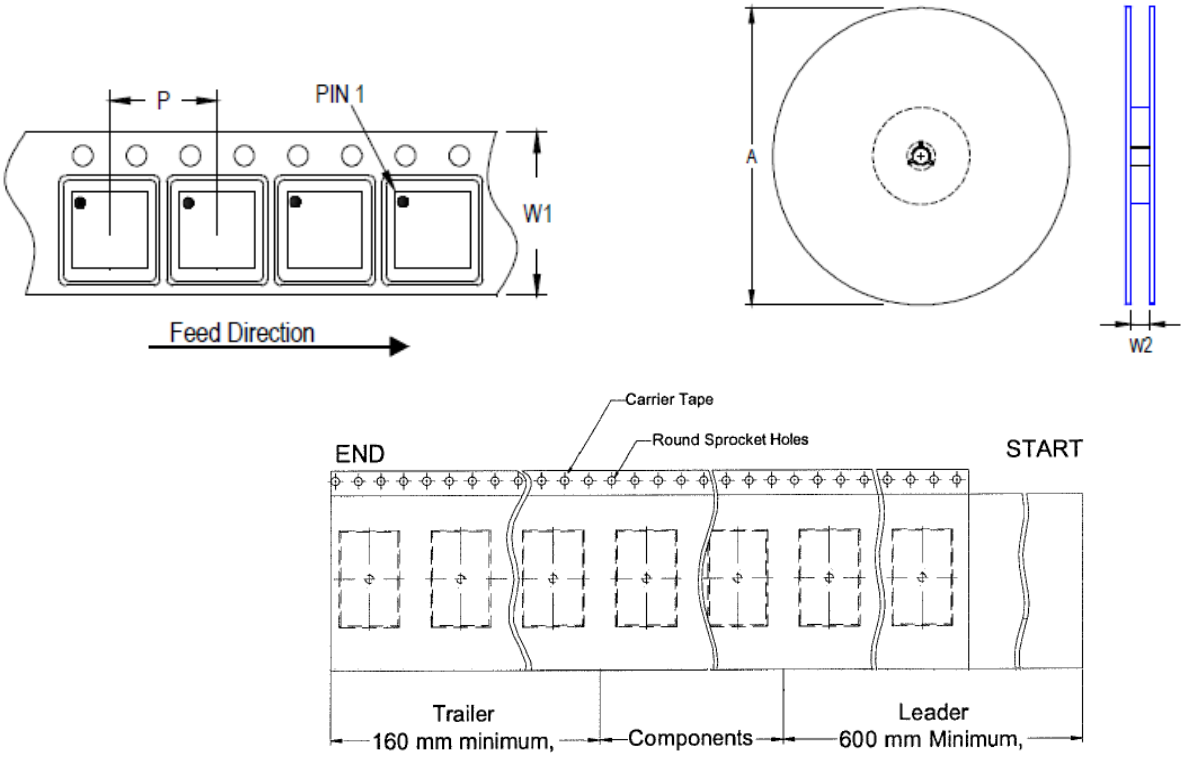


C, D, and K are determined by component size. The clearance between the components and the cavity is as follows:

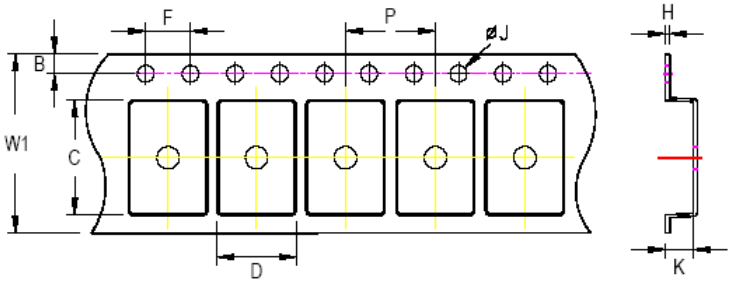
- For 8mm carrier tape: 0.5mm max.

Tape Size	W1	P		B		F		ØJ		K		H
	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Max
8mm	8.3mm	3.9mm	4.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	0.64mm	0.70mm	0.6mm

20.1.2 WDFN-8JAL 2x1.5 (FC)



Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min/Max (mm)
			(mm)	(in)				
(V, W) QFN/DFN 2x1.5	8	4	180	7	2,500	160	600	8.4/9.9



C, D, and K are determined by component size.

The clearance between the components and the cavity is as follows:

- For 8mm carrier tape: 0.5mm max.

Tape Size	W1	P		B		F		ØJ		K		H
	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Max
8mm	8.3mm	3.9mm	4.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	1.0mm	1.3mm	0.6mm

20.2 Tape and Reel Packing

20.2.1 XWL-CSP-6B 0.96x1.245 (BSC)

Step	Photo/Description	Step	Photo/Description
1	 Reel 7”	4	 12 inner boxes per outer box
2	 Packing by Anti-Static Bag	5	 Outer box **Carton A**
3	 3 reels per inner box **Box A**	6	

Container / Package	Reel		Box			Carton		
	Size	Units	Item	Reels	Units	Item	Boxes	Unit
XWL-CSP 0.96x1.245	7”	3,000	Box A	3	9,000	Carton A	12	108,000
			Box E	1	3,000	For Combined or Partial Reel.		

20.2.2 WDFN-8JAL 2x1.5 (FC)

Step	Photo/Description	Step	Photo/Description
1	 Reel 7”	4	 3 reels per inner box **Box A**
2	 HIC & Desiccant (1 Unit) inside	5	 12 inner boxes per outer box
3	 Caution label is on backside of Al bag	6	 Outer box **Carton A**

Container / Package	Reel		Box			Carton		
	Size	Units	Item	Reels	Units	Item	Boxes	Unit
QFN & DFN 2x1.5	7”	2,500	Box A	3	7,500	Carton A	12	90,000
			Box E	1	2,500	For Combined or Partial Reel.		

20.3 Packing Material Anti-ESD Property

Surface Resistance	Aluminum Bag	Reel	Cover tape	Carrier tape	Tube	Protection Band
Ω/cm^2	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**

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21 Datasheet Revision History

Version	Date	Description	Item
00	2025/3/24	Final	*Changed the names of pin C2 to RSEL and pin 3 to GND.* *General Description on page 1* - Modified IC pinout and changed descriptions related to the removed pin. *Ordering Information on page 1* - Modified Ordering Information *Features on page 1* - Added and modified description. *Functional Table on page 2* - Added Functional Table *Functional Pin Description on page 4* - Modified IC pinout and changed descriptions related to the removed pin. *Absolute Maximum Ratings on page 7* - Modified IC pinout and changed descriptions related to the removed pin. *Recommended Operating Conditions on page 7* - Modified IC pinout and changed descriptions related to the removed pin. *Electrical Characteristics on page 8, 9, 10* - Modified IC pinout and deleted descriptions related to the - removed pin. - Modified the PWM accuracy specification. *Typical Application Circuit on page 11, 12* - Modified the BOM reference. *Typical Operating Characteristics on page 13, 14, 15, 16* - Added and modified the curves and waveforms. *Operation on page 19* - Updated Output Voltage Setting table.