RICHTEK®

RT4822

Wide Input and Ultra-Low Quiescent Current Boost Converter with High Efficiency and I²C Flexible Control

1 General Description

The RT4822 allows systems to take advantage of new battery chemistries that can supply significant energy when the battery voltage is lower than the required voltage for system power ICs. By combining built-in power transistors, synchronous rectification, and low supply current, this IC provides a compact solution for systems using advanced Li-Ion battery chemistries.

The RT4822 is a boost regulator designed to provide a minimum output voltage from a single-cell Li-Ion battery, even when the battery voltage is below the system's minimum requirement. In its boost mode, output voltage regulation is guaranteed up to a maximum load current of 1500mA. Additionally, its quiescent current in shutdown mode is less than 1μA, which significantly extends battery life. The regulator transitions smoothly between bypass and normal boost modes. The device can be forced into bypass mode to reduce quiescent current.

The RT4822 is available in the WL-CSP-9B 1.3x1.2 (BSC) package. The recommended junction temperature range is –40°C to 125°C, and the ambient temperature range is –40°C to 85°C.

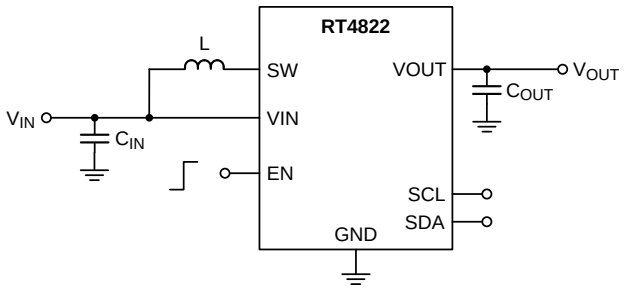
2 Applications

- NFC Device Power Supply
- USB Charging Ports
- PC Accessory Applications
- TWS (True Wireless Stereo) Hall Sensors
- Gaming Device Sensors

3 Features

- **Ultra-Low Operating Quiescent Current**
- **Quickly Start-Up Time (< 400μsec)**
- **Few External Components Required: 1μH Inductor, 0402 Case Size Input and 0603 Case Size Output Capacitors**
- **Input Voltage Range: 1.8V to 5.5V**
- **Programmable Output Voltage from 3.15V to 5.5V with 25mV/Step**
- **Support V_{IN} > V_{OUT} Operation**
- **Default Boost Output Voltage Setting: V_{OUT} = 5V**
- **Maximum Continuous Load Current: 1.5A at V_{IN} > 3.6V Boosting V_{OUT} to 5V**
- **Up to 93% Efficiency**
- **Internal Synchronous Rectifier**
- **Overcurrent Protection**
- **Cycle-by-Cycle Current Limit**
- **Undervoltage Protection**
- **Overvoltage Protection**
- **Short-Circuit Protection**
- **Over-Temperature Protection**
- **Small WL-CSP-9B 1.3x1.2 (BSC) Package**

4 Simplified Application Circuit



5 Ordering Information

RT4822 □

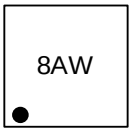
Package Type(1)

WSC: WL-CSP-9B 1.3x1.2 (BSC)

Note 1.

Richtek products are Richtek Green Policy compliant and marked with (1) indicates compatible with the current requirements of IPC/JEDEC J-STD-020.

6 Marking Information



8A: Product Code
W: Date Code

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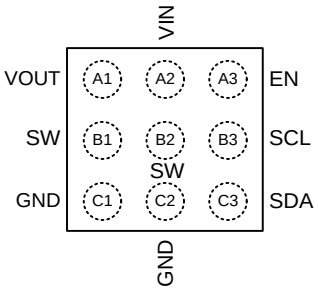
7 Pin Configuration

(TOP VIEW)

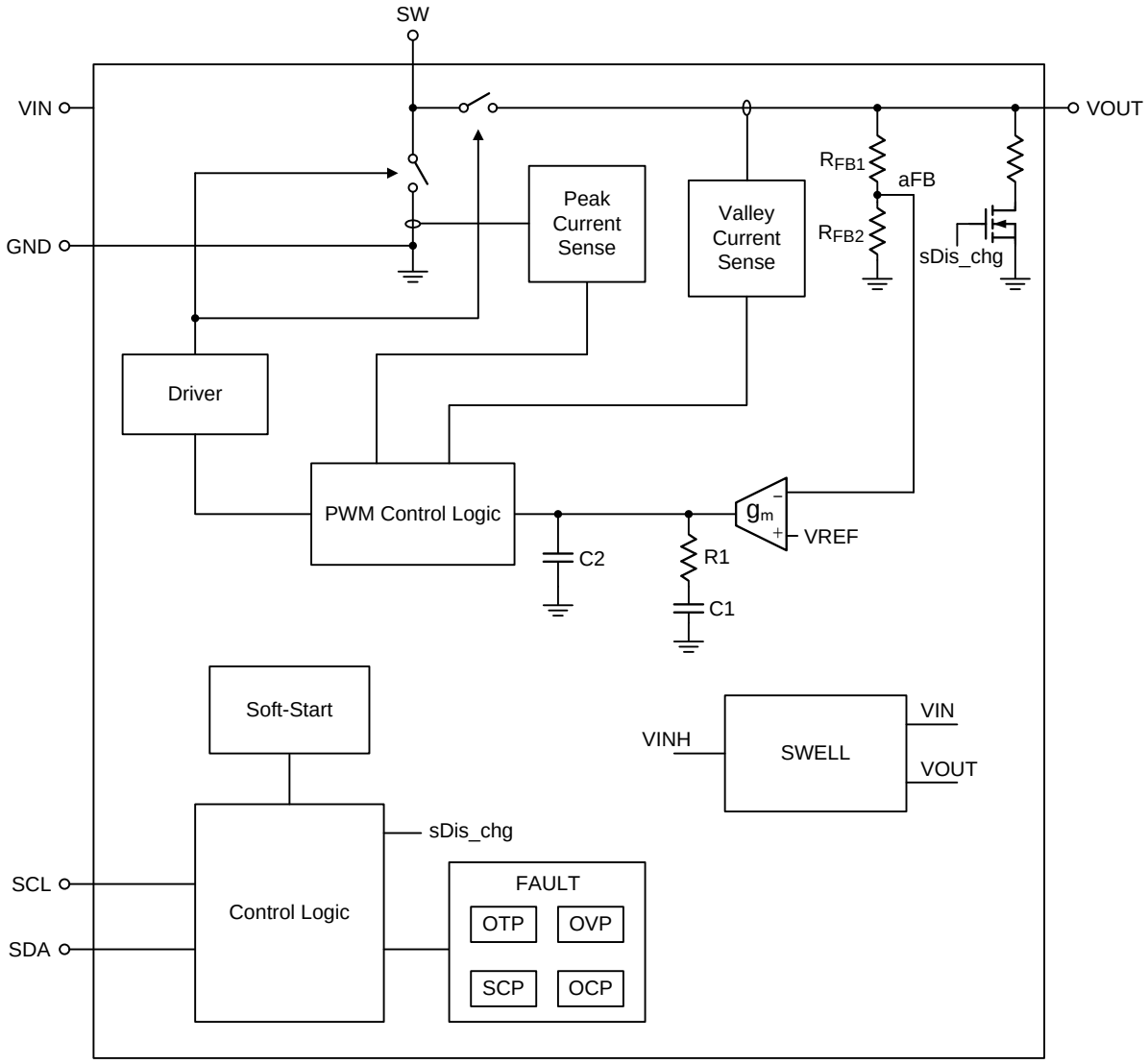


WL-CSP-9B 1.3x1.2 (BSC)

8 Functional Pin Description

Pin No.	Pin Name	Pin Function
A1	VOUT	Output voltage. Place C_{OUT} as close as possible to the device.
A2	VIN	Input voltage. This pin must be connected to input power source as it is used to supply the internal power of the device.
A3	EN	Enable. When this pin is set to high, the circuit is enabled. Do not leave this pin floating.
B1, B2	SW	Switching node. The power inductor should be connected between SW and power input.
B3	SCL	I^2C serial interface clock. This pin requires a pull-up resistor to the I^2C power supply.
C1, C2	GND	Ground. This is power and signal ground reference for the device. The bypass capacitor for C_{OUT} should be connected back to this pin using the shortest path possible to ensure optimal performance.
C3	SDA	I^2C serial interface data. This pin requires a pull-up resistor to the I^2C power supply.

9 Functional Block Diagram



10 Absolute Maximum Ratings

(Note 2)

- VIN, VOUT, SW, EN, SDA, SCL ---------- –0.3V to 6.5V
- Power Dissipation, P_D @ T_A = 25°C
- WL-CSP-9B 1.3x1.2 (BSC) ---------- 1.54W
- Package Thermal Resistance (Note 3)
- WL-CSP-9B 1.3x1.2 (BSC), θ_{JA} ---------- 64.9°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 4)

  HBM (Human Body Model) ---------- 2kV

Note 2. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 3. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-9 thermal measurement standard.

Note 4. Devices are ESD sensitive. Handling precautions are recommended.

11 Recommended Operating Conditions

(Note 5)

- Input Voltage Range (Boost Mode) ---------- 1.8V to 5.5V
- Input Voltage Range (Bypass Mode) ---------- 2.2V to 5.5V
- Output Voltage Range ---------- 3.15V to 5.5V
- Input Capacitor, CIN ---------- 4.7µF
- Output Capacitor, COUT ---------- 3.5µF to 50µF
- Inductance, L ---------- 0.7µH to 2.2µH
- Input Current (Average Current into SW) ---------- 1.8A
- Input Current (Peak Current into SW) ---------- 4A
- Ambient Temperature Range ---------- –40°C to 85°C
- Junction Temperature Range ---------- –40°C to 125°C

Note 5. The device is not guaranteed to function outside its operating conditions.

12 Electrical Characteristics

(V_{IN} = 3.6V, C_{IN} = 4.7μF, C_{OUT} = 10μF, L1 = 1μH. All typical (Typ) limits apply for T_A = 25°C, unless otherwise specified. All minimum (Min) and maximum (Max) apply over the full operating ambient temperature range (–40°C ≤ T_A ≤ 85°C).

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Supply						
VIN Supply Input Voltage	V_{IN}		1.8	--	5.5	V
Into VIN Operating Quiescent Current	I_{Q_NSW}	I_{OUT} = 0mA, V_{IN} = 3.6V, V_{OUT} = 5V, EN = GND	--	0.1	0.5	μA
Into VOUT Standby Mode Quiescent Current	$I_{Q\_NSW\_VOUT}$		--	4	6	μA
VIN Quiescent Current (Device Normal Switching)	I_{Q_SW}	V_{IN} = 3.6V, shutdown mode	--	--	1	μA
		V_{IN} = 3.6V, V_{OUT} = 5V, boost mode	--	6	--	
		V_{IN} = 3.6V, bypass mode	--	16	25	
Power-On Reset	V_{POR}		1.2	1.5	--	V
Enable						
Input Voltage Logic-Low	V_{IL}		--	--	0.4	V
Input Voltage Logic-High	V_{IH}		1.2	--	--	V
Logic Input Leakage Current	I_{ILK}	Input connected to GND or VIN	--	--	0.5	μA
Output						
Regulated DC Output Voltage	V_{OUT_REG}	1.8V ≤ V_{IN} ≤ 4.8V, V_{OUT} = 5V, I_{OUT} = 0mA, PFM operation	5.04	5.06	5.08	V
		V_{IN} = 3.6V, I_{OUT} = 1A, V_{OUT} = 5V, PWM operation	4.95	5	5.05	
Output Ripple Performance	V_{OUT_Ripple}	V_{IN} = 3.6V, V_{OUT} = 5V, C_{OUT} = 10μF, I_{OUT} = 0A to 1A	--	60	120	mV
Output Discharge Resistor	R_{DISCH}	V_{IN} = 3.6V	--	100	--	Ω
Power Switch						
On-Resistance of High-Side MOSFET	R_{DSON_H}		--	80	--	mΩ
On-Resistance of Low-Side MOSFET	R_{DSON_L}		--	80	--	mΩ
Minimum On-Time	t_{ON_MIN}	V_{IN} = 1.8V to 4.8V, V_{OUT} = 5V	20	--	60	ns
Maximum Duty Cycle	D_{MAX}	V_{IN} = 1.8V, V_{OUT} = 5.5V, I_L = 400mA	68.8	--	--	%
Positive Inductor Valley Current Limit (V_{IN} or V_{OUT} > 2.2V)	I_{LIM_VALLEY}	Register 0x00[4:3] = 01	--	850	--	mA
		Register 0x00[4:3] = 10	--	2150	--	
		Register 0x00[4:3] = 11	--	3620	--	
Pass-Through Current Limit	I_{LIM_PASS}	The setting is the same as pre-charge current limit.	250	300	350	mA
Negative Inductor Peak Current Limit	$I_{LIM\_PEAK\_NEG}$		–3	–2	–1	A

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Oscillator						
Oscillator Frequency	f_{OSC}	V_{IN} = 3.6V, V_{OUT} = 5V, I_{OUT} = 200mA to 1A	3	3.5	4	MHz
		V_{IN} < 2.5V → start to reduce frequency	2	--	--	
Soft-Start						
Start-Up Time	t_{START_BST}	V_{IN} = 3.6V, V_{OUT} = 5V, I_{OUT} = 0mA. Time from active EN to VOUT	100	400	500	μs
Pre-Charge Current Limit	I_{LIM_PRECHG}	Register 0x00[7:6] = 00	100	150	200	mA
		Register 0x00[7:6] = 01	250	300	350	
		Register 0x00[7:6] = 10	500	600	700	
		Register 0x00[7:6] = 11	1000	1200	1400	
Protection						
Undervoltage Protection Threshold	V_{UVP}	V_{UVP} = 80% x V_{OUT}	--	80	--	%
Overvoltage Protection Threshold	V_{OVP}	V_{IN} = 3.6V	--	6	--	V
Short-Circuit Protection Threshold	V_{SCP}		0.3	0.5	0.7	V
Hiccup On-Time	t_{ON_HICCUP}	V_{IN} = 2.2V to 5.5V	1.7	2	2.3	ms
Hiccup Off-Time	t_{OFF_HICCUP}	V_{IN} = 2.2V to 5.5V	18	20	22	ms
Over-Temperature Protection Threshold	T_{OTP}		140	150	160	°C
Over-Temperature Protection Hysteresis	T_{OTP_HYS}		--	20	--	°C
Overcurrent Protection Threshold	I_{OCP_5A}	V_{IN} = 5V	4	5	5.5	A
Efficiency						
Efficiency	η	V_{OUT} = 5V, V_{IN} = 3.6V, Load = 10μA	--	72	--	%
		V_{OUT} = 5V, V_{IN} = 3.6V, Load = 10mA	--	90	--	
		V_{OUT} = 5V, V_{IN} = 3.6V, Load = 600mA	--	93	--	
		V_{OUT} = 5V, V_{IN} = 3.6V, Load = 1000mA	--	91	--	

12.1 I^2C Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
SCL, SDA Low-Level Input Threshold Voltage	V_{IL_I2C}		--	--	0.4	V
SCL, SDA High-Level Input Threshold Voltage	V_{IH_I2C}		--	1.8	--	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
SDA Output Low Sink Current	I_{OL_I2C}		−10	--	10	μA
Data Set-Up Time	t_{DSU_I2C}		70	--	--	ns
SCL Clock Frequency	f_{SCL}	Standard mode	--	--	100	kHz
		Fast mode	--	--	400	
		Fast mode plus	--	--	1000	
Bus Free Time between Stop and Start	t_{BUF}	Standard mode	4.7	--	--	μs
		Fast mode	1.3	--	--	
		Fast mode plus	0.5	--	--	
(Repeated) Start Hold Time	$t_{HD;STA}$	Standard mode	4.7	--	--	μs
		Fast mode	0.6	--	--	
		Fast mode plus	0.26	--	--	
(Repeated) Start Setup Time	$t_{SU;STA}$	Standard mode	4.7	--	--	μs
		Fast mode	0.6	--	--	
		Fast mode plus	0.26	--	--	
SDA Data Hold Time	$t_{HD;DAT}$	Standard mode	0.1	--	--	ns
		Fast mode	0.1	--	--	
		Fast mode plus	0.1	--	--	
STOP Condition Setup Time	$t_{SU;;STO}$	Standard mode	4	--	--	μs
		Fast mode	0.6	--	--	
		Fast mode plus	0.26	--	--	
SDA Valid Acknowledge Time	$t_{VD;ACK}$	Standard mode	--	--	3.45	μs
		Fast mode	--	--	0.9	
		Fast mode plus	--	--	0.45	
SDA Setup Time	$t_{SU;DAT}$	Standard mode	250	--	--	ns
		Fast mode	100	--	--	
		Fast mode plus	50	--	--	
SCL Clock Low Period	t_{LOW}	Standard mode	4.7	--	--	μs
		Fast mode	1.3	--	--	
		Fast mode plus	0.5	--	--	
SCL Clock High Period	t_{HIGH}	Standard mode	4	--	--	μs
		Fast mode	0.6	--	--	
		Fast mode plus	0.26	--	--	

13 Typical Application Circuit

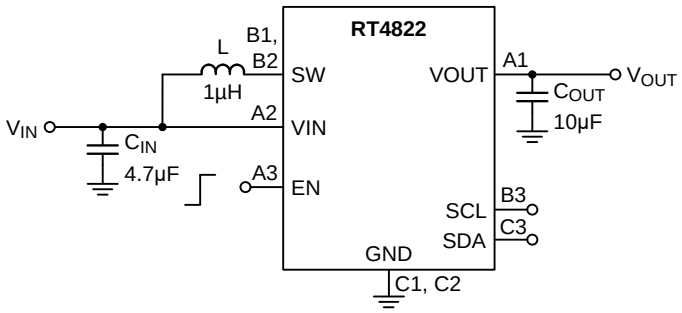
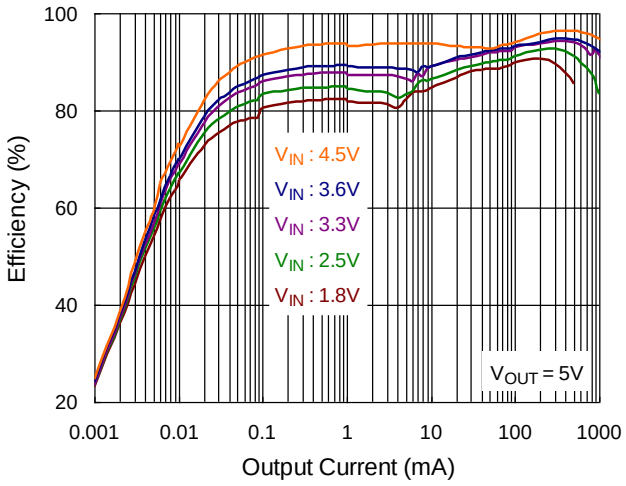


Table 3. Recommended Components Information

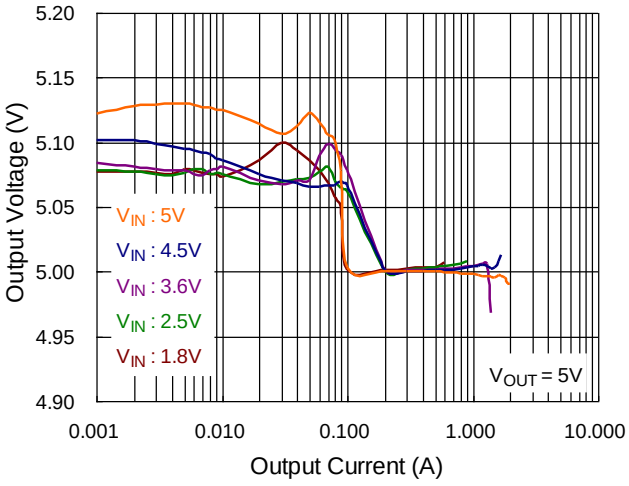
Reference	Part Number	Description	Package	Manufacturer
CIN	GRM155R60J475ME47D	4.7µF/6.3V/X5R	0402	Murata
COUT	GRM188R60J106ME47D	10µF/6.3V/X5R	0603	Murata
L	DFE252012F-1R0M=P2	1.0µH/3.3A	2.5x2.0x1.2mm	Murata

14 Typical Operating Characteristics

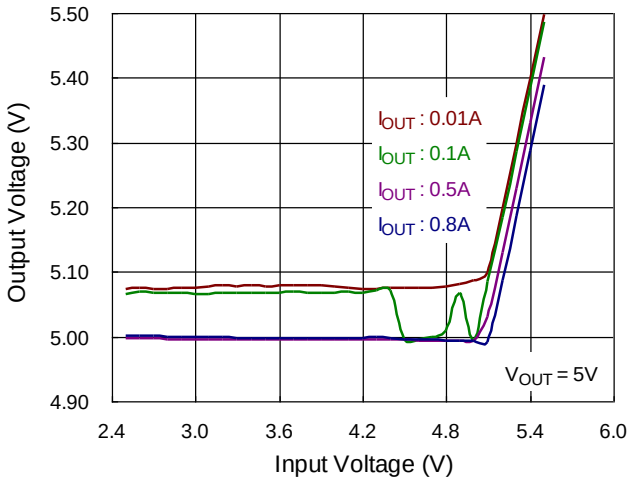
Efficiency vs. Output Current



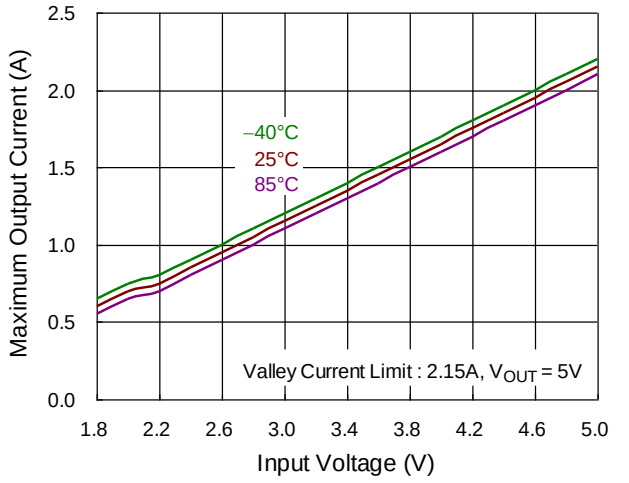
Boost Load Regulation



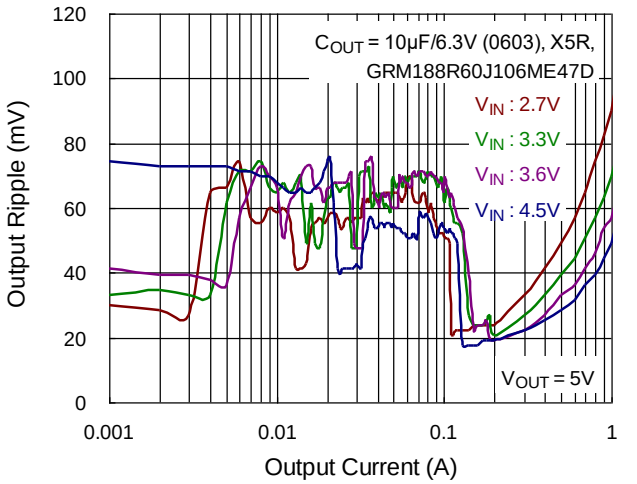
Boost Line Regulation



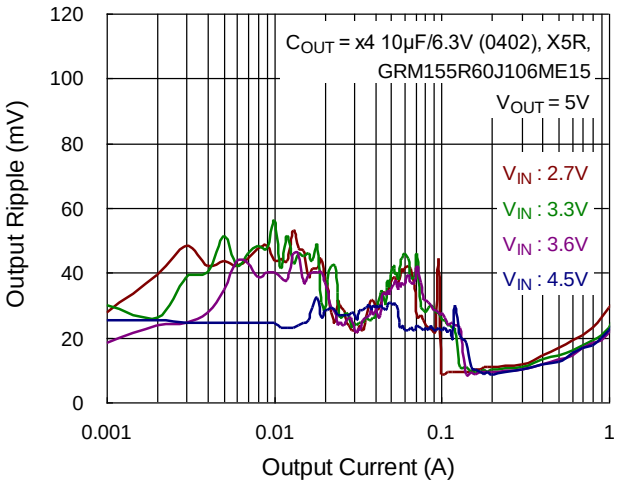
Maximum Output Current vs. Input Voltage



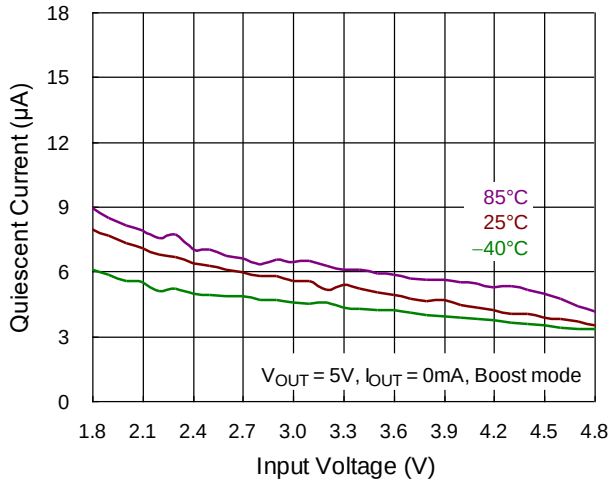
Output Ripple vs. Output Current



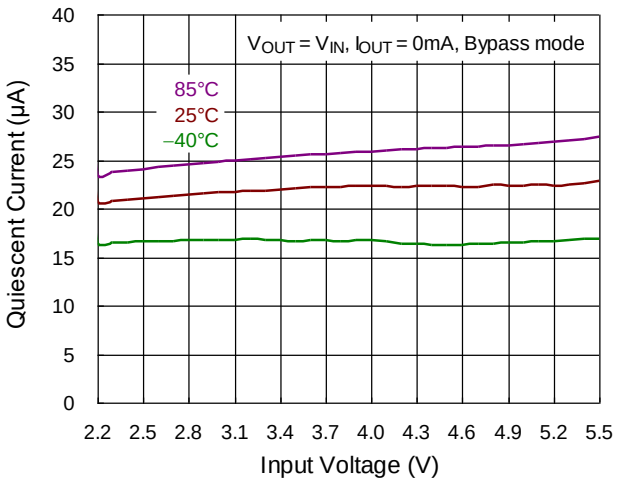
Output Ripple vs. Output Current



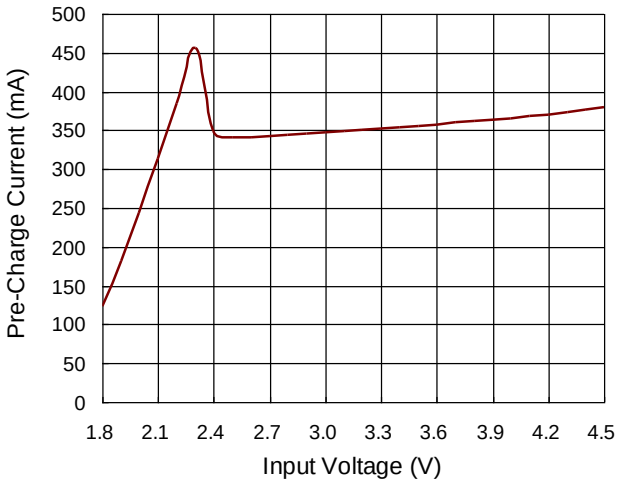
Quiescent Current vs. Input Voltage



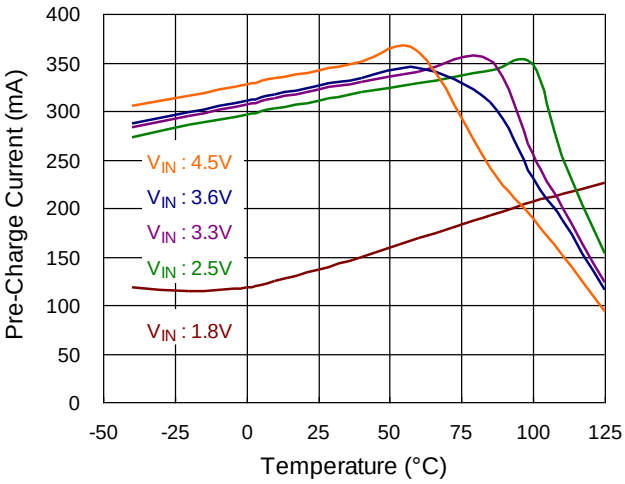
Quiescent Current vs. Input Voltage



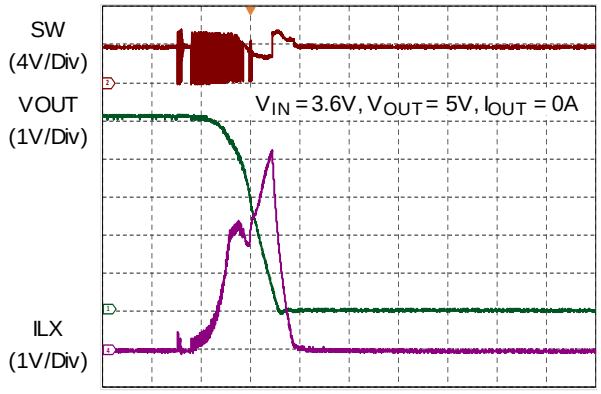
Pre-Charge Current vs. Input Voltage



Pre-Charge Current vs. Temperature

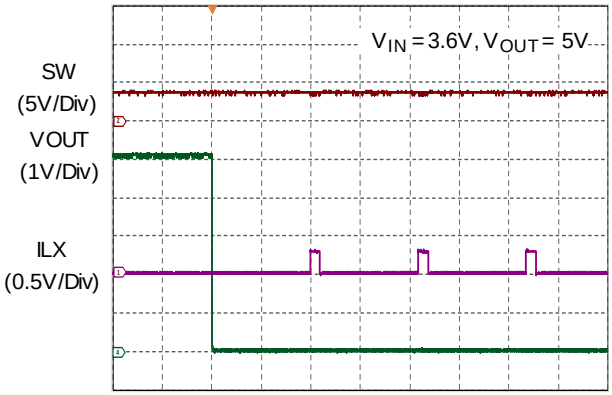


Boost Short Circuit



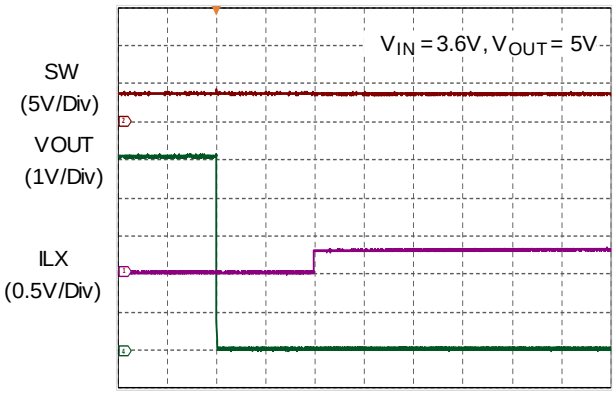
Time (0.01ms/Div)

Boost Short Circuit with Hiccup Mode

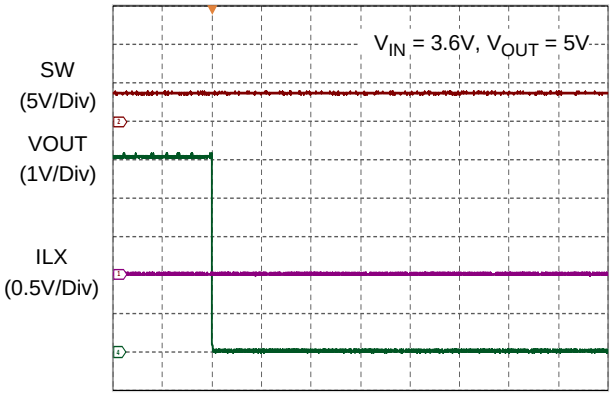


Time (10ms/Div)

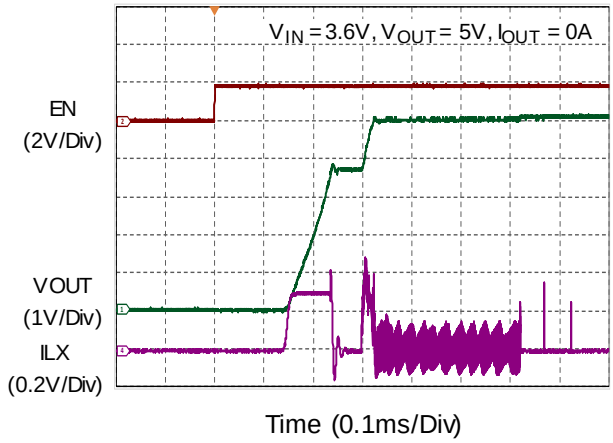
Boost Short Circuit with Linear Mode



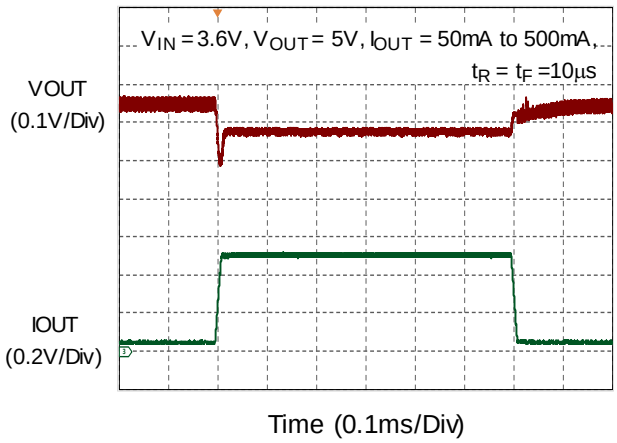
Boost Short Circuit with Latch-Off Mode



Power-On



Load Transient



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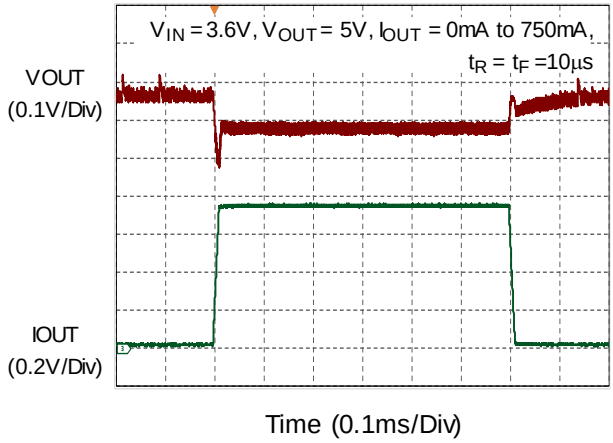

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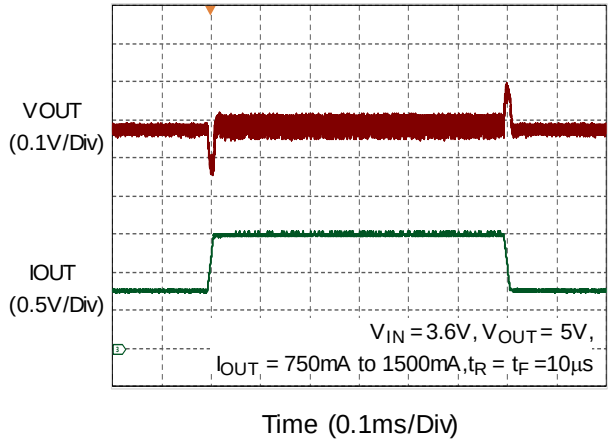
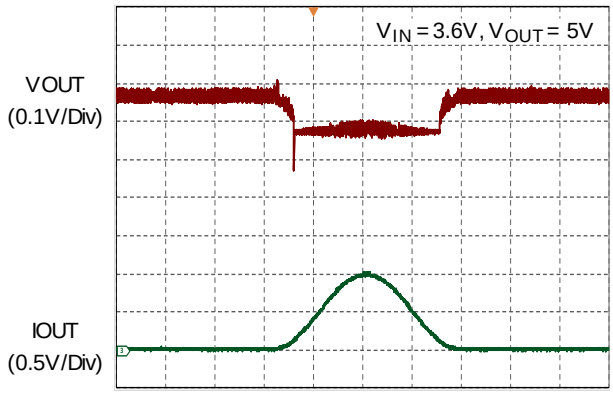
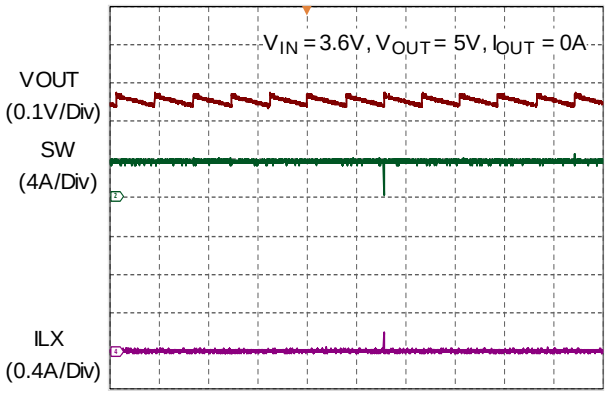


Sine Waveform Stability



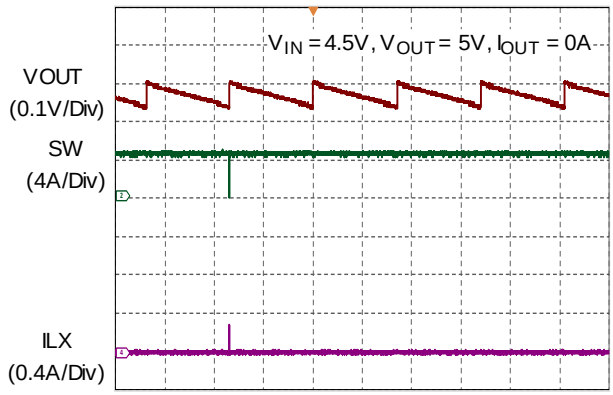
Time (5ms/Div)

PFM Output Ripple



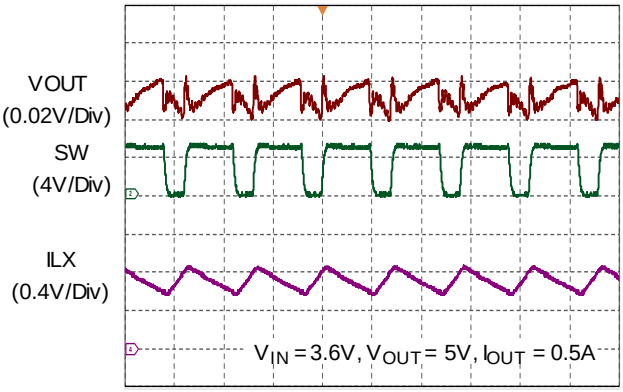
Time (20ms/Div)

PFM Output Ripple



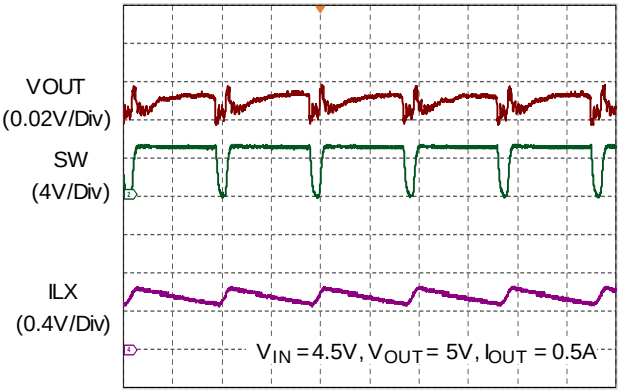
Time (20ms/Div)

PWM Output Ripple



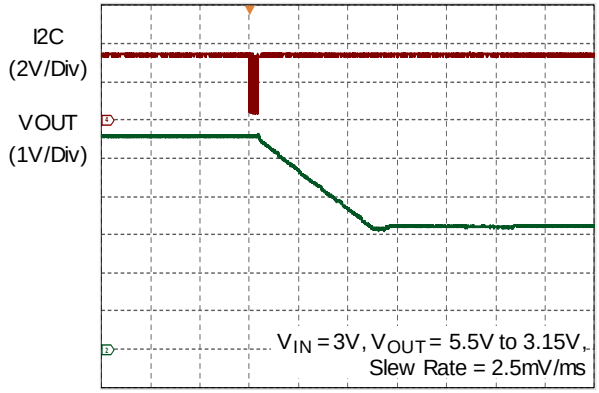
Time (0.0002ms/Div)

PWM Output Ripple



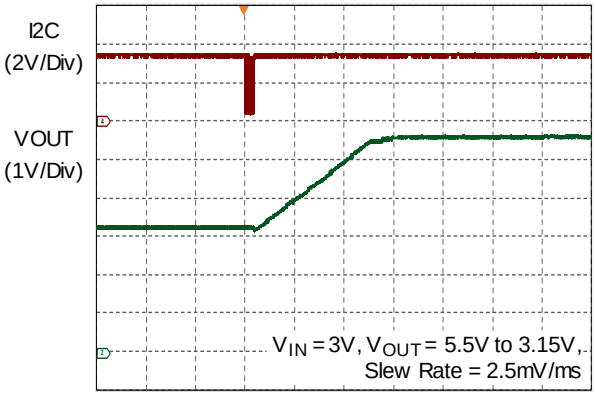
Time (0.0002ms/Div)

DVS Down



Time (0.4ms/Div)

DVS Up



15 Operation

The RT4822 integrates built-in power transistors, synchronous rectification, and low supply current to offer a compact and efficient solution for systems powered by advanced Li-Ion battery chemistries.

In boost mode, the RT4822 ensures stable output voltage regulation up to a maximum load current of 1.5A. Additionally, its quiescent current in shutdown mode is less than 1μA, which significantly extends battery life.

15.1 Start-Up Sequence and Considerations

When the input voltage falls below the POR threshold, both the internal digital and analog circuit of the RT4822 are disabled. Conversely, when the input voltage exceeds the POR threshold, the behavior of the boost converter is as follows:

1. The internal digital circuit of the IC is activated.
2. After turning on the EN pin, the internal registers start to load the default values from eFuse.
3. The boost converter enters free-running mode (detail in free-running mode section).
4. If V_{OUT} > 2.2V (or V_{IN} > 2.2V), the boost converter switched to close loop control.

Figure 1 and Figure 2 show eFuse download diagram and the corresponding flow chart. When input voltage is above the POR threshold and EN is set high, the eFuse starts to load into the digital circuit. The deglitch time ranges from 3μs to 15μs (maximum), and the eFuse download time spans from 16μs to 24μs (maximum). During the eFuse data download process, the RT4822's internal circuit ensures the completion of download progress, unless VIN falls below the POR threshold.

It is recommended to set the deglitch time between the POR and EN rising edge to 1ms. This duration helps to prevent VIN signal bouncing when the power is plugged in.

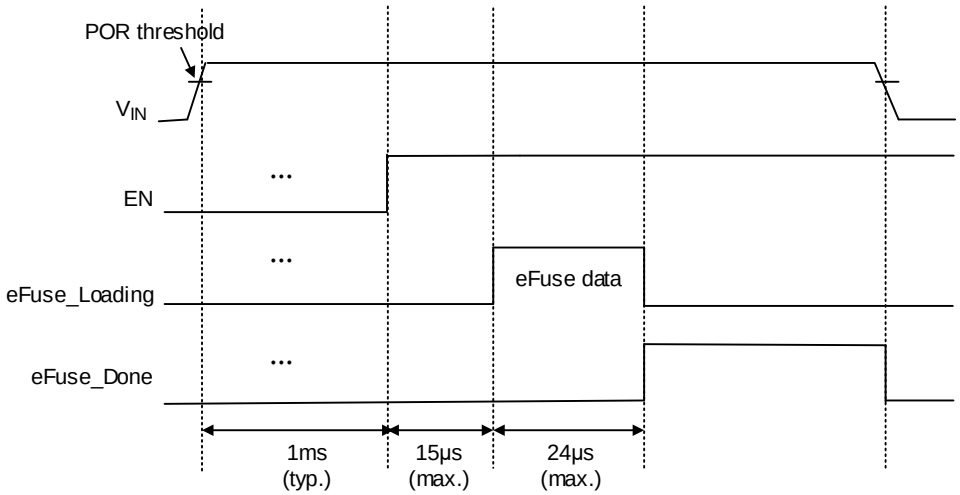


Figure 1. eFuse Download Timing Diagram

15.2 Free-Running Mode

When both the V_{IN} voltage and the V_{OUT} voltage fall below 2.2V, the boost converter enters free-running mode. In this mode, the converter operates at a switching frequency of 1.5MHz and the duty cycle is set to 25%. This mode serves as a transition phase during the power-on stage, featuring an implemented current limit function to facilitate a smooth soft-start for the converter. The current limit level is designed to be lower than 900mA.

15.3 Mode Control

It is used to select the mode. As shown in Table 1 (set 0x05[0] to 0), there are four device states. When both BOOST_EN is '0' and BOOST_BP is '1', it enters forced bypass mode with low quiescent mode (20μA). When both BOOST_EN and BOOST_BP are '0', it is shutdown mode and the quiescent current is less than 1μA. It works in forced bypass without low quiescent mode. When BOOST_EN is '1', the RT4822 operates in boost and auto bypass mode. There should be a delay time (< 400μs) from when BOOST_EN is set to '1' to when power is ready to guarantee normal operation.

Table 1. Pin Configuration for Converter

0x05[5] BOOST_EN	0x05[4] BOOST_BP	Mode Define	Device State
0	0	Shutdown mode	The device is shutdown. The device shutdown current is approximately about 1μA (maximum).
0	1	Bypass mode	The device operates in forced bypass with low quiescent mode, featuring a low quiescent current down to about 16μA (typical).
1	Do not care	Boost mode	The device is active in forced bypass without low quiescent mode. The device supply current is approximately about 6μA (typical).

15.4 Enable

The boost can be enabled or disabled by the EN pin and the register (0x05[5]) BOOST_EN bit. When the EN pin is higher than the threshold of logic-high, the device starts operating according to the operation diagram in Figure 2. In shutdown mode, the converter stops switching, and the internal control circuit is turned off. The output voltage beings to discharge due to component consumption (e.g., capacitor ESR) and the internal discharge circuit (register 0x05[2:1]).

15.5 Soft-Start State

During soft-start state, when VOUT reaches 99% of V_{OUT_Target}., the RT4822 enters boost operation. When the system powers on with heavy loading (higher than pre-charge current), the RT4822 remains in pre-charge state until load is reduced.

15.6 Boost/Auto Bypass Mode

There are two normal operation modes: boost mode and auto bypass mode. In boost mode (when V_{IN} – 0.3V < V_{OUT_Target}), the converter boosts output voltage to V_{OUT_Target}, and delivers power to load through internal synchronous switches after the soft-start state. In auto bypass mode (when V_{IN} – 0.3V ≥ V_{OUT_Target}), the input voltage is delivered directly to the output terminal and the load. This allows for the maximum current capacity with the RT4822. Details of the information are provided below.

15.7 Boost Mode (Auto PFM/PWM Control Method)

To save power and improve efficiency at low loads, the boost operates in PFM (Pulse Frequency Modulation) mode as the inductor transitions into DCM (Discontinuous Current Mode). The switching frequency adjusts in proportion to the load to maintain output voltage regulation. As the load increases and the inductor current shifts into continuous current mode, the boost automatically switches to PWM mode.

Table 2. The RT4822 Start-Up Description

Mode	Description	Condition
LIN	Linear startup	V_{IN} - 200mV ≥ V_{OUT}
Soft-Start	Boost soft-start	0.99 x V_{OUT_Target} > V_{OUT} ≥ V_{IN} - 200mV
Boost	Boost mode	V_{OUT_Target} ≥ 0.99 x V_{OUT_Target}
If V_{IN} exceeds V_{OUT}		
Auto Bypass	Auto bypass mode	V_{IN} ≥ V_{OUT} The control loop automatically transfers between auto bypass mode and boost mode.

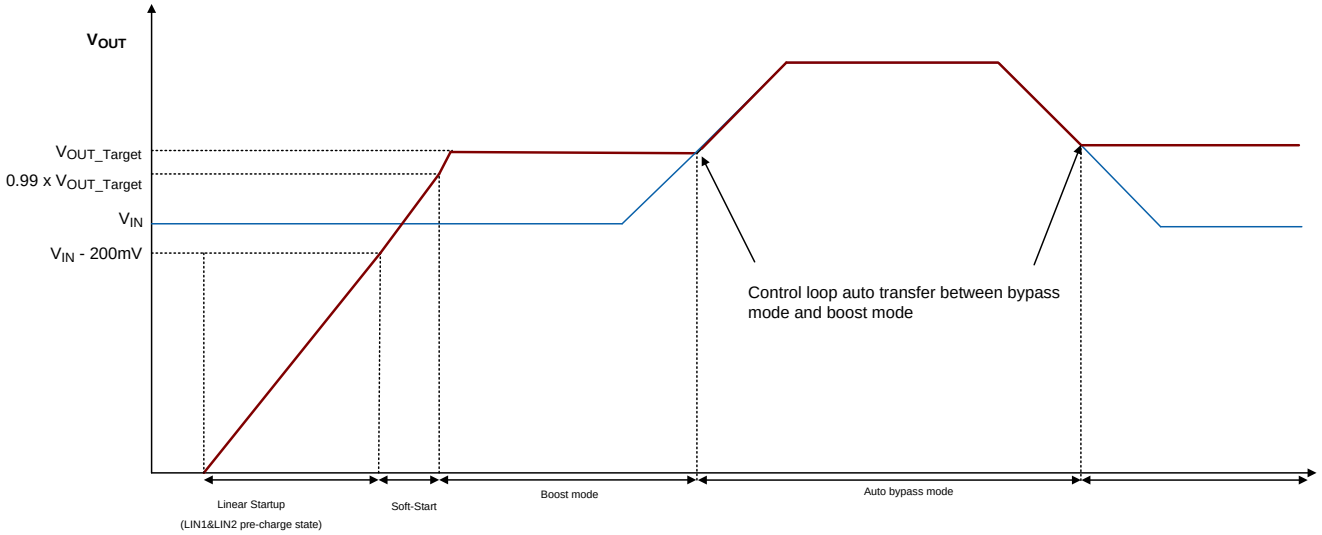


Figure 2. V_{OUT} Mode Transition Diagram with EN L to H and V_{IN} Variation (I_{OUT} = 0A)

15.8 Protection

The RT4822 features several protections, which are listed in the table below. The table describes the behavior of each protection feature.

Protection Type	Fault Event Trigger	Fault Deglitch Time	Protection Method	Fault Protection Latch Time	Reset Method
OCP_IL5A	I_{L_PEAK} > 5A	No delay	Turn off UG, LG	20ms, Auto-recovery	I_{L_PEAK} < 5A
OCP	I_{L_VALLEY} > 3.6A	No delay	Stop LG switching	N/A	I_{L_VALLEY} < 3.3A
OVP	V_{OUT} > 6V	100ns	Turn off UG, LG	N/A	V_{OUT} < 6V
SCP	V_{OUT} < 0.7V	No delay	Turn off UG, LG	20ms, Auto-recovery	V_{OUT} > 0.7V
OTP	TEMP > 150°C	170µs	Turn off UG, LG	Turn off UG, LG	TEMP < 130°C
SCP_SS	V_{IN} - V_{OUT} > 0.2V	2ms	UG OCP = 0.3A	N/A	V_{IN} - V_{OUT} < 0.2V
OCP_BYP	I_L > 0.3A	2ms	Turn off UG	20ms, Auto-recovery	I_L < 0.3A
SCP_BYP	V_{IN} - V_{OUT} > 0.7V	No delay	Turn off UG, LG	20ms, Auto-recovery	V_{IN} - V_{OUT} < 0.7V

16 Application Information

(Note 6)

16.1 Start-Up

The RT4822 can be powered via the EN pin or the internal register 0x05[5]. When 0x05[0] is set to '1', the RT4822 is activated by the EN pin; otherwise, it is activated by 0x05[5].

The following steps must be followed for startup:

1. The input voltage (VIN) is configured within the recommended operating range.
2. Reset and initialize the digital circuit by setting 0x05[3] to 1 (RESET).
3. Set the output voltage (VOUT) using 0x02 (BOOST_VOUT).
4. Enable the boost converter using the EN pin or internal register 0x05[5].

16.2 Power-Off

When the RT4822 is turned off, the device enters a shutdown state. In this mode, the converter stops its switching operation, the internal control circuitry is deactivated, and the load is disconnected from the input. As a result, the output voltage may decrease below the input voltage while in shutdown.

The RT4822 incorporates a discharge function, which can be enabled via register 0x05[1]. As a result, the output voltage may drop rapidly when the RT4822 is powered off.

16.3 Enable

The device can be enabled or disabled by the EN pin. When the EN pin is higher than the threshold of logic-high, the device starts operating with soft-start. Once the EN pin is set at low, the device will be shut down. In shutdown mode, the converter stops switching, internal control circuitry is turned off, and the load is disconnected from the input. This also means that the output voltage can drop below the input voltage during shutdown.

16.4 Power Frequency Modulation

The Power Frequency Modulation (PFM) is used to improve efficiency at light load. When the output voltage is lower than a set threshold voltage, the converter will operate in PFM. It raises the output voltage with several pulses until the loop exits PFM.

16.5 Thermal Shutdown

The device has a built-in temperature sensor which monitors the internal junction temperature. If the temperature exceeds the threshold, the device stops operating. As soon as the IC temperature decreases below the threshold with a hysteresis, it starts operating again. The built-in hysteresis is designed to avoid unstable operation at IC temperatures near the over-temperature threshold.

16.6 Inductor Selection

The primary concern of inductor selection is the maximum loading of the application. The example is given by the application condition and equations below.

Application condition:

V_{IN} = 3.6V, V_{OUT} = 5V, I_{OUT} = 1.3A, converter efficiency = 90.2%, frequency = 3.5MHz, L = 1μH.

Step 1: Calculate the input current (I_{IN}).

$$I_{IN} = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times Eff} = 2.001A$$

Step 2: Calculate the duty cycle of the boost converter.

$$D = 1 - \frac{V_{IN}}{V_{OUT}} = 0.28$$

Step 3: Calculate the peak current of the inductor.

$$I_{L(Peak)} = I_{IN} + 0.5 \times \frac{V_{IN} \times D}{L \times Freq.} = 2.145A$$

The recommended nominal inductance value is 1μH. It is recommended to use an inductor with a DC saturation current ≥ 2200mA.

16.7 Input Capacitor Selection

At least an input capacitor of 4.7μF and the rate voltage of 6.3V for DC bias is recommended to improve transient behavior of the regulator and EMI behavior of the total power supply circuit for SW. And input capacitor placed as close as possible to the VIN and GND pins of the IC is recommended.

16.8 Output Capacitor Selection

At least a 10μF capacitors is recommended to improve V_{OUT} ripple.

Output voltage ripple is inversely proportional to C_{OUT}.

Output capacitor is selected according to output ripple which is calculated as:

$$V_{RIPPLE(P-P)} = t_{ON} \times \frac{I_{LOAD}}{C_{OUT}}$$

and

$$t_{ON} = t_{SW} \times D = t_{SW} \times \left(1 - \frac{V_{IN}}{V_{OUT}}\right)$$

therefore :

$$C_{OUT} = t_{SW} \times \left(1 - \frac{V_{IN}}{V_{OUT}}\right) \times \frac{I_{LOAD}}{V_{RIPPLE(P-P)}}$$

and

$$t_{SW} = \frac{1}{f_{SW}}$$

The maximum V_{RIPPLE} occurs at minimum input voltage and maximum output load.

16.9 Boost Converter Sleeping Mode Operation

The PFM mode and PWM mode are implemented in the RT4822. The PFM mode is designed for power-saving operation when the system operates at light load.

There is a mode transition between PFM and PWM modes. When system loading increases, the operating mode transitions from PFM mode to PWM mode. Note that within this small loading current range, the mode change causes output ripple to increase.

16.10 Current Limit

The RT4822 employs a valley-current limit detection scheme to sense inductor current during the off-time. When the loading current is increased such that the loading is above the valley current-limit threshold, the off-time is increased until the current is decreased to valley-current threshold. Next on-time begins after current is decreased to valley-current threshold. On-time is decided by (V_{OUT} – V_{IN}) / V_{OUT} ratio. The output voltage decreases when further loading current increases. The current limit function is implemented by the scheme, refer to Figure 3.

16.11 OCP (I_{OCP_5A}) Shutdown Protection

The RT4822 implements OCP shutdown protection. When the converter operates in boost mode, peak current limit and valley current limit function cannot protect the IC from short circuit or the huge loading. The RT4822 implements truth disconnection function. When peak current is > 5A (typical), the boost converter will turn off high-side MOSFET (UG) and low-side MOSFET (LG).

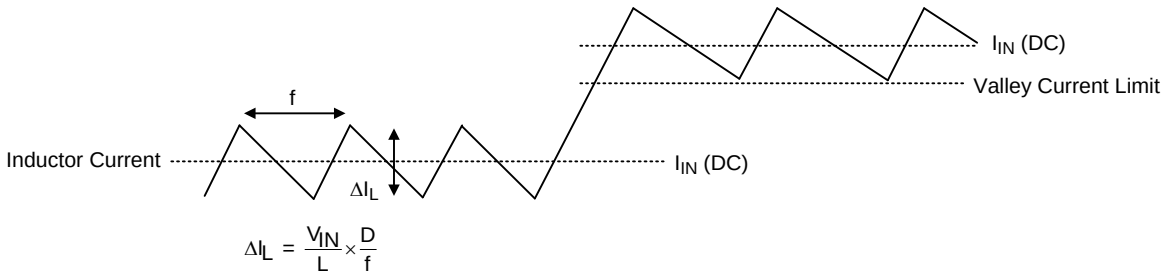


Figure 3. Inductor Currents in Current Limit Operation

16.12 Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula:

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a WL-CSP-9B 1.3x1.2 (BSC) package, the thermal resistance, θ_{JA}, is 64.9°C/W on a standard JEDEC 51-9 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below:

$P_{D(MAX)}$ = (125°C - 25°C) / (64.9°C/W) = 1.54W for a WL-CSP-9B 1.3x1.2 (BSC) package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curve in Figure 4 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

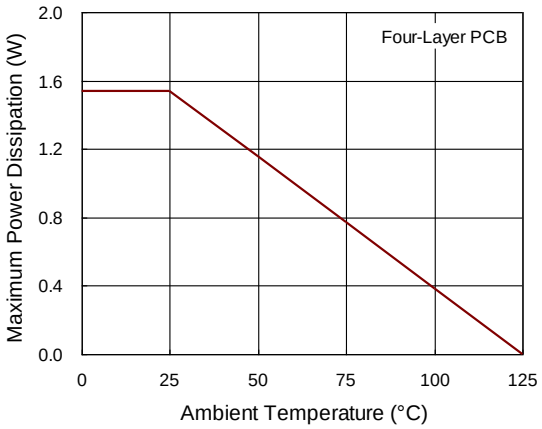


Figure 4. Derating Curve of Maximum Power Dissipation

16.13 Layout Considerations

The PCB layout is an important step to maintain the high performance of the RT4822.

Both the high current and the fast switching nodes demand full attention in the PCB layout to save the robustness of the RT4822. Improper layout might show the symptoms of poor line or load regulation, ground and output voltage shifts, stability issues, unsatisfying EMI behavior or worsened efficiency. For the best performance of the RT4822, the following PCB layout guidelines must be strictly followed.

- Place the input and output capacitors as close as possible to the input and output pins respectively for good filtering.
- For thermal consideration, it is needed to maximize the pure area for power stage area besides the SW.

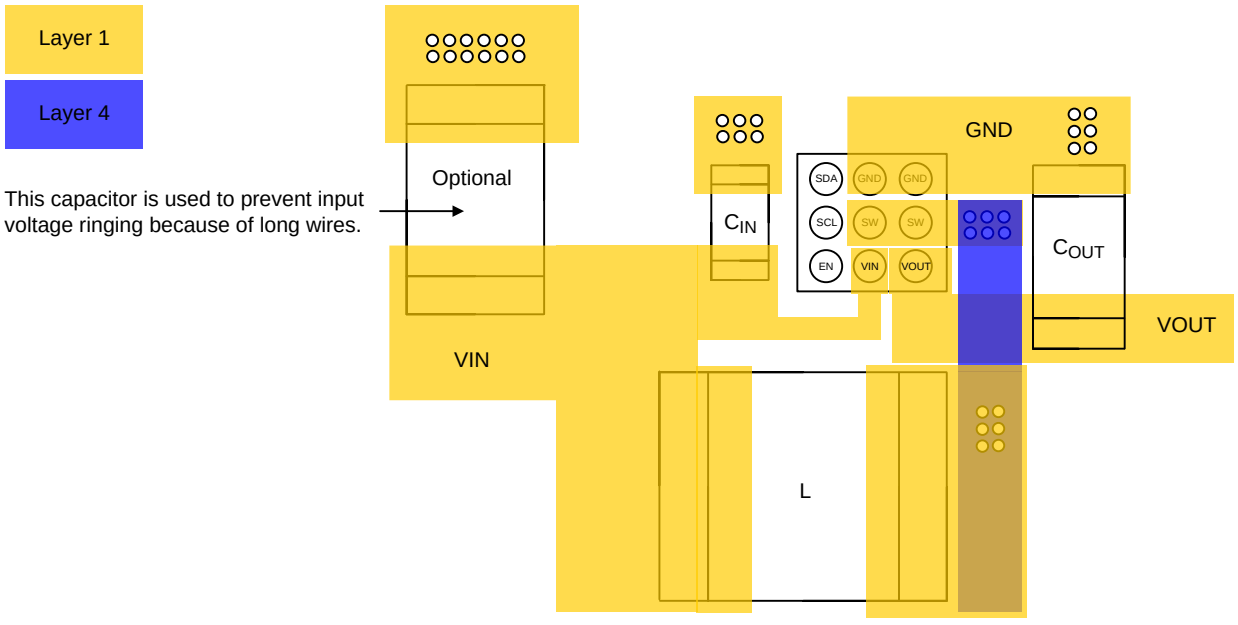


Figure 5. PCB Layout Guide

Note 6. The information provided in this section is for reference only. The customer is solely responsible for designing, validating, and testing any applications incorporating Richtek's product(s). The customer is also responsible for applicable standards and any safety, security, or other requirements.

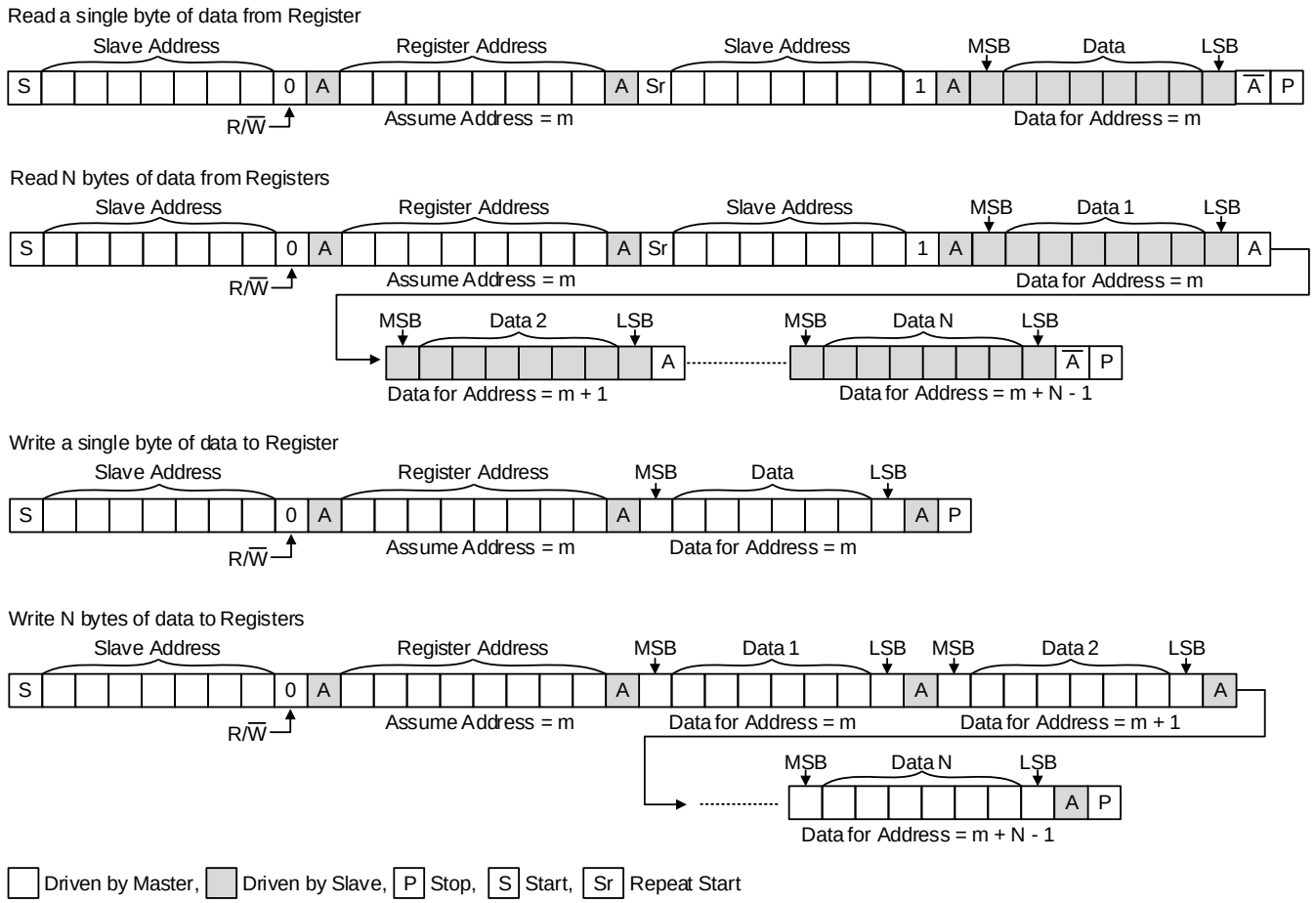
17 Functional Register Description

17.1 I²C Interface

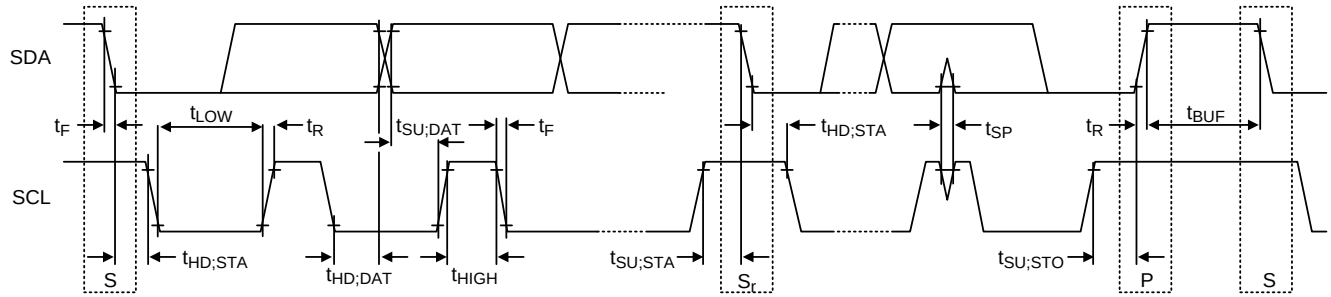
The following table shows the unique address of the RT4822.

RT4822 I²C Slave Address			
MSB	**LSB**	**R/W bit**	**R/W**
111010	1	1/0	EB/EA

The I²C interface bus must be connected to a 2.2kΩ resistor to the power node and independently connected to the processor. The I²C timing diagrams are listed below.



17.2 I²C Waveform Information



17.3 I²C Register Table

R: Read only.

R/C: Read then Clear.

R/W: Read and Write.

W/C: Write '1' then clear to '0' after this procedure finishes.

Addr	Reg Name	Bit	Bit Name	Default	Type	Description
0x00	BOOST_ REG1	7:6	IPCHG	01	R/W	Boost linear charge current. 00: 0.15A 01: 0.3A (default) 10: 0.6A 11: 1.2A
		5	BOOST_ MODE	0	R/W	Boost operation mode. 0: Auto mode (default) 1: FPWM mode
		4:3	BOOST_ ILIM	10	R/W	Boost current limit set bit. 00: Reserved (0.85A) 01: 0.85A 10: 2.15A (default) 11: 3.62A
		2:0	Reserved	000	R/W	Reserved

Addr	Reg Name	Bit	Bit Name	Default	Type	Description
0x01	BOOST_ REG2	7:6	SW_SR	00	RW	Boost SW switching slew. 00: 3V/ns (default) 01: 4V/ns 10: 6V/ns 11: 8V/ns
		5:4	SCP	10	RW	Short circuit protection. 00: Latch-off mode 01: Hiccup mode 10: Linear mode (default) 11: Reserved
		3:0	Reserved	0000	RW	Reserved

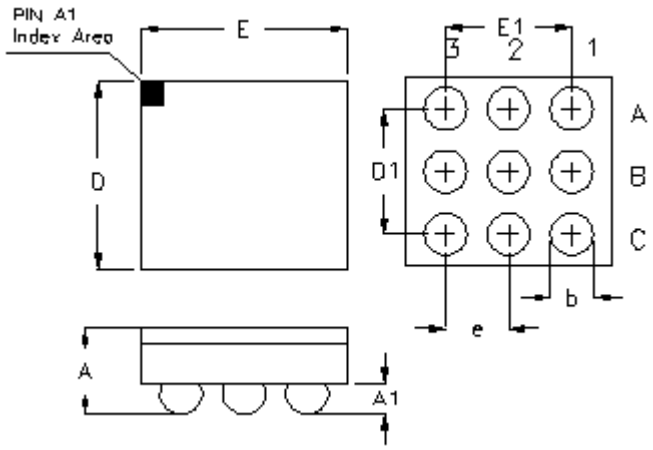
Addr	Reg Name	Bit	Bit Name	Default	Type	Description
0x02	BOOST_VOUT	7	Reserved	0	RW	Reserved
		6:0	BOOST_VOUT	1101011	RW	Boost output voltage can be set from 3.15V to 5.5V with 25mV/step. 0000000 to 0100001: 3.15V … 1101011: 5V (default) … 1111111: 5.5V

Addr	Reg Name	Bit	Bit Name	Default	Type	Description
0x03	BOOST_STATUS	7	BOOST_OV_STAT	0	R/C	Boost overvoltage threshold sense status. 0: No fault occurs 1: Fault occurs
		6	BOOST_UV_STAT	0	R/C	Boost undervoltage threshold sense status. 0: No fault occurs 1: Fault occurs
		5	BOOST_OTP	0	R/C	Boost over-temperature threshold sense status. 0: No fault occurs 1: Fault occurs
		4	Reserved	0	R/C	Reserved
		3	BOOST_OCP	0	R/C	Boost overcurrent threshold sense status. 0: No fault occurs 1: Fault occurs
		2	BOOST_FAULT	0	R/C	1 = sFAULT occurs 0: No fault occurs 1: Fault occurs
		1	POWER_GOOD	0	R	1 = sSSEND occurs 0: No fault occurs 1: Fault occurs
		0	Reserved	0	R	Reserved

Addr	Reg Name	Bit	Bit Name	Default	Type	Description
0x04	Reserved	7:0	Reserved	0000000	R	Reserved

Addr	Reg Name	Bit	Bit Name	Default	Type	Description
0x05	BOOST_ SETTING	7:6	BOOST_ DVS	01	RW	Voltage scaling slew rate for Boost. 00: 1V/ms 01: 2.5V/ms (default) 10: 5V/ms 11: 10V/ms
		5	BOOST_ EN	0	RW	BOOST enable. 0: Boost disable (default) 1: Boost enable
		4	BOOST_ BP	0	RW	Bypass mode (Priority higher than BOOST_EN) 0: Bypass mode disable (default) 1: Bypass mode enable
		3	RESET	0	W/C	Reset register table to default. 0: No change (default) 1: Reset all registers to default setting
		2	Reserved	0	RW	Reserved
		1	BOOST_ DIS	0	RW	Boost active output discharge method. 0: Without discharge (default) 1: With discharge
		0	CHIP_EN	0	RW	BOOST enable selection. 0: Internal I^2C control (default) 1: External pin control

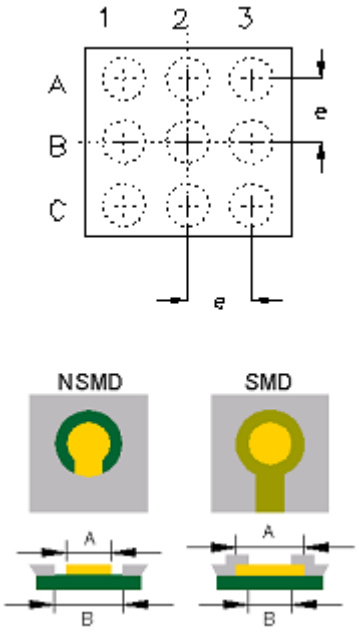
18 Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.500	0.600	0.020	0.024
A1	0.170	0.230	0.007	0.009
b	0.240	0.300	0.009	0.012
D	1.160	1.240	0.046	0.049
D1	0.800		0.031	
E	1.260	1.340	0.050	0.053
E1	0.800		0.031	
e	0.400		0.016	

9B WL-CSP 1.3x1.2 Package (BSC)

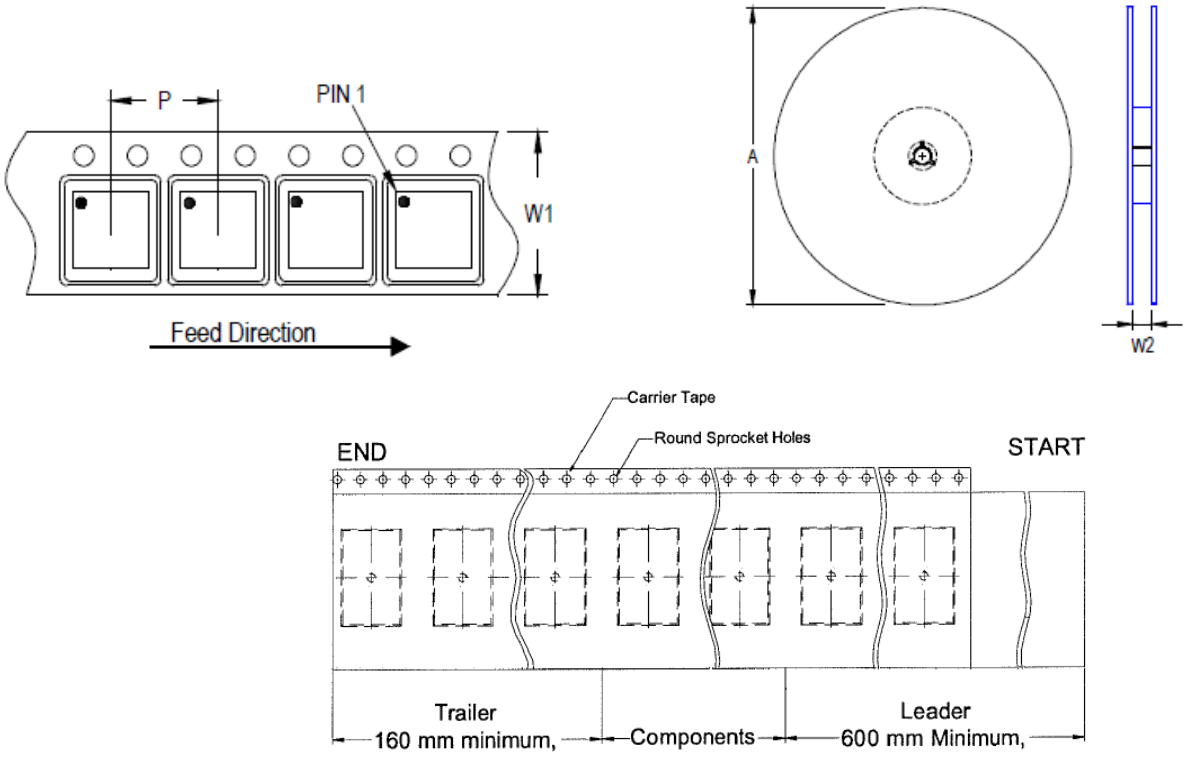
19 Footprint Information



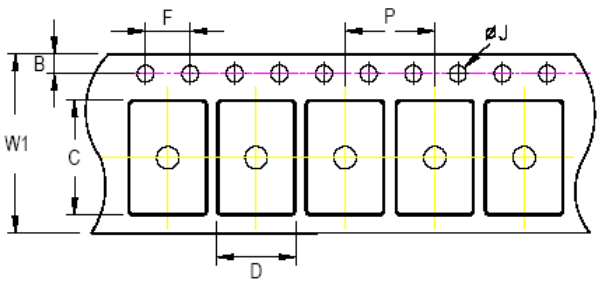
Package	Number of Pin	Type	Footprint Dimension (mm)			Tolerance
			e	A	B	
WL-CSP1.3x1.2-9(BSC)	9	NSMD	0.400	0.240	0.340	±0.025
		SMD		0.270	0.240	

20 Packing Information

20.1 Tape and Reel Data



Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min/Max (mm)
			(mm)	(in)				
WL-CSP 1.3x1.2	8	4	180	7	3,000	160	600	8.4/9.9



C, D, and K are determined by component size. The clearance between the components and the cavity is as follows:

- For 8mm carrier tape: 0.5mm max.

Tape Size	W1	P		B		F		ØJ		K		H
	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Max
8mm	8.3mm	3.9mm	4.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	0.7mm	0.8mm	0.6mm

20.2 Tape and Reel Packing

Step	Photo/Description	Step	Photo/Description
1	 Reel 7”	4	 12 inner boxes per outer box
2	 Packing by Anti-Static Bag	5	 Outer box **Carton A**
3	 3 reels per inner box **Box A**	6	

Container / Package	Reel		Box			Carton		
	Size	Units	Item	Reels	Units	Item	Boxes	Unit
WL-CSP 1.3x1.2	7”	3,000	Box A	3	9,000	Carton A	12	108,000
			Box E	1	3,000	For Combined or Un-full Reel.		

20.3 Packing Material Anti-ESD Property

Surface Resistance	Aluminum Bag	Reel	Cover tape	Carrier tape	Tube	Protection Band
Ω/cm^2	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**

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21 Datasheet Revision History

Version	Date	Description	Item
00	2022/11/3	Final	
01	2024/12/27	Modify	*Ordering Information on page 2* - Added note *Application Information page 20, 23* - Added start-up sequence - Added power off sequence - Updated declaration *Packing Information page 30, 31, 32* - Updated packing information