RICHTEK®

RT4812

High Efficiency Boost Converter

1 General Description

The RT4812 allows systems to take advantage of new battery chemistries that can supply significant energy even when the battery voltage is lower than the required voltage for system power ICs. By combining built-in power transistors, synchronous rectification, and low supply current, this IC provides a compact solution for systems using advanced Li-Ion battery chemistries.

The RT4812 is a boost regulator designed to provide a minimum output voltage from a single-cell Li-Ion battery, even when the battery voltage is below system minimum. In boost mode, output voltage regulation is guaranteed up to a maximum load current of 2.1A. Quiescent current in Shutdown Mode is less than 1μA, which maximizes battery life.

The recommended junction temperature range is –40°C to 125°C, and the ambient temperature range is –40°C to 85°C.

2 Ordering Information

RT4812 □□

Package Type(1)
J8F: TSOT-23-8 (FC)

Lead Plating System
G: Richtek Green Policy Compliant(2)

Note 1.

- Marked with (1) indicated: Compatible with the current requirements of IPC/JEDEC J-STD-020.
- Marked with (2) indicated: Richtek products are Richtek Green Policy compliant.

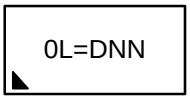
3 Features

- **CMCOT Topology with Small Output Ripple when VIN is close to VOUT Voltage**
- **Operate from a Single Li-ion Cell: 1.8V to 5.5V**
- **Adjustable Output Voltage: 1.8V to 5.5V**
- **PSM Operation**
- **Up to 96% Efficiency**
- **Boost Current Limit**
- **Output Overvoltage Protection**
- **Pin-Adjustable Average Output Current-Limit Threshold (2 Levels)**
- **Internal Compensation**
- **Output Discharge**
- **Output Short Protection**
- **True Load Disconnect**

4 Applications

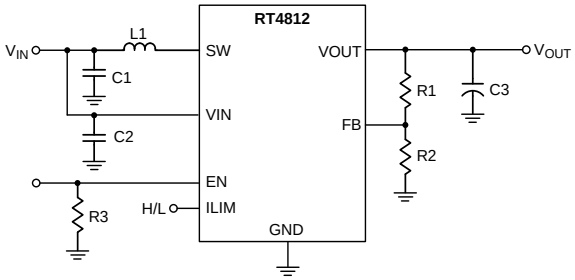
- Single-Cell Li-Ion, LiFePO4 Smart Phones
- Portable Equipment

5 Marking Information



0L= : Product Code
DNN : Date Code

6 Simplified Application Circuit



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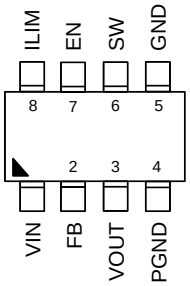
7 Pin Configuration

(TOP VIEW)

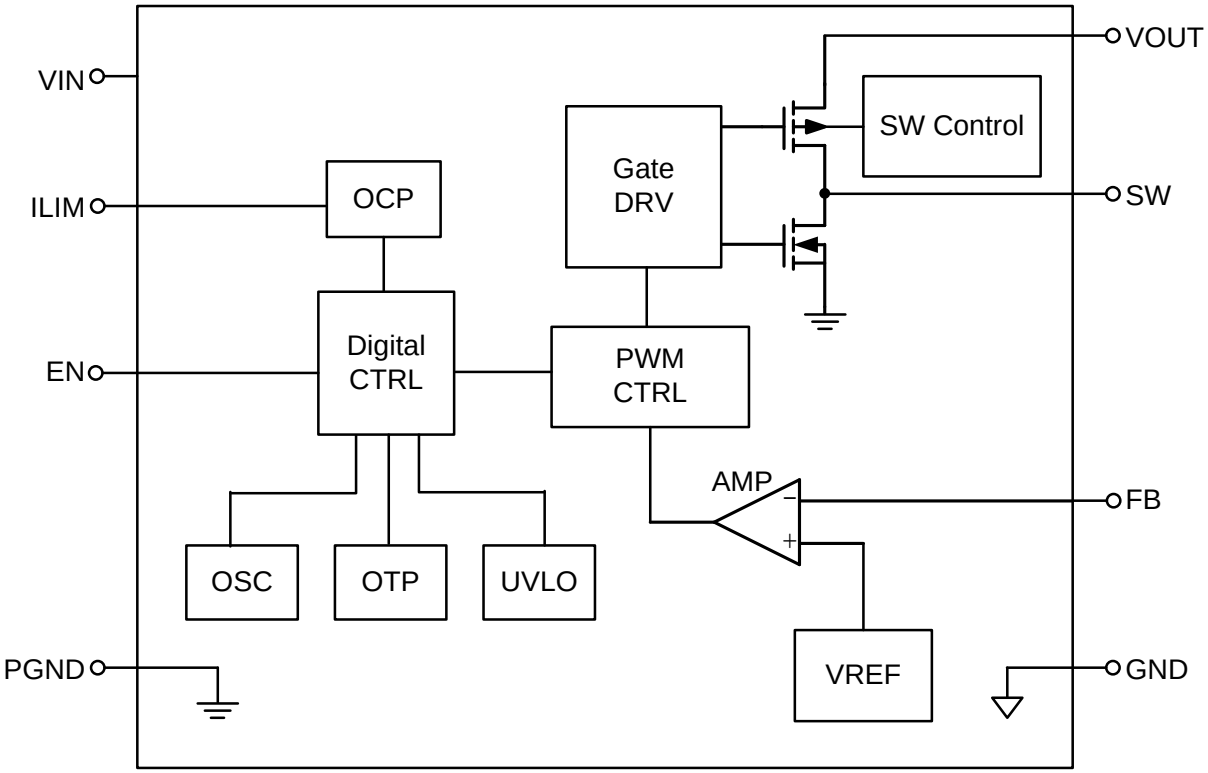


TSOT-23-8 (FC)

8 Functional Pin Description

Pin No.	Pin Name	Pin Function
1	VIN	Power input. Input capacitor C_{IN} must be placed as close to the IC as possible.
2	FB	Voltage feedback.
3	VOUT	Boost converter output.
4	PGND	Power ground.
5	GND	Analog ground.
6	SW	Switching node.
7	EN	Enable input (1 enabled, 0 disabled), must not be floating.
8	ILIM	Average output current limit control pin. (H/L)

9 Functional Block Diagram



10 Absolute Maximum Ratings

(Note 2)

- VIN, FB, ILIM, EN, SW to GND ---------- –0.2V to 6V
- VOUT to GND ---------- 6.2V
- Power Dissipation, P_D @ T_A = 25°C

  TSOT-23-8 (FC) ---------- 1.78W
- Package Thermal Resistance (Note 3)

  TSOT-23-8 (FC), θ_{JA} ---------- 56°C/W

  TSOT-23-8 (FC), θ_{JC} ---------- 28°C/W
- Lead Temperature (Soldering, 10sec.) ---------- 260°C
- Junction Temperature ---------- –65°C to 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 4)

  HBM (Human Body Model) ---------- 2kV

Note 2. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 3. θ_{JA} is measured at T_A = 25°C on a two-layer Richtek Evaluation Board.

Note 4. Devices are ESD sensitive. Handling precautions are recommended.

11 Recommended Operating Conditions

(Note 5)

- Input Voltage Range ---------- 1.8V to 5.5V
- Output Voltage Range ---------- 1.8V to 5.5V
- Junction Temperature (T_J) Range ---------- –40°C to 125°C
- Ambient Temperature (T_A) Range ---------- –40°C to 85°C

Note 5. The device is not guaranteed to function outside its operating conditions.

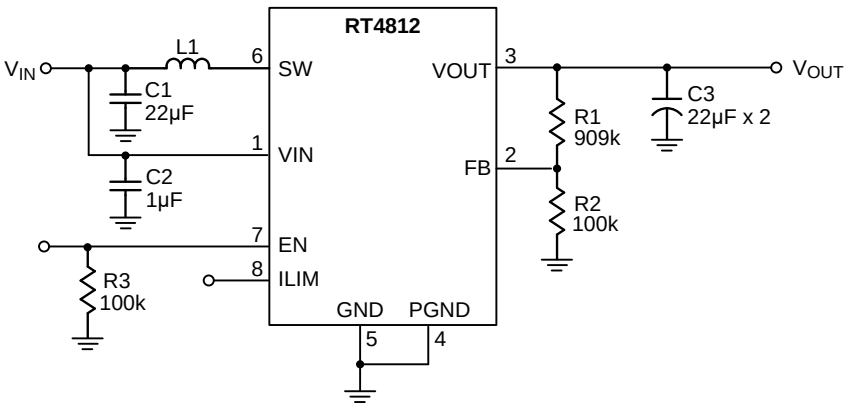
12 Electrical Characteristics

(V_{IN} = 3.6V, T_A = 25°C, unless otherwise specified.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Input Voltage	V_{IN}	$V_{IN} < V_{OUT} – 0.2V$	1.8	--	5.5	V
Output Voltage	V_{OUT}	$V_{IN} < V_{OUT} – 0.2V$	1.8	--	5.5	V
Undervoltage-Lockout Rising Threshold	V_{UVLO_R}		1.5	1.65	1.8	V
Undervoltage-Lockout Falling Threshold	V_{UVLO_F}		1.3	1.55	1.7	V
Feedback Voltage	V_{FB}	Force PWM	0.495	0.5	0.505	V
Output Voltage Accuracy	V_{OUT_ACC}	$1.8 \le V_{IN} \le V_{OUT} – 0.2V$ I_{OUT} = 0mA (PSM)	–2	--	4	%

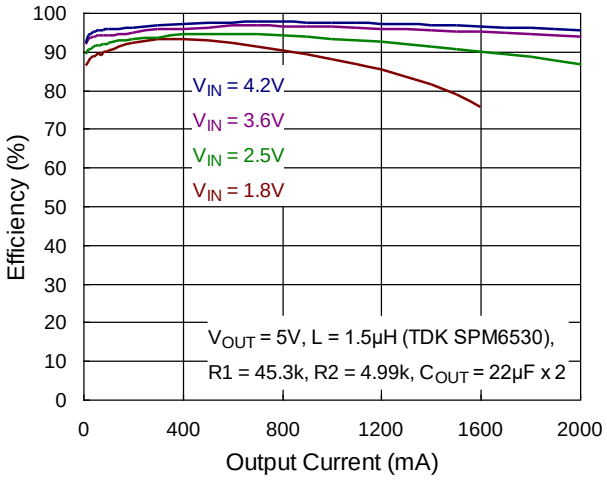
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Shutdown Current	I_{SHDN}	EN = 0V	--	0.1	1	μA
Quiescent Current (Non-Switching Current)	I_{Q_NSW}	Close loop, no load FB = 3V, non-switching current	--	90	--	μA
Pre-Charge Current	I_{PRECHG}		--	1	--	A
Switching Frequency	f_{SW}	$V_{OUT} - V_{IN} > 1V$	--	0.5	--	MHz
Average Output Current Limit	I_{LIM}	I_{LIM} = L	1	--	--	A
		I_{LIM} = H	2.1	--	--	
On-Resistance of High-Side MOSFET	R_{DSON_H}	V_{IN} = 5V	--	45	--	mΩ
On-Resistance of Low-Side MOSFET	R_{DSON_L}	V_{IN} = 5V	--	30	--	mΩ
The FB Pin Input Leakage Current	I_{FB_LK}		–1	--	1	μA
SW Leakage Current	I_{SW_LK}	All switch off	--	--	5	μA
Line Regulation	V_{LINE_REG}	V_{IN} = 2.7V to 4.5V, V_{OUT} = 5V, I_{OUT} = 1500mA	–2	--	2	%
Load Regulation	V_{LOAD_REG}	CCM, I_{OUT} < 2A, V_{IN} = 3.6V, V_{OUT} = 5V	–1.5	--	1.5	%
Output Overvoltage Protection	V_{OVP}		5.8	6	6.2	V
EN Input Voltage Falling Threshold	V_{EN_F}		--	--	0.4	V
EN Input Voltage Rising Threshold	V_{EN_R}		1.2	--	--	V
EN Input Current	I_{EN}		--	0.1	1	μA
Over-Temperature Protection Threshold	T_{OTP}		--	160	--	°C
Over-Temperature Protection Hysteresis	T_{OTP_HYS}		--	30	--	°C

13 Typical Application Circuit

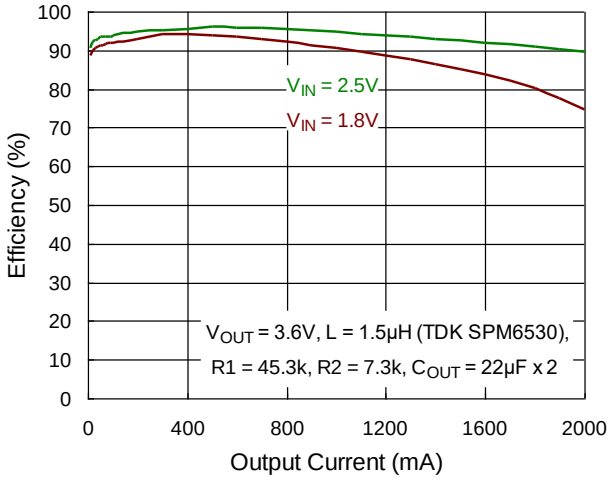


14 Typical Operating Characteristics

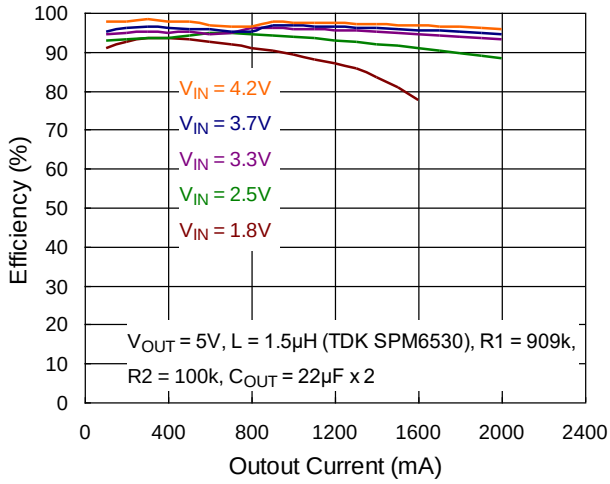
Efficiency vs. Output Current



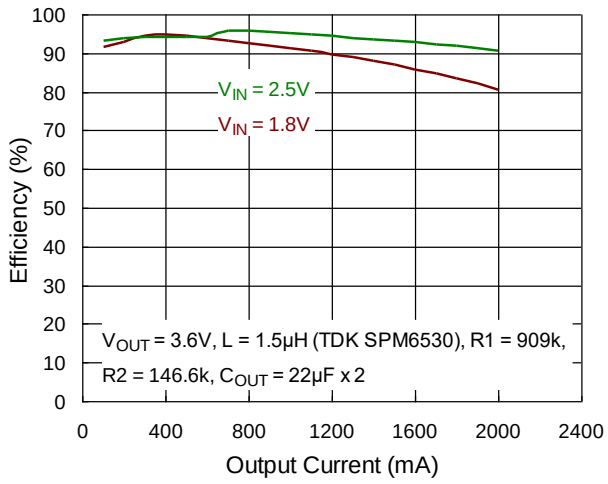
Efficiency vs. Output Current



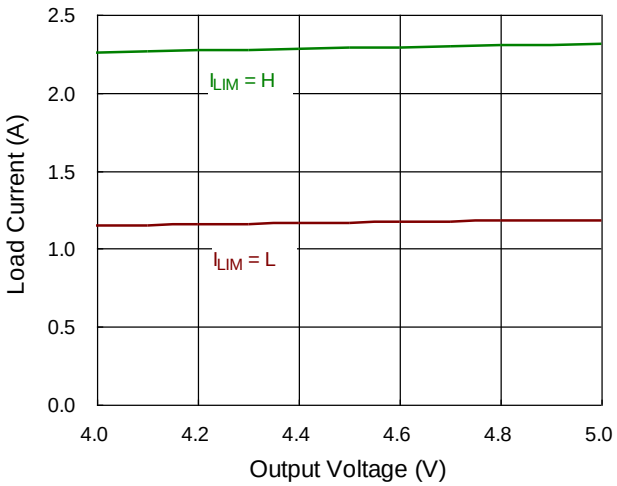
Efficiency vs. Outout Current



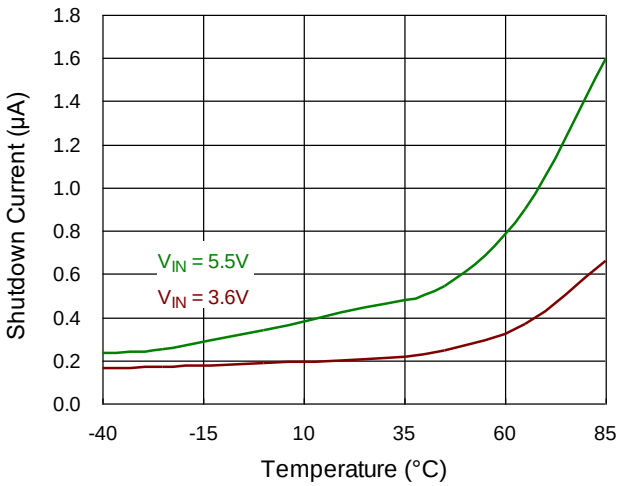
Efficiency vs. Output Current



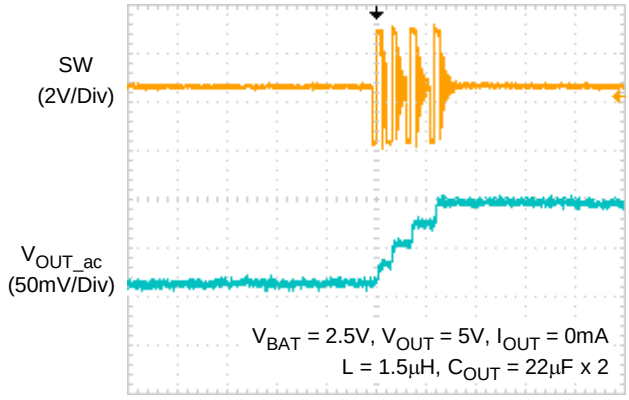
Load Current vs. Output Voltage



Shutdown Current vs. Temperature

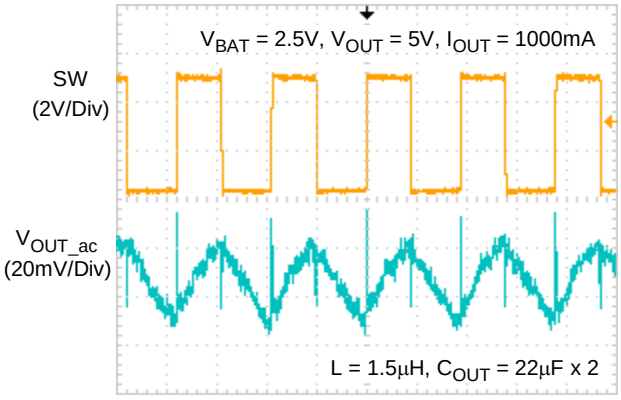


Output Voltage Ripple



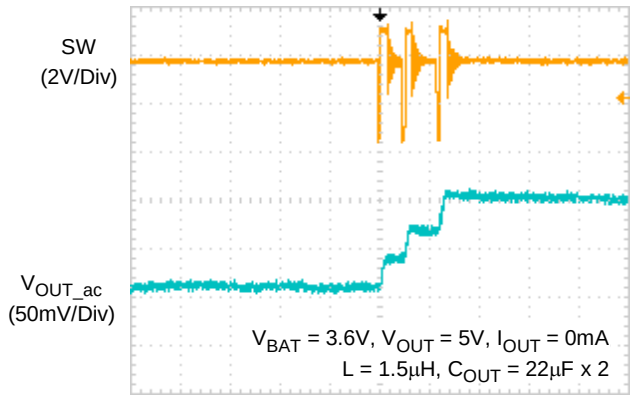
Time (10µs/Div)

Output Voltage Ripple



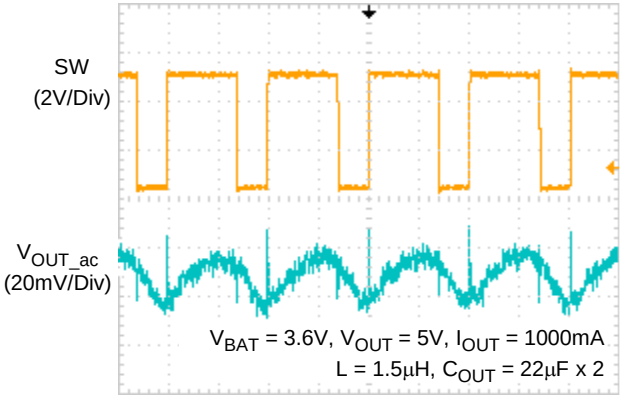
Time (1µs/Div)

Output Voltage Ripple



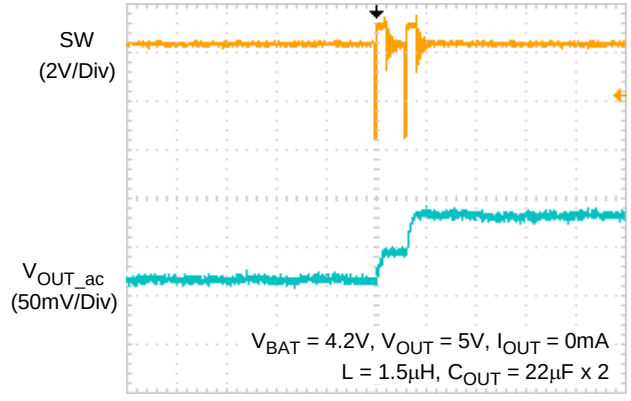
Time (10µs/Div)

Output Voltage Ripple



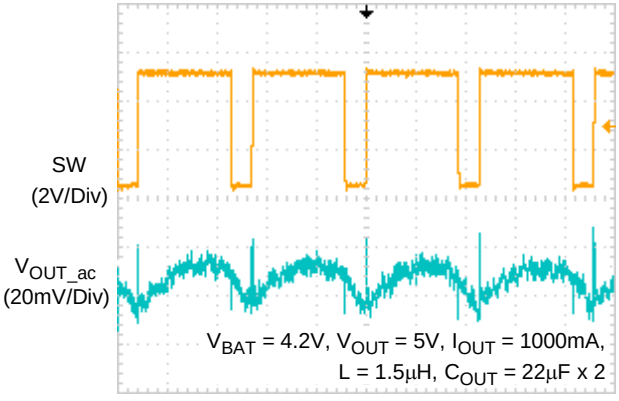
Time (1µs/Div)

Output Voltage Ripple



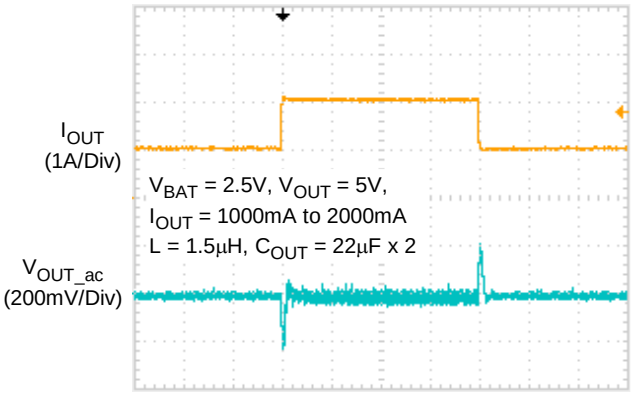
Time (10µs/Div)

Output Voltage Ripple

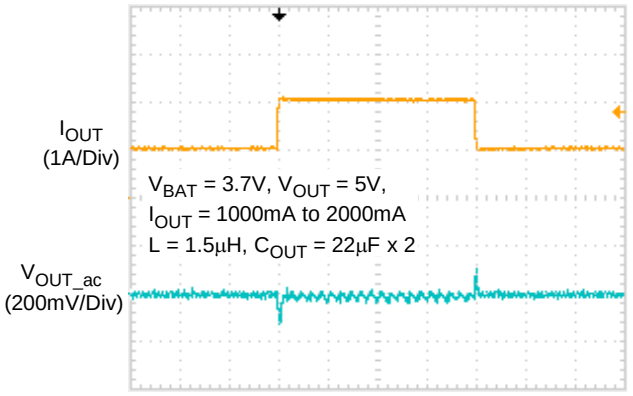


Time (1µs/Div)

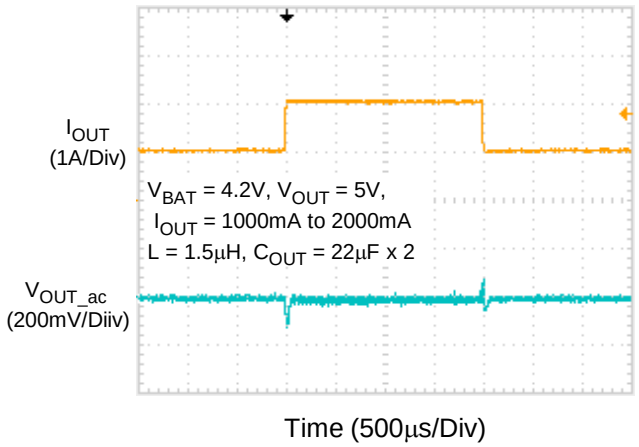
Load Transient Response



Load Transient Response



Load Transient Response



15 Operation

The RT4812 combines built-in power transistors, synchronous rectification, and low supply current, providing a compact solution for systems using advanced Li-Ion battery chemistries.

In boost mode, output voltage regulation is guaranteed up to a maximum load current of 2.1A. The quiescent current in Shutdown mode is less than 1μA, maximizing battery life.

Mode		Depiction	Condition
LIN	LIN 1	Linear startup 1	$V_{IN} > V_{OUT}$
	LIN 2	Linear startup 2	$V_{IN} > V_{OUT}$
Soft-Start		Boost soft-start	$V_{OUT} < V_{OUT(MIN)}$
Boost		Boost mode	$V_{OUT} = V_{OUT(MIN)}$

15.1 LIN State

When V_{IN} is rising, the system enters the LIN state, which consists of two parts: LIN1 provides a maximum charging current of 1A for C_{OUT}, and LIN2 provides a maximum charging current of 3A. Additionally, the EN pin is pulled high and V_{IN} is greater than UVLO.

As shown in the figure, if the timeout exceeds the specification, the system will enter fault state.

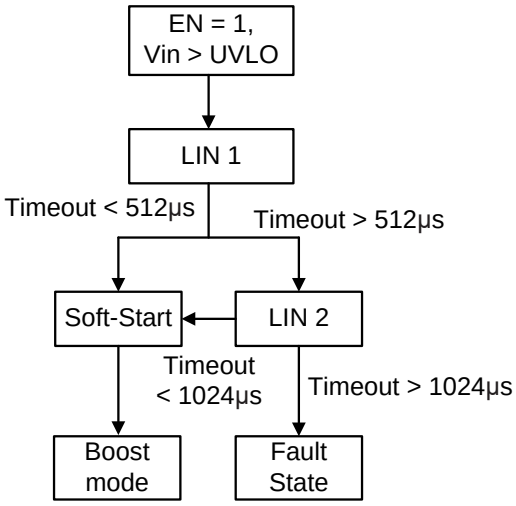


Figure 1. RT4812 State Chart

15.2 Startup and Shutdown State

When V_{IN} is rising and passes through the LIN state, the system will enter the startup state. If EN is pulled low, all functions are turned off in shutdown mode.

15.3 Soft-Start State

The system begins switching in the soft-start state. After the LIN state, the output voltage rises along with the internal reference voltage.

15.4 Fault State

As shown in Figure 1, it will enter the fault state under the following condition:

- The timeout of LIN2 exceeds 1024μs.

When a fault is triggered, there will be high impedance between the input and output. A restart will occur after 20ms.

15.5 Overcurrent Protection (OCP)

The converter senses the current signal when the high-side P-MOSFET turns on. As a result, the OCP operates with cycle-by-cycle current limitation. If the OCP occurs, the converter holds off the next on pulse until inductor current drops below the OCP limit.

15.6 Over-Temperature Protection (OTP)

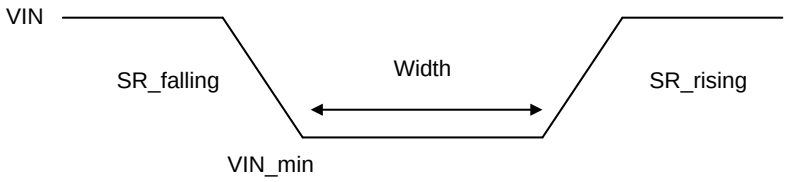
The converter has an over-temperature protection. When the junction temperature exceeds the thermal shutdown rising threshold, the system will latch, and the output voltage will no longer be regulated until the junction temperature drops below the falling threshold.

15.7 Input Voltage POR (Power-On Reset)

The RT4812 implements a Power-on Reset (POR) function. The POR function is used to reset the IC's status to its default settings. The POR function is activated when V_{IN} drops and must meet the POR requirements. The POR function may fail if the VIN patterns do not meet the requirements for a POR event.

The requirements for a POR event are listed below; refer to Figure 2 for the voltage pattern.

1. VIN_min < 0.5V
2. Width > 20μs
3. SR_rising < 1V/μs



VIN : Input voltage
SR_falling : Slew rate for input voltage drop
SR_rising : Slew rate for input voltage resume
Width : Duration of input voltage drop
VIN_min : Minimum voltage

Figure 2. POR Pattern Illustration

16 Application Information

(Note 6)

16.1 Enable

The device can be enabled or disabled by the EN pin. When the EN pin is higher than the logic-high threshold, the device starts operating with soft-start. Once the EN pin is set to low, the device will shut down. In shutdown mode, the converter stops switching, internal control circuitry is turned off, and the load is disconnected from the input. This also means that the output voltage can drop below the input voltage during shutdown.

16.2 Soft-Start State

After successfully completing the LIN state (VOUT ≥ VIN - 300mV), the regulator begins switching with a boost valley-current limit of 3500mA. During the soft-start state, V_{OUT} is ramped up by Boost internal loop. If V_{OUT} fails to reach target value during the soft-start period for more than 2ms, a fault condition is declared.

16.3 Output Voltage Setting

The output voltage is adjustable by an external resistive divider. The resistive divider must be connected between VOUT, FB and GND. When the output voltage is regulated properly, the typical value of the voltage at the FB pin is 500mV. The output voltage can be calculated using the equation below:

$$R1 = R2 \times \left(\frac{V_{OUT}}{V_{FB}} - 1 \right)$$

16.4 Power Save Mode (PSM)

PSM is used to improve efficiency at light loads. When the output voltage is lower than a set threshold voltage, the converter will operate in PSM.

It raises the output voltage with several pulses until the loop exits PSM.

16.5 Undervoltage-Lockout

The undervoltage-lockout circuit prevents the device from operating incorrectly at low input voltages. It prevents the converter from turning on the power switches under undefined conditions and prevents the battery from deep discharge. The VIN voltage must be greater than 1.65V to enable the converter. During operation, if the VIN voltage drops below 1.55V, the converter is disabled and waits for internal IC default parameter values to be ready until the supply exceeds the UVLO rising threshold. The RT4812 automatically restarts if the input voltage recovers to the input voltage UVLO high level.

16.6 Over-Temperature Protection

The device has a built-in temperature sensor which monitors the internal junction temperature. If the temperature exceeds the threshold, the device stops operating. As soon as the IC temperature has decreased below the threshold with hysteresis, it starts operating again. The built-in hysteresis is designed to avoid unstable operation at IC temperatures near the over-temperature threshold.

16.7 Inductor Selection

The recommended nominal inductance value is 1.5μH. It is recommended to use an inductor with a dc saturation current ≥ 5000mA.

Table 1. List of Inductors

Manufacturer	Series	Dimensions (in mm)	Saturation Current (mA)
TDK	SPM6530T	7.1 x 6.5 x 3.0	11500
Taiyo Yuden	NRS5040T	5.15 x 5.15 x 4.2	6400

16.8 Input Capacitor Selection

At least a 22μF capacitor with a rated voltage of 16V for the DC bias input is recommended to improve the transient behavior of the regulator and the EMI behavior of the total power supply circuit for SW. Additionally, at least a 1μF ceramic capacitor placed as close as possible to the VIN and GND pins of the IC is recommended.

16.9 Output Capacitor Selection

At least two 22μF capacitors are recommended to improve V_{OUT} ripple. Output voltage ripple is inversely proportional to C_{OUT}. The output capacitor is selected according to the output ripple, which is calculated as follows:

$$V_{RIPPLE(P-P)} = t_{ON} \times \frac{I_{LOAD}}{C_{OUT}}$$

and

$$t_{ON} = t_{SW} \times D = t_{SW} \times \left(1 - \frac{V_{IN}}{V_{OUT}}\right)$$

therefore :

$$C_{OUT} = t_{SW} \times \left(1 - \frac{V_{IN}}{V_{OUT}}\right) \times \frac{I_{LOAD}}{V_{RIPPLE(P-P)}}$$

and

$$t_{SW} = \frac{1}{f_{SW}}$$

The maximum V_{RIPPLE} occurs at minimum input voltage and maximum output load.

16.10 Output Discharge Function

When the EN pin is set to low, the VOUT pin is internally connected to GND for 10ms through an internal discharge N-MOSFET switch. After the 10ms period, the IC will be in a true shutdown state.

This feature prevents residual charge voltages on capacitors connected to the VOUT pins, which may impact proper power-up of the system.

16.11 Valley Current Limit

The RT4812 employs a valley current limit detection scheme to sense inductor current during the off-time. When the loading current is increased such that the loading is above the valley current-limit threshold, the off-time is increased until the current is decreased to the valley-current threshold. The next on-time begins after the current is decreased to the valley-current threshold. On-time is decided by (V_{OUT} – V_{IN}) / V_{OUT} ratio. The output voltage decreases when further loading current increases. The current limit function is implemented by this scheme; refer to Figure 3.

16.12 Average Output Current Limit

The RT4812 features an average output current limit to protect the output terminal. When the load current exceeds the limit, the output current will be clamped.

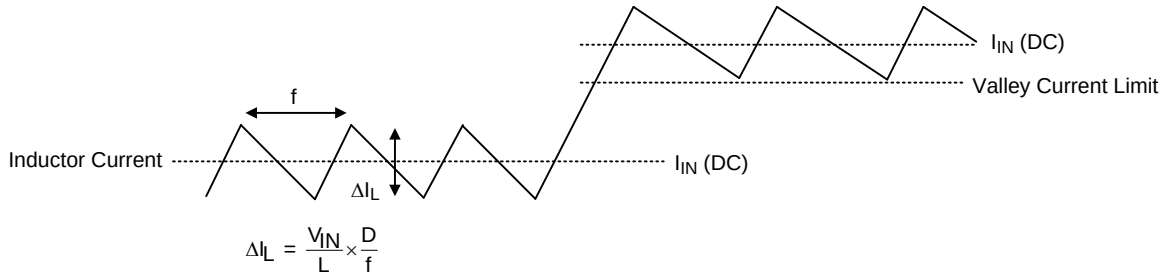


Figure 3. Inductor Current in Current Limit Operation

Table 2. List of Capacitor

Reference	Qty	Part Number	Description	Package	Manufacturer
CIN	1	GRM21BR61C226ME44	22μF/16V/X5R	0805	Murata
COUT	2	GRM21BR61C226ME44	22μF/16V/X5R	0805	Murata

16.13 Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula:

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a TSOT-23-8 (FC) package, the thermal resistance, θ_{JA}, is 56°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below:

$P_{D(MAX)}$ = (125°C – 25°C) / (56°C/W) = 1.78W for a TSOT-23-8 (FC) package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curve in Figure 4 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

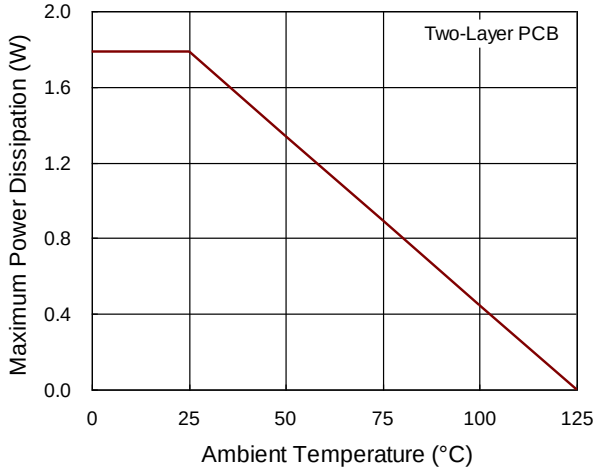


Figure 4. Derating Curve of Maximum Power Dissipation

16.14 Layout Considerations

The PCB layout is an important step to maintain the high performance of the RT4812.

Both the high current and the fast switching nodes require careful attention to the PCB layout to ensure the robustness of the RT4812.

Improper layout might result in poor line or load regulation, ground and output voltage shifts, stability issues, unsatisfactory EMI behavior, or reduced efficiency. For the best performance of the RT4812, the following PCB layout guidelines must be strictly followed:

- Input/output capacitors must be placed as close as possible to the input/output pins.
- The SW pin should be connected to the Inductor with a wide and short trace, and sensitive components should be kept away from this trace.
- The feedback divider should be placed as close as possible to the FB pin.

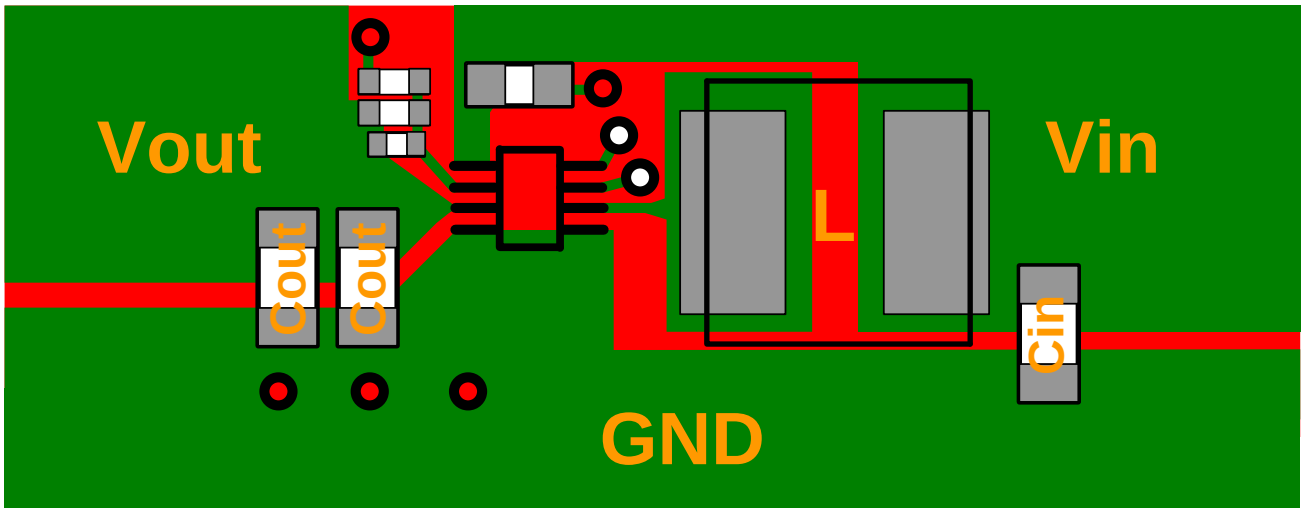
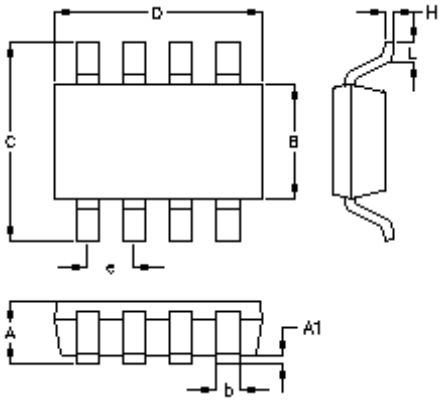


Figure 5. PCB Layout Guide

Note 6. The information provided in this section is for reference only. The customer is solely responsible for designing, validating, and testing any applications incorporating Richtek's product(s). The customer is also responsible for applicable standards and any safety, security, or other requirements.

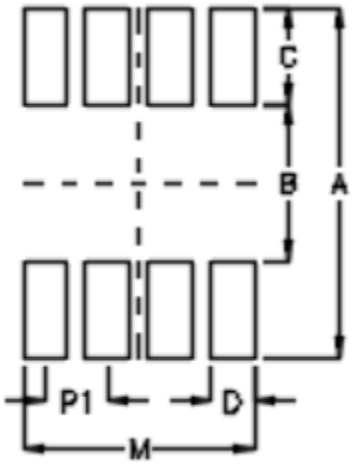
17 Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	1.000	0.028	0.039
A1	0.000	0.100	0.000	0.004
B	1.397	1.803	0.055	0.071
b	0.220	0.380	0.009	0.015
C	2.591	3.000	0.102	0.118
D	2.692	3.099	0.106	0.122
e	0.585	0.715	0.023	0.028
H	0.080	0.254	0.003	0.010
L	0.300	0.610	0.012	0.024

TSOT-23-8 (FC) Surface Mount Package

18 Footprint Information

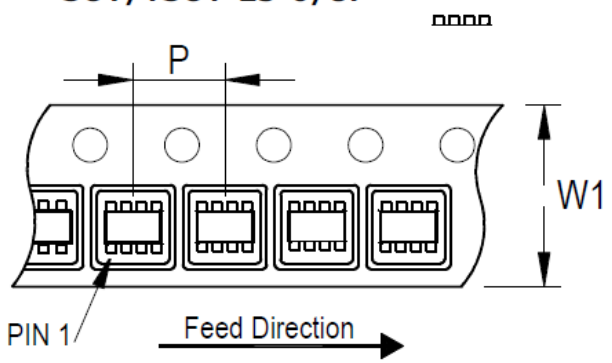


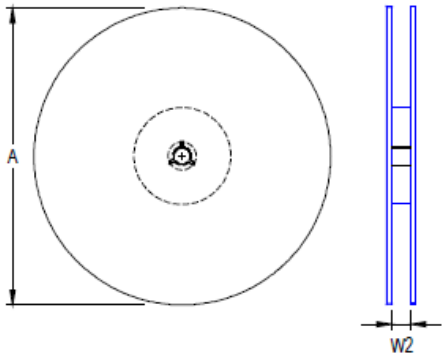
Package	Number of Pin	Footprint Dimension (mm)						Tolerance
		P1	A	B	C	D	M	
TSOT-28/TSOT-28(FC)/SOT-28	8	0.65	3.60	1.60	1.00	0.45	2.40	±0.10

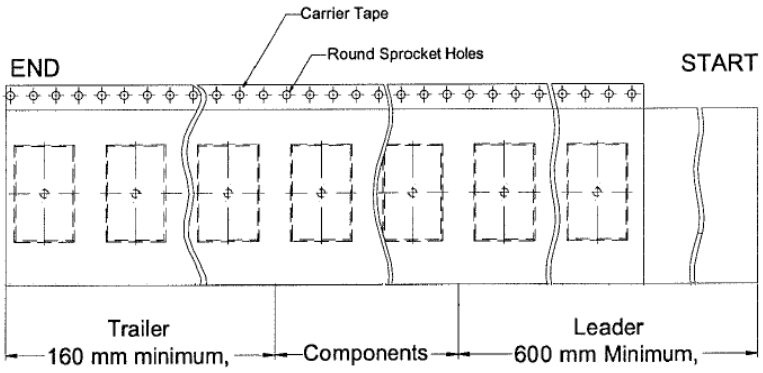
19 Packing Information

19.1 Tape and Reel Data

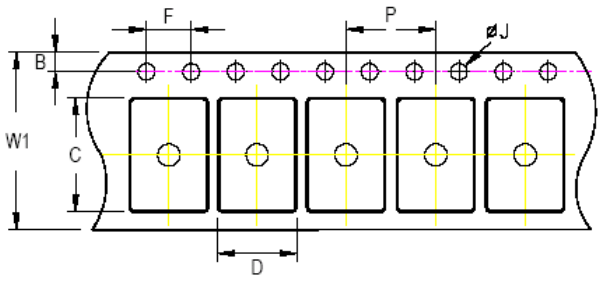
SOT/TSOT-23-6/8:







Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min./Max. (mm)
			(mm)	(in)				
TSOT-23-8	8	4	180	7	3,000	160	600	8.4/9.9



C, D, and K are determined by component size.

The clearance between the components and the cavity is as follows:

- For 8mm carrier tape: 0.5mm max.

Tape Size	W1	P		B		F		ØJ		K		H
	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Max.
8mm	8.3mm	3.9mm	4.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	1.0mm	1.2mm	0.6mm

19.2 Tape and Reel Packing

Step	Photo/Description	Step	Photo/Description
1	 Reel 7”	4	 3 reels per inner box **Box A**
2	 HIC & Desiccant (1 Unit) inside	5	 12 inner boxes per outer box
3	 Caution label is on backside of Al bag	6	 Outer box **Carton A**

Container / Package	Reel		Box			Carton		
	Size	Units	Item	Reels	Units	Item	Boxes	Unit
TSOT-23-8	7”	3,000	Box A	3	9,000	Carton A	12	108,000
			Box E	1	3,000	For Combined or Partial Reel.		

19.3 Packing Material Anti-ESD Property

Surface Resistance	Aluminum Bag	Reel	Cover tape	Carrier tape	Tube	Protection Band
Ω/cm^2	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**

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20 Datasheet Revision History

Version	Date	Description	Item
10	2024/8/20	Modify	*General Description on page 1* -Added Temperature range *Ordering Information on page 1* -Modified description *Electrical Characteristics on page 5, 6* -Updated description and symbol *Application Information on page 16* -Added the declaration *Footprint Information on page 18* -Added footprint information *Packing Information on page 19, 20, 21* -Added packing information