2.5MHz Synchronous Boost Regulator

1 General Description

The RT4803B allows systems to take advantage of new battery chemistries that can supply significant energy when the battery voltage is lower than the required voltage for system power ICs. By combining built-in power transistors, synchronous rectification, and low supply current, this IC provides a compact solution for systems using advanced Li-Ion battery chemistries.

The RT4803B is a boost regulator designed to provide a minimum output voltage from a single-cell Li-Ion battery, even when the battery voltage is below the system minimum. In boost mode, output voltage regulation is guaranteed up to a maximum load current of 2000mA. The quiescent current in shutdown mode is less than 1μA, which maximizes battery life. The regulator transitions smoothly between bypass and normal boost modes. The device can be forced into bypass mode to reduce quiescent current.

The RT4803B is available in the WL-CSP-16B 1.67x1.67 (BSC) package. The recommended junction temperature range is –40°C to 125°C, and the ambient temperature range is –40°C to 85°C.

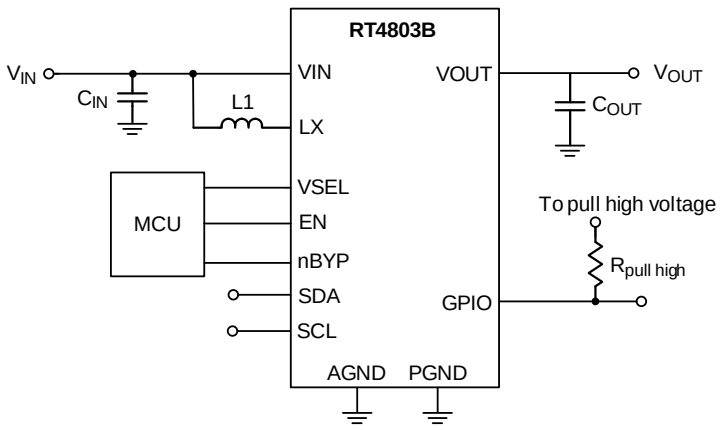
2 Applications

- Single-Cell Li-Ion, LiFePO4 for Smartphones or Tablets
- 2.5G/3G/4G Mini-Module Data Cards

3 Features

- **Input Voltage Range: 1.8V to 5V**
- **Programmable Output Voltage from 2.85V to 4.4V with 50mV/Step**
- **Default Boost Output Voltage Setting:**
  - **V_{OUT} = 3.4V at VSEL = H**
  - **V_{OUT} = 3.15V at VSEL = L**
- **Maximum Continuous Load Current: 2A at V_{IN} > 2.65V Boosting V_{OUT} to 3.35V**
- **Up to 95% Efficiency**
- **nBYP (L): Forced Bypass Mode**
- **nBYP (H): Auto Bypass Operation when V_{IN} > Target V_{OUT}**
- **Internal Synchronous Rectifier**
- **Overcurrent Protection**
- **Undervoltage Protection**
- **Overvoltage Protection**
- **Over-Temperature Protection**
- **Ultra-Low Operating Quiescent Current**
- **Discharge Function Triggered at GPIO Manual Pull Low**
- **Available in a WL-CSP-16B 1.67x1.67 (BSC) Package**

4 Simplified Application Circuit



5 Ordering Information

RT4803B □-□

- Packing
  A: Standard
- Package Type (1)
  P: WL-CSP-16B 1.67x1.67 (BSC)

Note 1.

Richtek products are Richtek Green Policy compliant and marked with (1) indicates compatible with the current requirements of IPC/JEDEC J-STD-020.

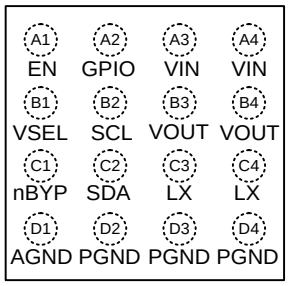
6 Marking Information

D8: Product Code
XXYY: Wafer ID with Check Sum
CCC-RRR: IC Coordinate (X, Y)
YMDAN: Date Code

Table of Contents

7 Pin Configuration

(TOP VIEW)

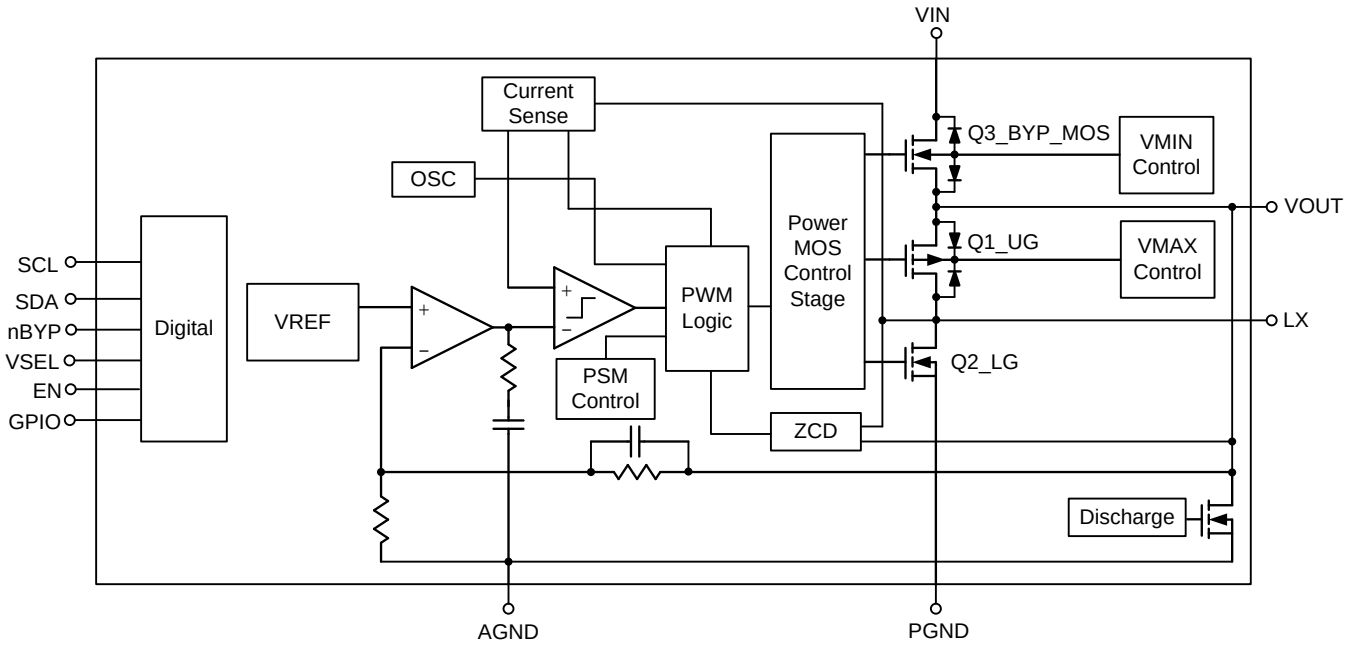


WL-CSP-16B 1.67x1.67 (BSC)

8 Functional Pin Description

Pin No.	Pin Name	I/O	Pin Function
A1	EN	I	Chip enable input pin. A high-level voltage enables the device, while a low-level voltage turns the device off. This pin must be terminated.
A2	GPIO	I/O	General purpose input/output. (Details are illustrated in the operation section.)
A3, A4	VIN	I	Power supply input.
B1	VSEL	I	Output voltage selection pin. The default boost output voltage setting is V_{OUT} = 3.4V at VSEL = H and V_{OUT} = 3.15V at VSEL = L. This pin must be terminated.
B2	SCL	I	Serial interface clock. (Pull down if I^2C is not used.)
B3, B4	VOUT	O	Boost output voltage pin. The PCB trace length from BSTVOUT to the output filter capacitor should be as short and wide as possible.
C1	nBYP	I	This pin can be used to activate forced bypass mode. When this pin is LOW, the bypass switches are turned on into forced bypass mode. The detailed mode is defined in Table 2.
C2	SDA	I/O	Serial interface data line. (Pull down if I^2C is not used.)
C3, C4	LX	I/O	This pin is the connection between two built-in switches in the chip and should be connected to the external inductor. The inductor should be connected to this pin with the shortest path.
D1	AGND	--	Analog ground. This is the signal ground reference for the IC.
D2, D3, D4	PGND	--	Power ground should be connected to this pin with the shortest path for power transmission to reduce the parasitic components effects.

9 Functional Block Diagram



10 Absolute Maximum Ratings

(Note 2)

- EN, GPIO, VIN, VSEL, SCL, VOUT, nBYP, SDA, LX ---------- –0.2V to 6V
- LX (<200ns) ---------- –3V to 6V
- Power Dissipation, P_D @ T_A = 25°C

  WL-CSP-16B 1.67x1.67 (BSC) ---------- 2.09W
- Package Thermal Resistance (Note 3)

  WL-CSP-16B 1.67x1.67 (BSC), θ_{JA} ---------- 47.7°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 4)

  HBM (Human Body Model) ---------- 2kV

Note 2. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 3. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board, following the JEDEC 51-7 thermal measurement standard.

Note 4. Devices are ESD sensitive. Handling precautions are recommended.

11 Recommended Operating Conditions

(Note 5)

- Input Voltage Range ---------- 1.8V to 5V
- Output Voltage Range ---------- 2.85V to 4.4V
- Ambient Temperature Range ---------- –40°C to 85°C
- Junction Temperature Range ---------- –40°C to 125°C

Note 5. The device is not guaranteed to function outside its operating conditions.

12 Electrical Characteristics

(V_{IN} = 3V, V_{OUT} = 3.4V, T_A = 25°C, unless otherwise specified.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VIN Operation Range	V_{IN}		1.8	--	5	V
Quiescent Current	I_Q	Auto Bypass Mode, V_{IN} = 3.8V	--	36	70	µA
		Boost Mode, I_{LOAD} = 0mA, Switching, V_{IN} = 3V	--	56	100	
		Forced Bypass with LIQ, V_{IN} = 3.6V	--	5	8	
		Forced Bypass without LIQ, V_{IN} = 3.6V	--	16	25	
VIN Shutdown Current	I_{SHDN}	EN = 0V, nBYP = H, V_{IN} = 3.6V	--	--	2	µA

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VOUT to VIN Reverse Leakage	I_{LK}	V_{OUT} = 5V, EN = nBYP = H, V_{IN} < V_{OUT}, into V_{IN} leakage current (Note 6)	--	0.2	2	μA
VOUT Leakage Current	I_{LK_OUT}	V_{OUT} = 0V, EN = 0V, V_{IN} = 4.2V	--	0.1	1	μA
VOUT Discharge Impedance	R_DIS_OUT		--	80	--	Ω
Undervoltage Lock Out	V_{UVLO}	V_{IN} Rising	--	1.6	1.8	V
Undervoltage Lock Out Hysteresis	V_{UVLO_HYS}		--	200	--	mV
GPIO Low	V_{GPIO}	I_{GPIO} = 5mA	--	--	0.36	V
GPIO Leakage Current	I_{GPIO_LK}	V_{GPIO} = 5V	--	--	1	μA
Logic Level High EN, VSEL, nBYP, GPIO	V_{IH}		0.84	--	--	V
Logic Level Low EN, VSEL, nBYP, GPIO	V_{IL}		--	--	0.36	V
Output Voltage Accuracy	$V_{OUT\_ACCURACY}$	V_{OUT} - V_{IN} > 100mV, PWM	–2	--	2	%
Minimum On Time	T_{ON}	V_{IN} = 3V, V_{OUT} = 3.5V, I_{LOAD} > 1000mA	--	80	--	ns
Maximum Duty Cycle	D_{MAX}		40	--	--	%
Switching Frequency	f_{SW}	V_{IN} = 2.65V, V_{OUT} = 3.5V, I_{LOAD} = 1000mA	2	2.5	3	MHz
Boost Valley Current Limit	I_{CL}	V_{IN} = 2.9V	3.5	4	4.5	A
LIN1 Pre-Charge Current	I_{LIN1}		700	1000	1300	mA
LIN2 Pre-Charge Current	I_{LIN2}		1400	2000	2600	mA
Auto/Forced Bypass Current Limit	I_{BPCL}	V_{IN} = 3.2V	3	4	10	A
N-Channel Boost Switch $R_{DS(ON)}$ (UG)	R_{DSN}	V_{IN} = 3.2V, V_{OUT} = 3.5V	--	60	95	mΩ
P-Channel Boost Switch $R_{DS(ON)}$ (LG)	R_{DSP}	V_{IN} = 3.2V, V_{OUT} = 3.5V	--	40	80	mΩ
N-Channel Bypass Switch $R_{DS(ON)}$ (BYP_MOS)	R_{DSP_BYP}	V_{IN} = 3.2V, V_{OUT} = 3.5V	--	40	60	mΩ
Hot Die Trigger Threshold	T_{HD}	Boost Mode	--	100	--	°C
Hot Die Release Threshold	T_{HDR}	Boost Mode	--	90	--	°C
Over-Temperature Protection	T_{OTP}		--	160	--	°C
Over-Temperature Protection Hysteresis	T_{OTP_HYS}		--	20	--	°C
FAULT Restart Time	T_{RST}		--	1	--	ms

Note 6. V_{OUT} cannot be connected to an external power source at any operation state.

12.1 I²C Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
SCL, SDA High-Level Input Threshold Voltage	V_{IH_I2C}		0.84	--	--	V
SCL, SDA Low-Level Input Threshold Voltage	V_{IL_I2C}		--	--	0.36	V
SDA Digital Output Low	V_{OL_I2C}		--	--	0.36	V
SCL Clock Frequency	f_{CLK}	Standard-mode	--	--	100	kHz
		Fast-mode	--	--	400	
		Fast-mode Plus	--	--	1000	
Bus Free Time between Stop and Start Condition	t_{BUF}	Standard-mode	4.7	--	--	µs
		Fast-mode	1.3	--	--	
		Fast-mode Plus	0.5	--	--	
(Repeated) Start Hold Time	$t_{HD;STA}$	Standard-mode	4	--	--	µs
		Fast-mode	0.6	--	--	
		Fast-mode Plus	0.26	--	--	
(Repeated) Start Setup Time	$t_{SU;STA}$	Standard-mode	4.7	--	--	µs
		Fast-mode	0.6	--	--	
		Fast-mode Plus	0.26	--	--	
STOP Condition Setup Time	$t_{SU;STO}$	Standard-mode	4	--	--	µs
		Fast-mode	0.6	--	--	
		Fast-mode Plus	0.26	--	--	
SDA Data Hold Time	$t_{HD;DAT}$	Standard-mode	0.1	--	--	ns
		Fast-mode	0.1	--	--	
		Fast-mode Plus	0.1	--	--	
SDA Valid Acknowledge Time	$t_{VD;ACK}$	Standard-mode	--	--	3.45	µs
		Fast-mode	--	--	0.9	
		Fast-mode Plus	--	--	0.45	
SDA Setup Time	$t_{SU;DAT}$	Standard-mode	250	--	--	ns
		Fast-mode	100	--	--	
		Fast-mode Plus	50	--	--	
SCL Clock Low Time	t_{LOW}	Standard-mode	4.7	--	--	µs
		Fast-mode	1.3	--	--	
		Fast-mode Plus	0.5	--	--	
SCL Clock High Time	t_{HIGH}	Standard-mode	4	--	--	µs
		Fast-mode	0.6	--	--	
		Fast-mode Plus	0.26	--	--	

13 Typical Application Circuit

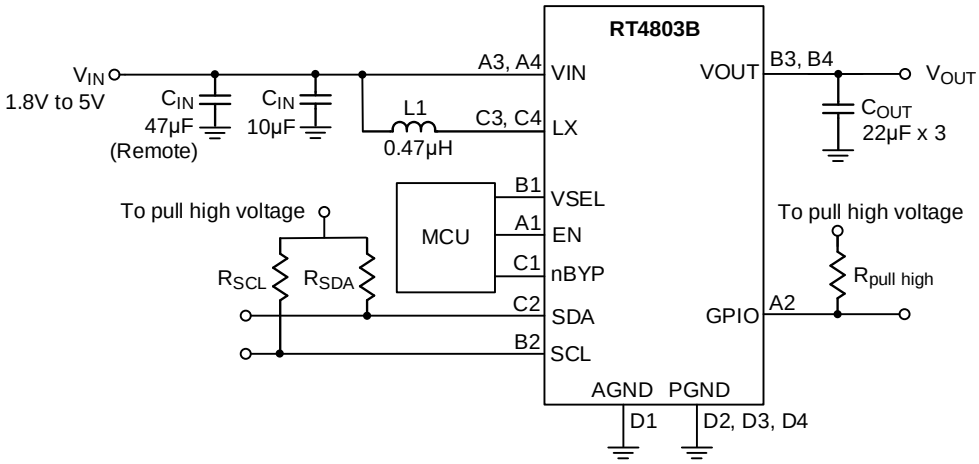


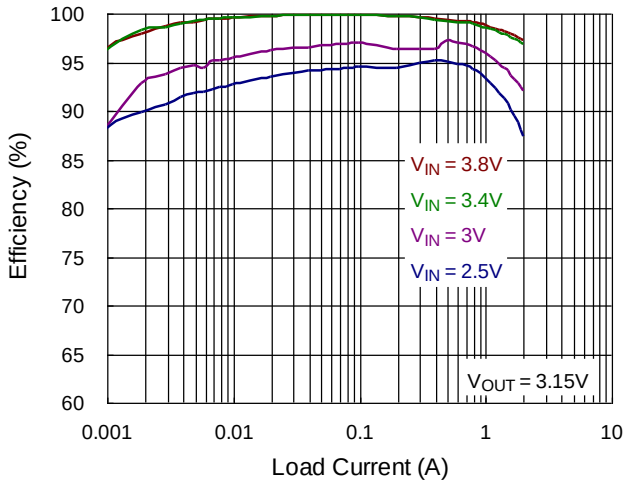
Table 1. BOM of Test Board

Reference	Part Number	Description	Package	Manufacturer
C_{IN} (Remote) (Note 7)	GRM31CR61C476ME44	47µF/16V/X5R	1206	Murata
C_{IN}	GRM188R61A106KE69	10µF/10V/X5R	0603	Murata
C_{OUT}	GRM188R61A226ME15D	22µF/10V/X5R	0603	Murata
L1	DFE252012F-R47M=P2	0.47µH	2520	Murata

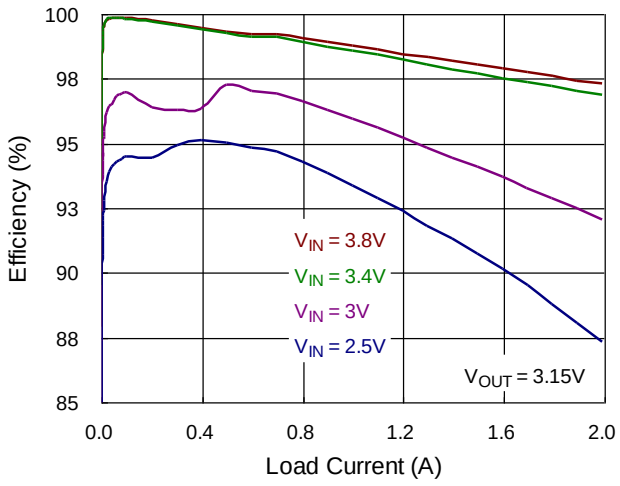
Note 7. Remote capacitors are utilized to mitigate the long wire effect, while also enhancing the output ripple.

14 Typical Operating Characteristics

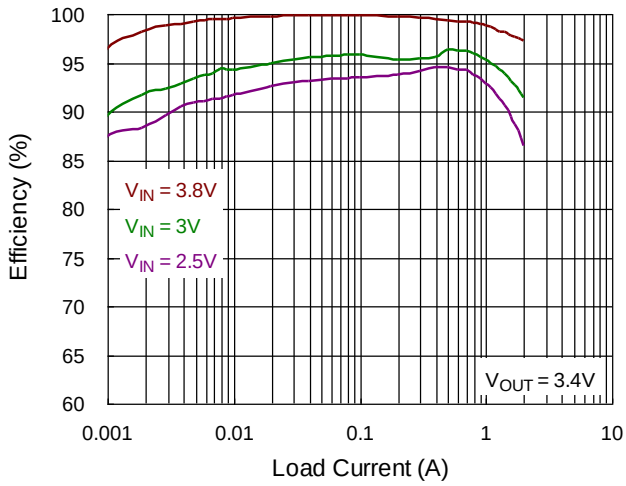
Efficiency vs. Load Current



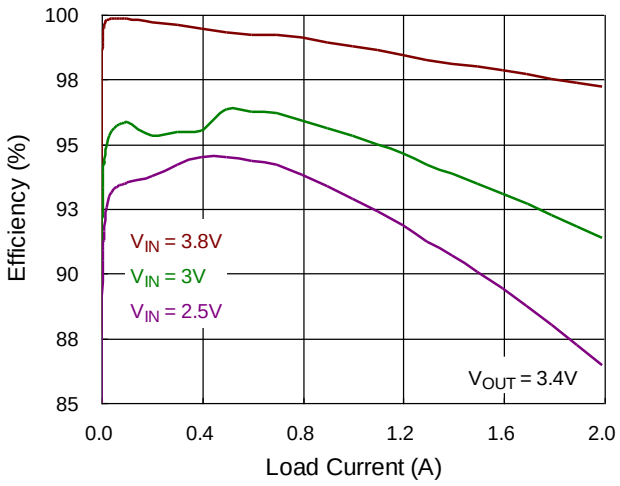
Efficiency vs. Load Current



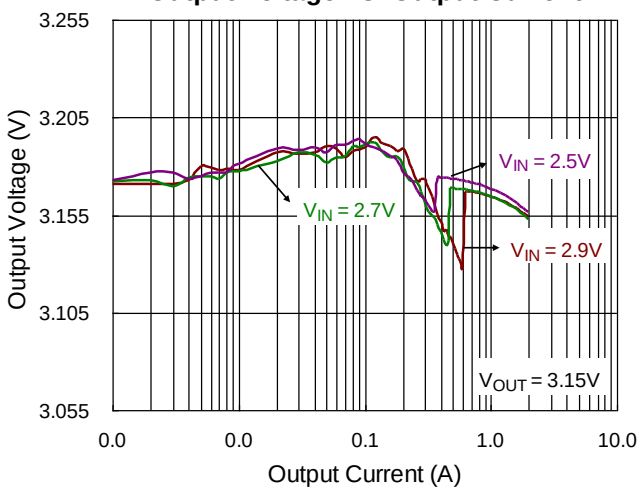
Efficiency vs. Load Current



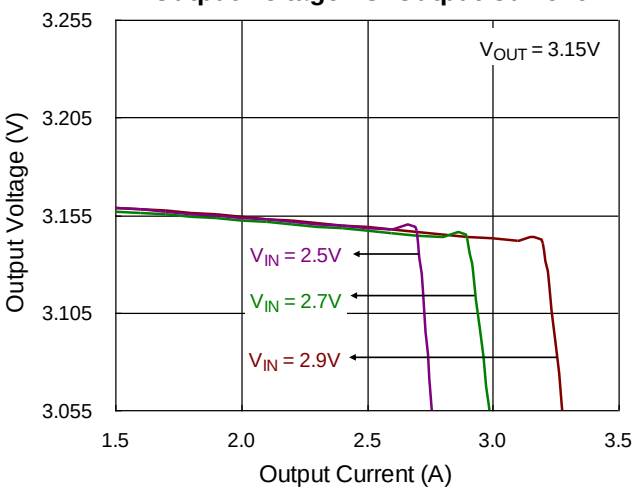
Efficiency vs. Load Current



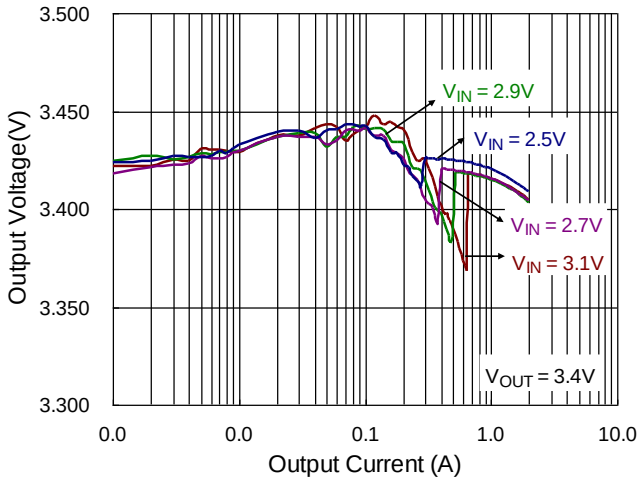
Output Voltage vs. Output Current



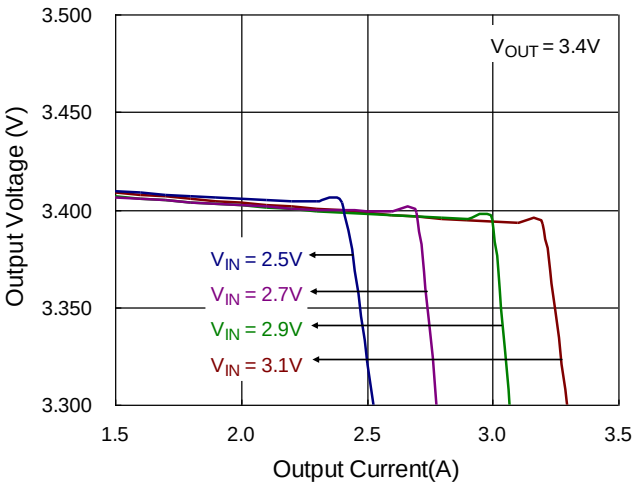
Output Voltage vs. Output Current



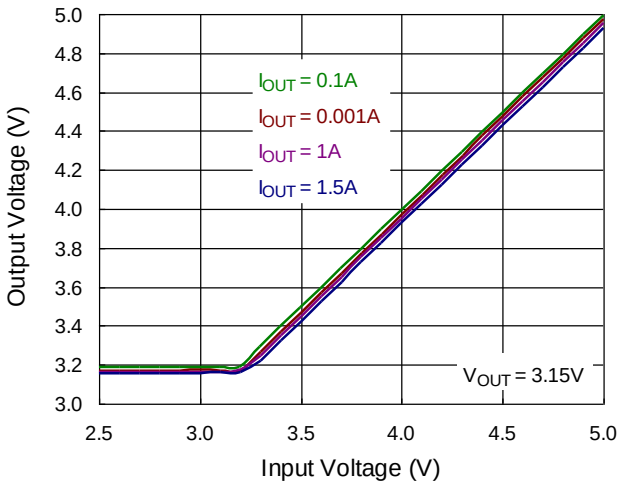
Output Voltage vs. Output Current



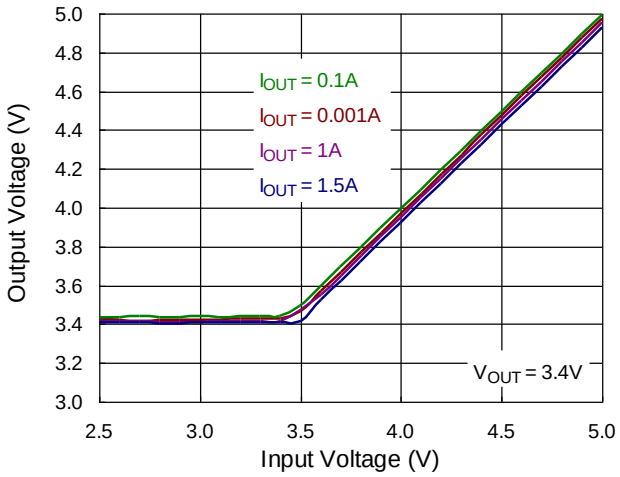
Output Voltage vs. Output Current



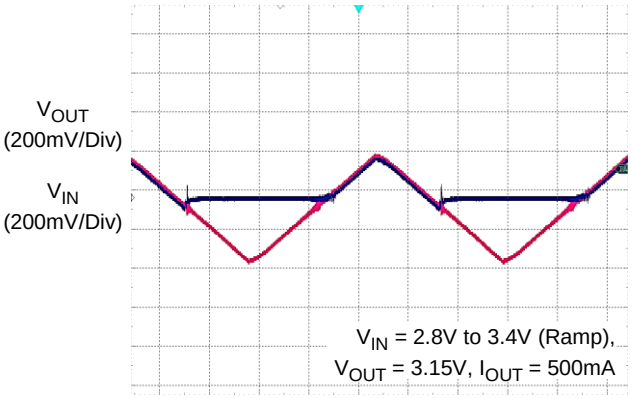
Output Voltage vs. Input Voltage



Output Voltage vs. Input Voltage

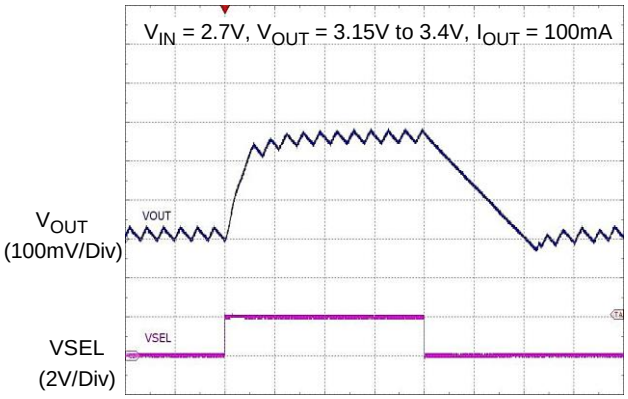


Boost to Bypass Mode Exit / Entry



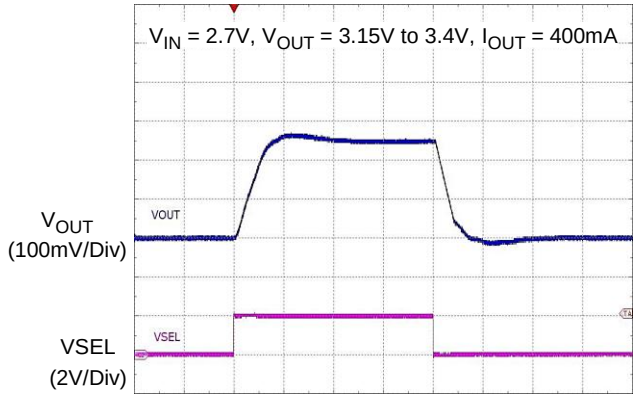
Time (400μs/Div)

VSEL Load Current



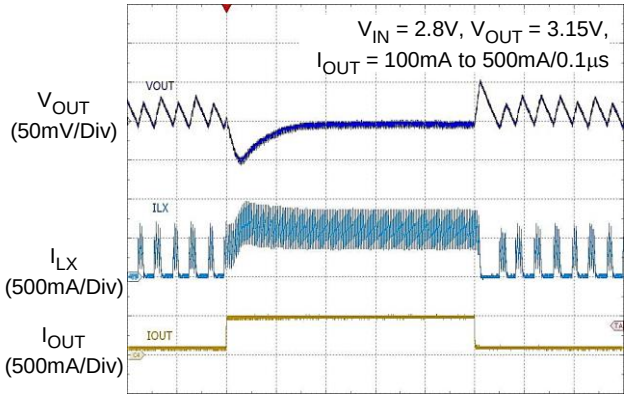
Time (20μs/Div)

VSEL Load Current



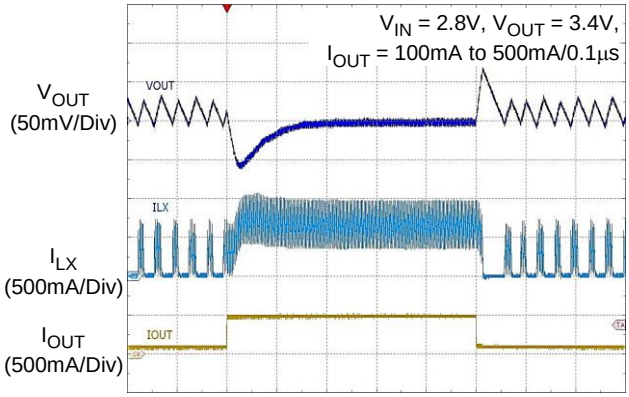
Time (20μs/Div)

Load Transient V_{OUT} = 3.15V



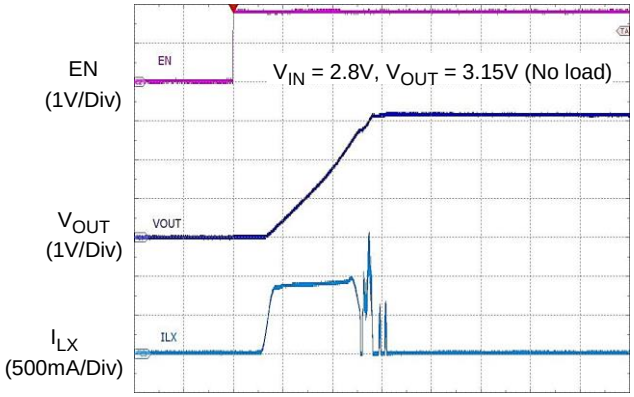
Time (20μs/Div)

Load Transient V_{OUT} = 3.4V



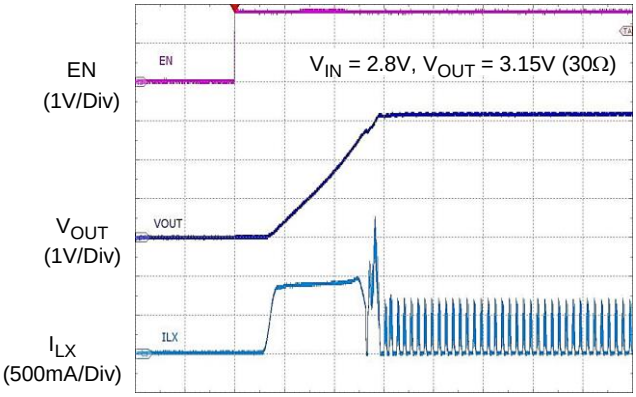
Time (20μs/Div)

Power On V_{OUT} = 3.15V (No Load)



Time (50μs/Div)

Power On V_{OUT} = 3.15V (30Ω)



Time (50μs/Div)

15 Operation

The RT4803B integrates built-in power transistors, synchronous rectification, and low supply current, delivering a compact solution for systems employing advanced Li-Ion battery chemistries. Under boost mode, it ensures output voltage regulation up to a maximum load current of 2000mA. Additionally, the quiescent current in Shutdown mode is less than 1μA, effectively maximizing battery life.

15.1 Undervoltage Lockout

The undervoltage lockout circuit safeguards against incorrect operation at low input voltages by preventing the converter from activating its power switches under undefined conditions. To enable the converter, the V_{IN} voltage must exceed the UVLO rising threshold. If the V_{IN} voltage drops below the UVLO falling threshold during operation, the converter is disabled until the supply surpasses the UVLO rising threshold. Moreover, the RT4803B automatically restarts if the input voltage recovers to the input voltage UVLO high level.

15.2 EN and nBYP

It is used for selecting operating modes. As described in Table 2, there are four device states. When both EN and nBYP are set to low, the device enters forced bypass mode with a low quiescent current (4μA). Pulling EN low and nBYP high places the device in shutdown mode, with a quiescent current of less than 1μA. If EN is set to high and nBYP to low, the device operates in forced bypass mode without the low quiescent current. When both EN and nBYP are set to high, the RT4803B operates in boost and auto-bypass modes.

Table 2

EN Input	nBYP Input	Mode Define	Device State
0	0	Forced bypass with low quiescent mode	The device operates in forced bypass with a low quiescent mode featuring a low quiescent current down to about 4μA (typical).
0	1	Shutdown mode	The device is in shutdown mode. The shutdown current is approximately about 1μA (max.).
1	0	Forced bypass without low quiescent mode	The device is active in forced bypass mode without the low quiescent mode. The device supply current is approximately about 15μA (typical).
1	1	Boost and auto bypass mode	The device includes boost and auto bypass modes, depending on whether V_{IN} is larger than V_{OUT}. The device supply current is approximately about 35μA (typical) in auto bypass mode and 55μA (typical) in boost mode.

15.3 Enable (nBYP = High Status)

The device's functionality can be enabled or disabled via the EN pin. When the EN pin exceeds the logic-high threshold, the device begins operating in accordance with the operation diagram in Figure 2, and the conditions outlined in Table 3. In shutdown mode, the converter ceases switching, and the internal control circuitry is deactivated. Consequently, the output voltage is diminished due to component consumption (such as Cap ESR), and no discharge function is active in this state. The discharge function is exclusively activated when the GPIO is set to a low status (with Reg.0x01[3] set to 0).

15.4 Soft-Start State

During the soft-start phase, if VOUT reaches 95% of V_{OUT_Target}, the RT4803B will transition into boost operation. Alternatively, if the count exceeds 512μs, the RT4803B will enter a fault state.

15.5 Boost/Auto Bypass Mode

When nBYP = H, two normal operation modes are available: boost mode and auto bypass mode. In boost mode, the RT4803B supplies power to the load through internal synchronous switches after the soft-start phase. In auto bypass mode, the input voltage is directly bypassed to the output terminal, enabling the RT4803B to deliver maximum current capacity. Detailed descriptions are provided as follows:

15.5.1 Boost Mode (Auto PFM/PWM Control Method)

To conserve power and enhance efficiency at low loads, the Boost operates in PFM (Pulse Frequency Modulation) as the inductor transitions into DCM (Discontinuous Current Mode). The switching frequency adjusts in proportion to the load to maintain output voltage regulation. As the load increases and the inductor current becomes continuous again, the Boost automatically reverts to PWM (Pulse Width Modulation) fixed frequency mode.

15.5.2 Auto Bypass Mode

The control loop will automatically transition to auto bypass mode if VIN exceeds VOUT. MOSFET Q3 will activate, causing MOSFETs Q1 and Q2 to turn off synchronously. Upon entering auto bypass mode, the MOSFET Q3 current limit is 4000mA (typical), as described in Figure 1.

15.5.3 Forced Bypass Mode

When nBYP is set to L, MOSFET Q3 activates, causing MOSFETs Q1 and Q2 to turn off, allowing the input voltage to pass directly to the output terminal. In forced bypass mode, the MOSFET Q3 current limit is 4000mA (typical), as described in Figure 1.

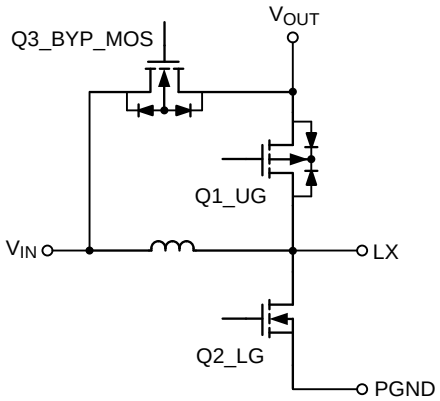


Figure 1. Boost Converter with Bypass Mode

15.6 LIN State

When V_{IN} > UVLO and EN transitions from low to high, the output capacitor undergoes linear startups until V_{IN} - V_{OUT} is less than 300mV (typical). The linear startups consist of LIN1 and LIN2 states. LIN1 pre-charge involves a 1000mA (typical) current with an 800μs duration, and the IC shifts to LIN2 pre-charge utilizing 2000mA (typical) for a 1600μs duration if V_{IN} – V_{OUT} remains greater than 300mV (typical). If V_{IN} – V_{OUT} is less than 300mV, the RT4803B enters soft-start operation after the linear startup (LIN1/2) states. Alternatively, if V_{IN} – V_{OUT} exceeds 300mV, the RT4803B transitions to a fault state.

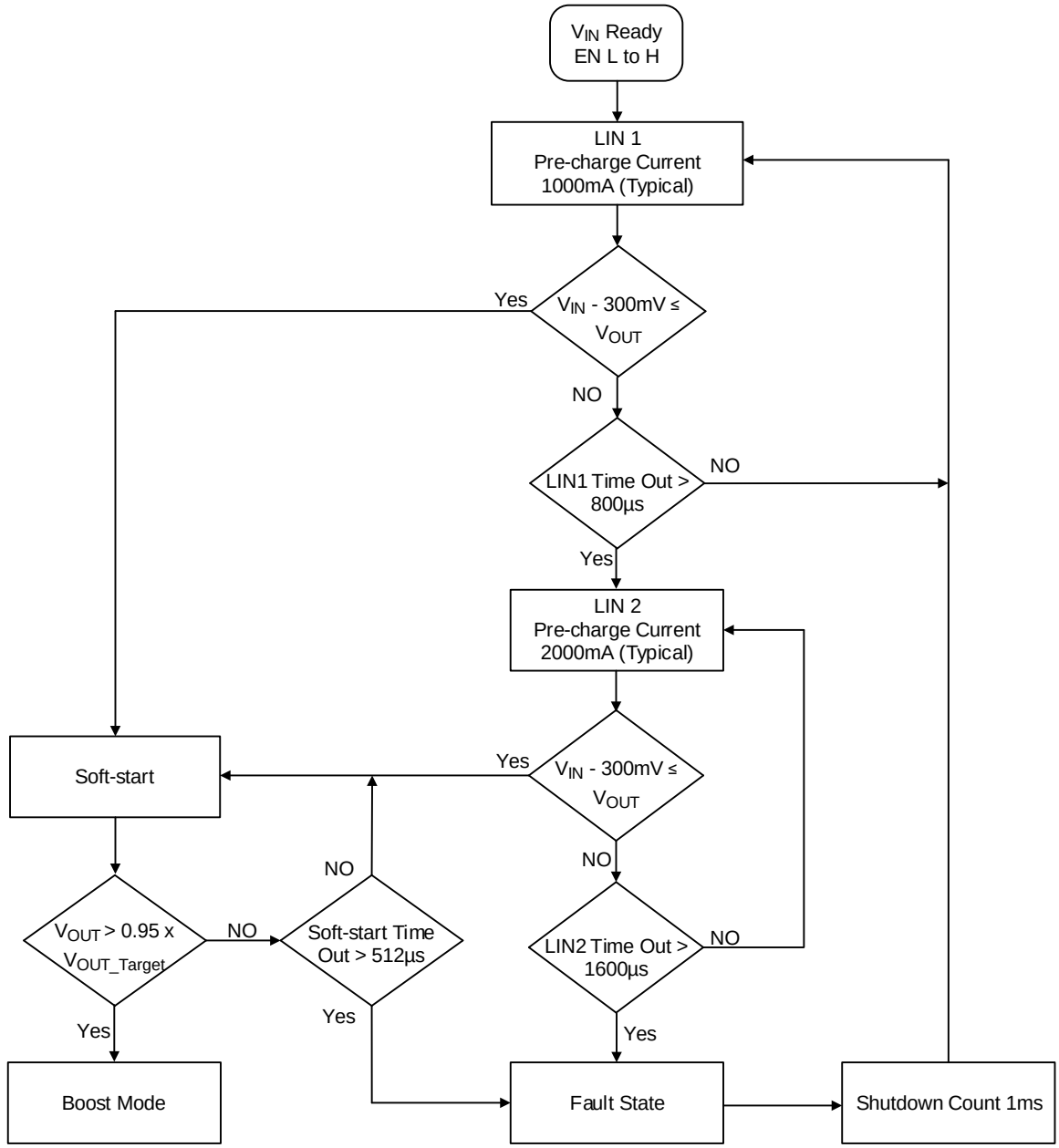


Figure 2. The RT4803B State Chart

Table 3

Mode	Description	Condition
LIN (Include LIN1/LIN2 States)	Linear Startup 1	$V_{IN} - 300mV \geq V_{OUT}$
	Linear Startup 2	
Soft-start	Boost Soft-start	$0.95 \times V_{OUT\_Target} > V_{OUT} \geq V_{IN} - 300mV$
Boost	Boost Mode	$V_{OUT\_Target} \geq 0.95 \times V_{OUT\_Target}$
Auto Bypass	Auto Bypass Mode	When $V_{IN} \geq V_{OUT}$, the control loop automatically transitions between auto bypass mode and boost mode.

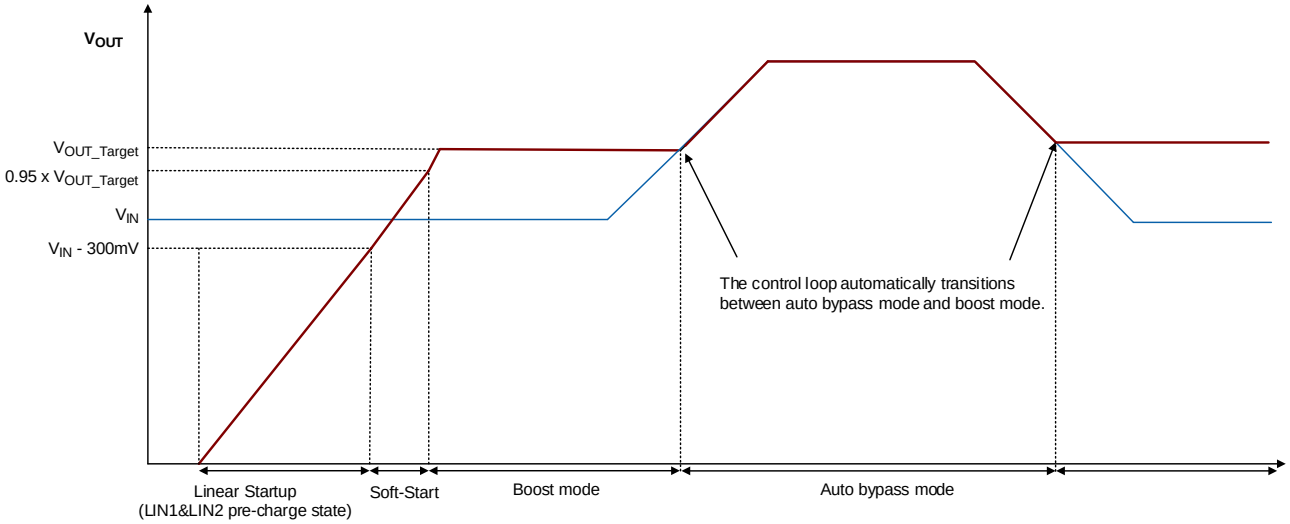


Figure 3. V_{OUT} Mode Transition Diagram with EN L to H and V_{IN} Variation (nBYP = H; I_O = 0A)

15.7 VSEL

To uphold a target minimum output voltage under challenging application conditions, such as full load transients, the output voltage set point can be dynamically increased by activating the VSEL input. This functionality also assists in mitigating voltage undershoot during line transients in worst-case scenarios. By default, the RT4803B has an output voltage setting of 3.15V when VSEL is set to L, and this can be programmed using Reg.0x02[4:0]. Additionally, when VSEL is set to H, the default output voltage setting is 3.4V, which can be programmed using Reg.0x03[4:0].

15.8 GPIO

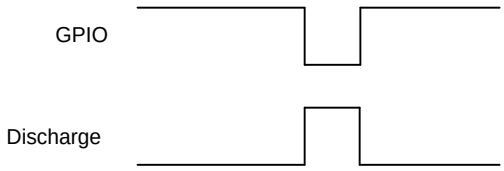
The GPIO can be configured to serve as either a mode selection or an nRST/nFAULT function, with control over the GPIO port configuration bit in Reg.0x01[3].

15.8.1 Reg.0x01[3] Setting 0:

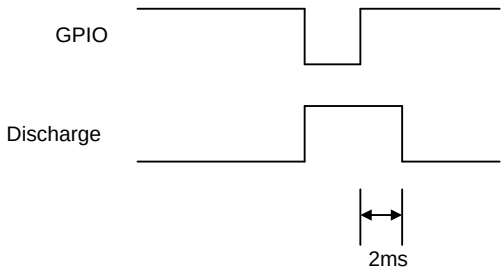
The GPIO supports for a manual reset input (nRST) and an interrupt generation output (nFAULT).

For the fault output (open-drain interrupt), the GPIO will pull low if a fault occurs. Meanwhile, the manual reset input allows the RT4803B to restart upon manual toggling, following the state chart in Figure 3.

Additionally, the RT4803B incorporates a discharge function, the activation of which relies on the setting of Reg.0x01[3]. This function is released 2ms after the GPIO goes high in all modes except shutdown mode. In shutdown mode, the function is immediately released when the GPIO goes high.



(a). In Shutdown Mode (EN = 0, nBYP = 1)



(b). In Other Modes

Figure 4. Discharge Function Diagram

15.8.2 Reg.0x01[3] Setting 1:

To configure the GPIO pin as the input for device mode selection, the following settings should be applied:

- MODE_CTRL[1:0] in Register 0x01[1:0] should be set to 2'b00.
- GPIOCFG in Register 0x01[3] should be set to 1'b1.

With these configurations in place:

- When the GPIO pin is set to Low, the device will operate in Auto PFM/PWM mode.
- When the GPIO pin is set to High, the device will operate in Forced PWM control mode.

15.9 Current Limit

The RT4803B utilizes a valley-current limit detection scheme to monitor the inductor current during the off-time. When the load current exceeds the valley current-limit threshold, the off-time is extended until the current decreases to the valley-current threshold. Subsequently, the next on-time commences once the current has decreased to the valley-current threshold. The on-time is determined by the (V_{OUT} – V_{IN}) / V_{OUT} ratio. If the load current continues to increase, the output voltage will decrease. The current limit function is implemented using this scheme, as described in the provided figure.

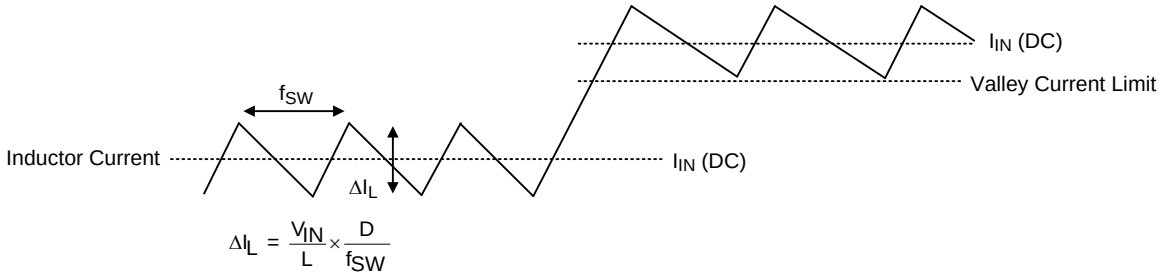


Figure 5. Inductor Currents in Current Limit Operation

15.10 OTP

The converter incorporates over-temperature protection. If the junction temperature exceeds the thermal shutdown rising threshold, the system will enter a latch state, and the output voltage regulation will cease until the junction temperature falls below the falling threshold.

15.11 OVP

The device does not operate when the input voltage (V_{IN}) exceeds the overvoltage protection (OVP) level, set at 5.7V. A typical 100mV hysteresis is implemented to prevent unstable on/off behavior. If the input voltage exceeds 5.7V, the IC will shut down until the voltage level decreases to below 5.6V, at which point the device will return to normal operation. The OVP protection serves to prevent the IC from operating under abnormal input power conditions and protect the device from potential damage.

15.12 UVP

To mitigate the risk of large power dissipation that could potentially damage the IC during abnormal operation, the RT4803B employs Undervoltage Protection (UVP). If the output voltage (V_{OUT}) drops below 80% of the targeted output voltage, the IC will enter shutdown mode upon triggering a fault signal. After the fault state has persisted for 1ms, the IC will resume operation once the abnormal state is resolved.

15.13 Fault State

The fault state will be triggered under the following conditions:

1. Linear startup failure
2. Soft-start failure
3. Undervoltage Protection (UVP)
4. Over-Temperature Protection (OTP)

Upon the occurrence of a fault state, the IC will enter shutdown for 1ms. Following the completion of the 1ms count, the IC will restart. The state chart portraying the operation of the RT4803B is illustrated in Figure 2.

15.14 Protection

Certainly, below is a table describing the protection actions for the RT4803B:

Protection Type	Threshold Refer to Electrical Spec.	Protection Method	Shut Down Delay Time	Reset Method
OCP	I_L > 4A	Turn On UG	Without Shutdown Behavior	I_L < 4A
OVP	V_{IN} > 5.7V	Turn Off UG, LG, BYP_MOS	No Delay	V_{IN} < 5.6V
UVLO	V_{IN} < 1.6V (max)	Turn Off UG, LG, BYP_MOS	No Delay	V_{IN} > 1.8V (max)
OTP	TEMP > 160°C	Turn Off UG, LG, BYP_MOS	No Delay	OTP Hysteresis = 20°C
UVP	V_{OUT} < 0.8 x V_{OUT_Target}	Turn Off UG, LG, BYP_MOS	2ms	V_{OUT} > 0.8 x V_{OUT_Target}

16 Application Information

(Note 8)

16.1 Boost Output Current Capacity

The RT4803B device incorporates a valley inductor current limit and a max duty cycle limit scheme. In boost mode, the current-limit threshold can be adjusted via an I^2C register. While the current limit is programmable, the output current capacity is constrained by the maximum duty cycle design. Therefore, it is essential that the duty cycle in the first application be smaller than the max duty cycle to ensure the maximum continuous output current (IOUTMAX) is not exceeded.

$$1 - \frac{V_{IN}}{V_{OUT}} = \text{Duty} < 40\% \,(\text{max duty cycle limit})$$

If application condition duty cycle smaller than max duty cycle limit, that max output capacity can be calculate as below equation:

$$I_{OUT_{MAX}} = \frac{V_{IN}}{V_{OUT}} \times \eta \times I_{IN_{MAX}}$$

($I_{IN_{MAX}}$ about equal $I_{L_{\text{valley current limit level}}}$)

16.2 Inductor Selection

The choice of inductor value significantly impacts transient, ripple, and overall performance. The RT4803B recommends a nominal inductance value of 0.47μH to achieve superior performance.

Since the inductor peak current varies based on the load, it is prudent to select an inductor with a saturation current rating higher than the peak current of the application flowing through the power switches. Opting for an inductor with a low DCR is advised to enhance performance and efficiency for the application. Careful consideration of the inductor's saturation current is necessary, taking into account the current limit (4500mA max default level).

The peak current of the application can be estimated using the following equation:

$$I_{LPEAK_{MAX}} = \frac{V_{IN} \times D}{2 \times L \times f_{SW}} + \frac{I_{OUT_{MAX}} \times V_{OUT}}{V_{IN} \times \eta}$$

16.3 Input Capacitor Selection

The steady-state and transient response operation performance of the RT4803B is influenced by the stability of the input voltage. To prevent input voltage instability during operation, it is recommended to use a minimum of a 10μF input capacitor. It is advisable to place this capacitor as close as possible to the VIN and GND pins of the IC.

Furthermore, it is important to consider the potential impact of the "long wire" effect, which can result in instability in boost converter operation. To mitigate this effect and improve system stability, the usage of a remote input capacitor of 47μF is suggested.

16.4 Output Capacitor Selection

The ripple voltage, which is a crucial factor in selecting the output capacitor, consists of two components. The first component is the product of the ripple current with the ESR (Equivalent Series Resistance) of the output capacitor. The second component is formed by the charging and discharging process of the output capacitor. This comprehensive understanding of the ripple voltage is essential in accurately choosing an appropriate output capacitor for the RT4803B.

Output capacitor is selected according to output ripple which is calculated as below equation.

$$\Delta V_{OUT} = \Delta V_{ESR} + \Delta V_{OUT_{CAP}}$$

$$\Delta V_{ESR} = I_{C_{RMS}} \times R_{C_{ESR}}$$

$$\Delta V_{OUT_{CAP}} = \frac{I_{OUT} \times Duty}{f_{SW} \times C_{MIN}}$$

Users can use the equation to choose a capacitor that meets the systems ripple specifications. It is recommended to use at least 22μF x 3 capacitors to match the application's V_{OUT} ripple requirements and ensure stability performance.

16.5 Register Table Lists

Slave address = 1110101 (0x75)

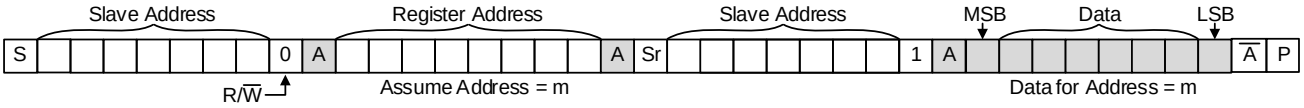
Name	Address	Description
CONFIG	0x01	MODE control and spread modulation control
VOUTFLOOR	0x02	VSEL = L output voltage programmable register address
VOUTROOF	0x03	VSEL = H output voltage programmable register address
ILIMSET	0x04	Set current limit and soft-start current limit
STATUS	0x05	Read IC status

16.6 I^2C Interface

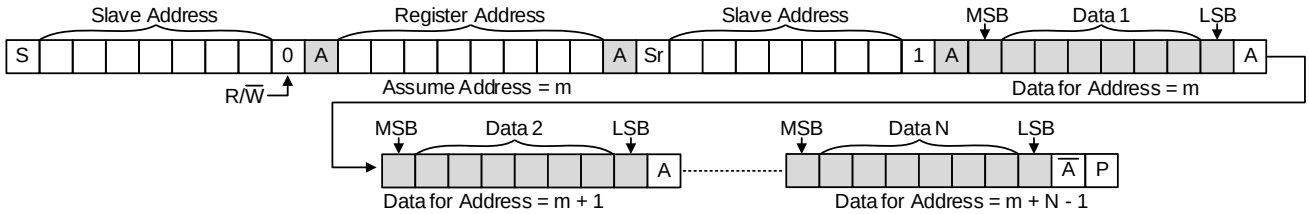
The RT4803B I^2C slave address is 1110101 (7bits). The I^2C interface supports fast mode (bit rate up to 400kb/s).

The write or read bit stream (N ≥ 1) is shown below:

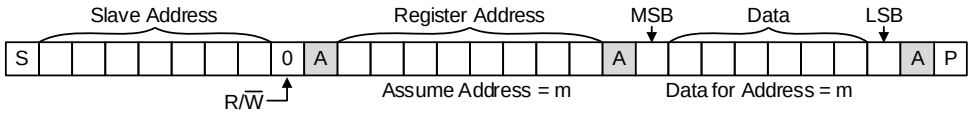
Read a single byte of data from Register



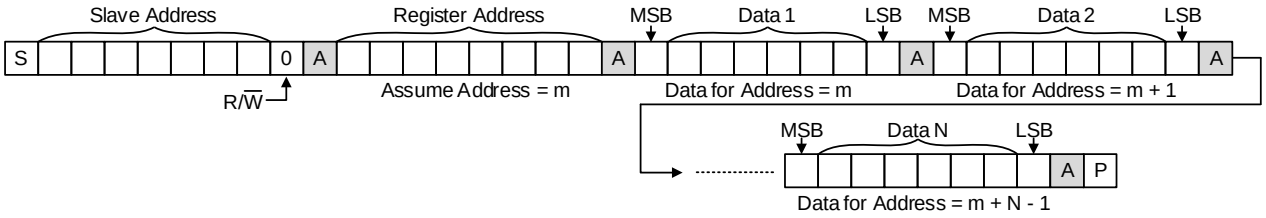
Read N bytes of data from Registers



Write a single byte of data to Register

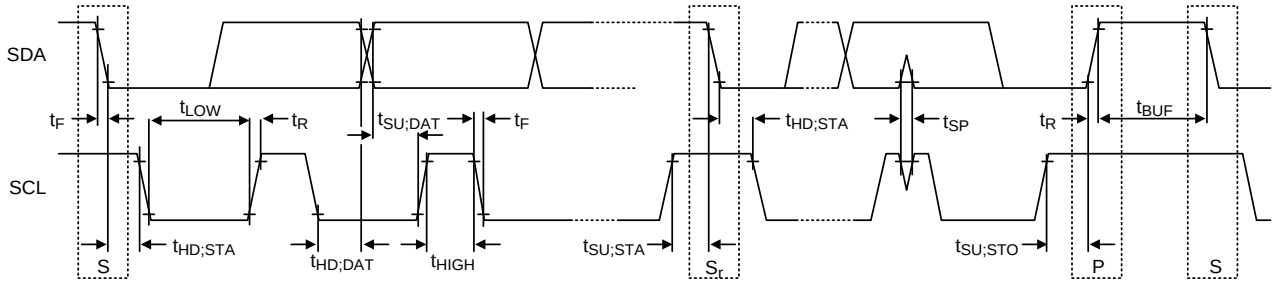


Write N bytes of data to Registers



Driven by Master, Driven by Slave, P Stop, S Start, Sr Repeat Start

16.7 I²C Waveform Information



16.8 Thermal Considerations

For continuous operation, it is essential to ensure that the absolute maximum junction temperature is not exceeded. The maximum power dissipation is influenced by factors such as the thermal resistance of the IC package, PCB layout, surrounding airflow rate, and the temperature differential between the junction and ambient conditions. The maximum power dissipation can be calculated using the following formula:

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

For recommended operating condition specifications, the maximum junction temperature is 125°C. The junction to ambient thermal resistance, θ_{JA}, is layout dependent. For the WL-CSP-16B 1.67x1.67 (BSC) package, the thermal resistance, θ_{JA}, is 47.7°C/W on a standard JEDEC 51-7 four-layer thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by the following formula:

$P_{D(MAX)}$ = (125°C – 25°C) / (47.7°C/W) = 2.09W for a WL-CSP-16B 1.67x1.67 (BSC) package

The maximum power dissipation depends on the operating ambient temperature for a fixed $T_{J(MAX)}$ and thermal resistance, θ_{JA}. The derating curve in Figure 6 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

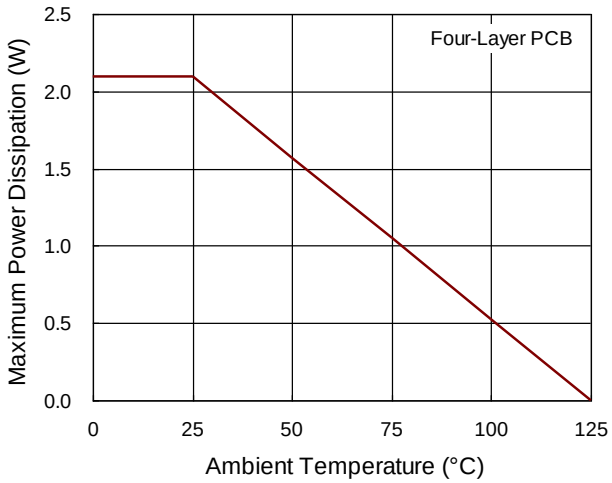


Figure 6. Derating Curve of Maximum Power Dissipation

16.9 Layout Considerations

The PCB layout plays a crucial role in maintaining the high performance of the RT4803B. Both the high current and fast switching nodes require careful attention in the PCB layout to ensure the robustness of the RT4803B. An improper layout could result in poor line or load regulation, ground and output voltage shifts, stability issues, unsatisfactory EMI behavior, or reduced efficiency. To achieve the best performance from the RT4803B, it is essential to strictly adhere to the following PCB layout guidelines:

- Place the input and output capacitors as close as possible to the input and output pins respectively for good filtering.
- For thermal considerations, it is necessary to maximize the pure area for the power stage area, especially around the LX pin.

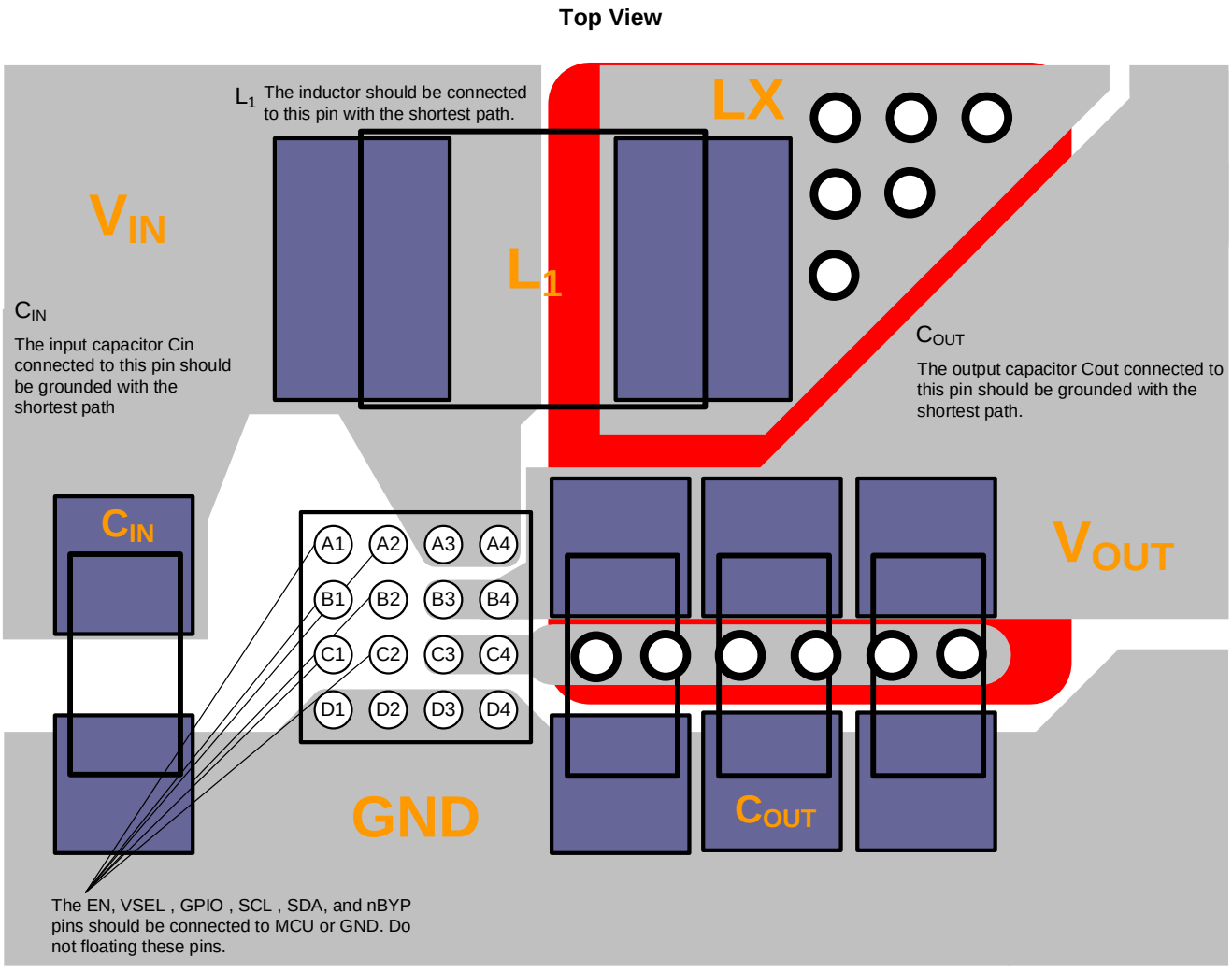


Figure 7. PCB Layout Guide

Note 8. The information provided in this section is for reference only. The customer is solely responsible for the designing, validating, and testing your product incorporating Richtek's product and ensure such product meets applicable standards and any safety, security, or other requirements.

17 Functional Register Description

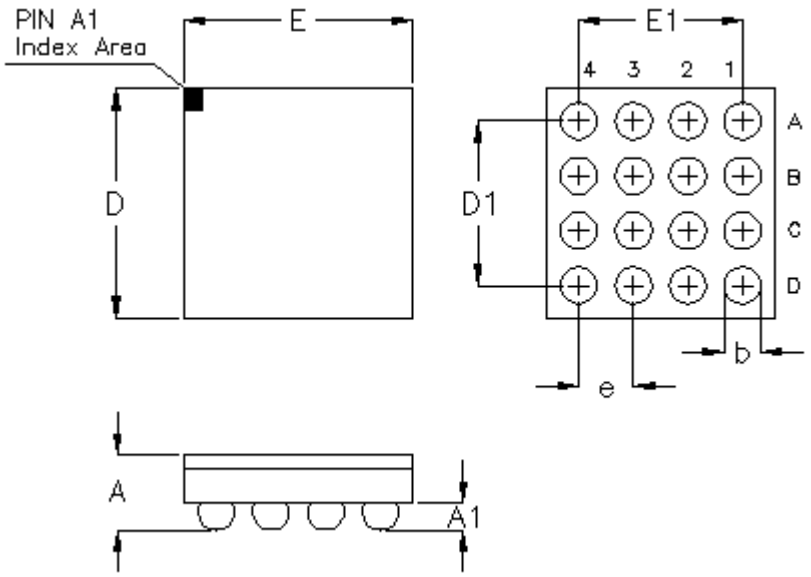
Address 0x01		CONFIG						
Bits	7	6	5	4	3	2	1	0
Name	RESET	ENABLE[1:0]		Reserved	GPIOCFG	SSFM	MODE_CTRL[1: 0]	
Reset	0	0	0	0	0	0	0	1
Type	RW	RW	RW	RW	RW	RW	RW	RW
Address 0x02		**VOUTFLOOR**						
Bits	7	6	5	4	3	2	1	0
Name	Reserved			VOUT[4:0]				
Reset	0	0	0	0	0	1	1	0
Type	RW	RW	RW	RW	RW	RW	RW	RW
Address 0x03		**VOUTROOF**						
Bits	7	6	5	4	3	2	1	0
Name	Reserved			VOUT[4:0]				
Reset	0	0	0	0	1	0	1	1
Type	RW	RW	RW	RW	RW	RW	RW	RW
Address 0x04		**ILIMSET**						
Bits	7	6	5	4	3	2	1	0
Name	Reserved		ILIM_OFF	SOFT_START	ILIM[3:0]			
Reset	0	0	0	1	1	1	0	1
Type	RW	RW	RW	RW	RW	RW	RW	RW
Address 0x05		**STATUS**						
Bits	7	6	5	4	3	2	1	0
Name	TSD	HOTDIE	DCDCMODE	OPMODE	ILIMPT	ILIMBST	FAULT	PGOOD
Reset	0	0	0	0	0	0	0	0
Type	R	R	R	R	R	R	R	R

Addr	Reg Name	Bit	Bit Name	Default	Type	Description
0x01	CONFIG	7	RESET	0	R/W	0: Normal operation (Default) 1: All registers are reset to default value.
		6:5	ENABLE[1:0]	00	R/W	00: Device operation follows hardware control signal. (Refer to Table 2) (Default) 01: Device operation in auto transition mode (boost/auto pass) regardless of the nBYP control signal. (EN = 1) 10: Device is forced in bypass mode regardless of the nBYP control signal. (EN = 1) 11: Device is in shutdown mode. Regardless of the nBYP control signal. (EN = 1)
		4	Reserved	0	R/W	Reserved
		3	GPIOCFG	0	R/W	0: GPIO port is configured to support manual reset input (nRST) and interrupt generation output (nFAULT). (Default) 1: GPIO port is configured as a device mode selection input.
		2	SSFM	0	R/W	0: Spread spectrum modulation is disabled. (Default) 1: Spread spectrum modulation is enabled in PWM mode.
		1:0	MODE_CTRL[1:0]	01	R/W	00: Device operation follows hardware control signal (GPIO must be configured as mode select input). 01: PFM with automatic transition into PWM operation. (Default) 10: Forced PWM operation. 11: PFM with automatic transition into PWM operation (VSEL = L), forced PWM operation. (VSEL = H).

Addr	Reg Name	Bit	Bit Name	Default	Type	Description
0x02	VOUTFLOOR	7:5	Reserved	000	R/W	Reserved
		4:0	VOUT[4:0]	00110	R/W	00000: V_{OUT} = 2.85V 00001: V_{OUT} = 2.9V 00010: V_{OUT} = 2.95V 00011: V_{OUT} = 3V 00100: V_{OUT} = 3.05V … 00110: V_{OUT} = 3.15V (Default) … 11111: V_{OUT} = 4.4V
0x03	VOUTROOF	7:5	Reserved	000	R/W	Reserved
		4:0	VOUT[4:0]	01011	R/W	00000: V_{OUT} = 2.85V 00001: V_{OUT} = 2.9V 00010: V_{OUT} = 2.95V 00011: V_{OUT} = 3V 00100: V_{OUT} = 3.05V … 01011: V_{OUT} = 3.4V (Default) … 11111: V_{OUT} = 4.4V
0x04	ILIMSET	7:6	Reserved	00	R/W	Reserved
		5	ILIM_OFF	0	R/W	0: Current limit enabled (Default) 1: Current limit disabled
		4	SOFT_START	1	R/W	0: Boost soft-start current is limited per ILIM bit settings. (EN L to H with V_{IN} ready state) 1: Boost soft-start current is limited to ca. 1250mA inductor valley current. (Default) (EN L to H with V_{IN} ready state)
		3:0	ILIM[3:0]	1101	R/W	1000: 1500mA 1001: 2000mA 1010: 2500mA 1011: 3000mA 1100: 3500mA 1101: 4000mA (Default) 1110: 4500mA 1111: 5000mA

Addr	Reg Name	Bit	Bit Name	Default	Type	Description
0x05	STATUS	7	TSD	0	R	0: Normal operation (Default) 1: Thermal shutdown tripped. The flag is reset after readout.
		6	HOTDIE	0	R	0: T_J < 90°C (Typ.) (Default) 1: T_J > 100°C (Typ.)
		5	DCDCMODE	0	R	0: Device operates in PFM mode. (Default) 1: Device operates in PWM mode.
		4	OPMODE	0	R	0: Device operates in forced bypass mode. (Default) 1: Device operates in DC-DC mode.
		3	ILIMPT	0	R	0: Normal operation (Default) 1: Indicates that the bypass FET current limit has triggered. This flag is reset after readout.
		2	ILIMBST	0	R	0: Normal operation (Default) 1: Indicates that the valley input current limit has triggered. This flag is reset after readout.
		1	FAULT	0	R	0: Normal operation (Default) 1: Indicates that a fault condition has occurred. This flag is reset after readout.
		0	PGOOD	0	R	0: Indicates the output voltage is out of regulation. (Default) 1: Indicates the output voltage is within its nominal range. This bit is set if the converter is forced in pass-through.

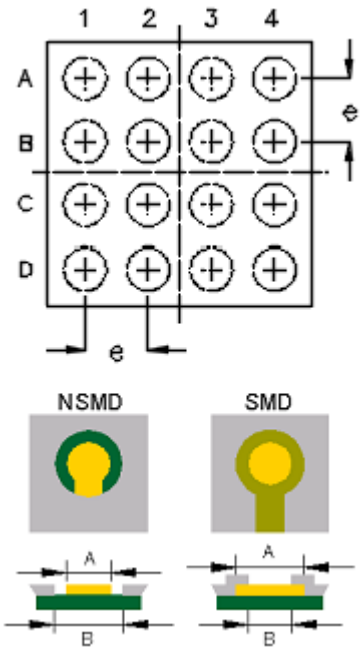
18 Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.500	0.600	0.020	0.024
A1	0.170	0.230	0.007	0.009
b	0.240	0.300	0.009	0.012
D	1.620	1.720	0.064	0.068
D1	1.200		0.047	
E	1.620	1.720	0.064	0.068
E1	1.200		0.047	
e	0.400		0.016	

WL-CSP-16B 1.67x1.67 (BSC)

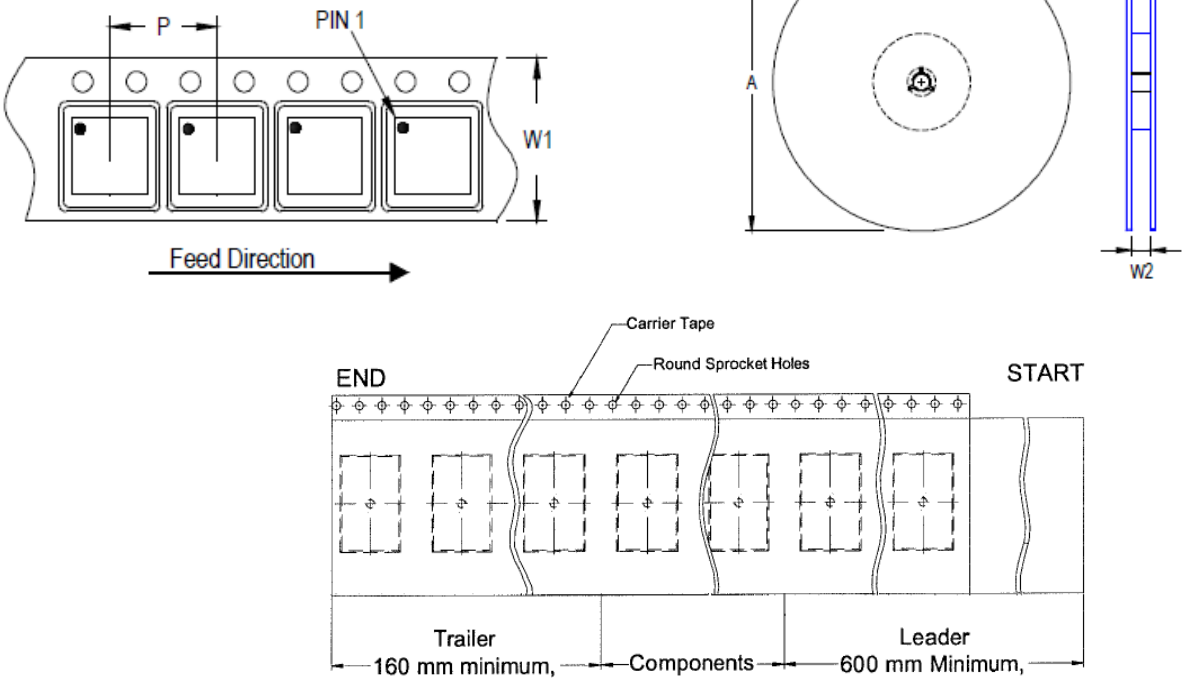
19 Footprint Information



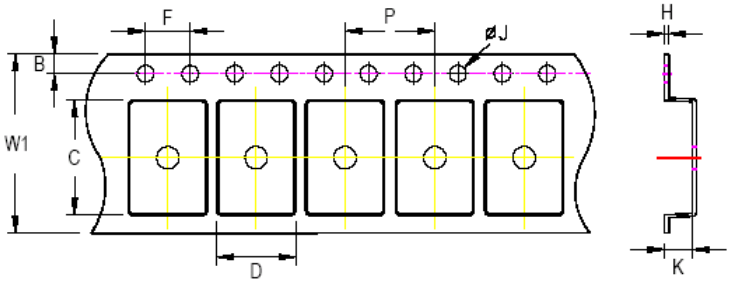
Package	Number of Pin	Type	Footprint Dimension (mm)			Tolerance
			e	A	B	
WL-CSP1.67*1.67-16(BSC)	16	NSMD	0.400	0.240	0.340	±0.025
		SMD		0.270	0.240	

20 Packing Information

20.1 Tape and Reel Data



Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min./Max. (mm)
			(mm)	(in)				
WL-CSP 1.67x1.67	8	4	180	7	3,000	160	600	8.4/9.9



C, D, and K are determined by component size. The clearance between the components and the cavity is as follows:

- For 8mm carrier tape: 0.5mm max.

Tape Size	W1	P		B		F		ØJ		H
	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Max.
8mm	8.3mm	3.9mm	4.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	0.6mm

20.2 Tape and Reel Packing

Step	Photo/Description	Step	Photo/Description
1	 Reel 7”	4	 12 inner boxes per outer box
2	 Packing by Anti-Static Bag	5	 Outer box **Carton A**
3	 3 reels per inner box **Box A**	6	

Container / Package	Reel		Box			Carton		
	Size	Units	Item	Reels	Units	Item	Boxes	Unit
WL-CSP 1.67x1.67	7”	3,000	Box A	3	9,000	Carton A	12	108,000
			Box E	1	3,000	For Combined or Partial Reel.		

20.3 Packing Material Anti-ESD Property

Surface Resistance	Aluminum Bag	Reel	Cover tape	Carrier tape	Tube	Protection Band
Ω/cm^2	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**

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21 Datasheet Revision History

Version	Date	Description	Item
00	2024/5/7	Final	Marking Information on P2 Typical Application Circuit on P9 Application Information on P23 Packing Information on P31