Triple-Channel PWM Controller with I²C Interface for IMVP9.2 CPU Core Power Supply

1 General Description

The RT3638AJ is an IMVP9.2 compliant CPU power controller which includes three voltage rails: an 8-phase synchronous buck controller for the VCCCORE VR, a single-phase synchronous buck controller for the VCCGT VR, and a single-phase synchronous buck controller for VCCSA VR. The output of each rail can be configured to support desired phase assignments up to a maximum of 8 phases for VCCCORE, single phase for VCCGT, and single phase for VCCSA. For example, the RT3638AJ supports output operations, such as 8+1+1, 7+1+1, 6+1+1. The RT3638AJ supports the Smart Phase Management (SPM) feature, to achieve maximum efficiency in all load ranges. Thresholds for automatic phase addition or removal are user-programmable via the I²C protocol interface. The RT3638AJ adopts G-NAVP™ (Green Native AVP), Richtek's proprietary topology derived from the finite DC gain of the EA amplifier with current mode control. This topology simplifies droop setting to meet all Intel CPU requirements for AVP (Adaptive Voltage Positioning). Based on the G-NAVP™ topology, the RT3638AJ features a new generation of quick response mechanism (Adaptive Quick Response, AQR) to optimize AVP performance during load transients and reduce output capacitors. The RT3638AJ supports mode transition functions with various operating states.

A serial VID (SVID) interface is built in to communicate with Intel IMVP9.2 compliant CPUs. The RT3638AJ offers built-in non-volatile memory (NVM) for platform setting functions, such as ICCMAX, switching frequency, or AQR trigger levels. The RT3638AJ provides VR ready output signals. It also features complete fault protection functions, including overvoltage (OV), overcurrent (OC), undervoltage (UV), and undervoltage lockout (UVLO). The RT3638AJ is available in a WQFN-68L 8x8 package. The recommended junction temperature range is from –40°C to 125°C.

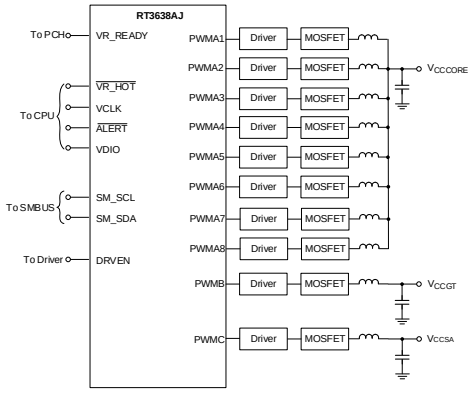
2 Features

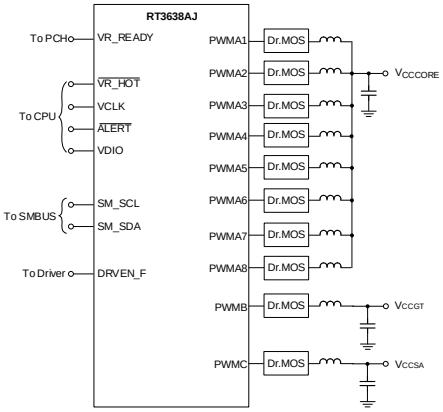
- **Intel IMVP9.2 Compliant**
- **8/7/6/5/4/3/2/1/0 Phase (VCCCORE VR) + 1/0 Phase (VCCGT VR) + 1/0 Phase (VCCSA VR) PWM Configuration**
- **Support SPS with Current Sensing by Either Current Type or Voltage Type**
- **Support 1 PWM Drive 2 Power Stage and Phase Doubler RT9637 for Core Rail Up to 16-Phase Operation**
- **Easy-Set G-NAVP™ Control**
- **0.5% DAC Accuracy**
- **Differential Remote Voltage Sense**
- **Internal Non-Volatile Memory to Store Custom Configuration**
- **Accurate Current Balance**
- **Diode Emulation Mode at Light-Load Condition**
- **Fast Transient Response-Adaptive Quick Response**
- **VR Ready Indicator**
- **Output Current Monitoring**
- **Protection Flag for OVP, OCP, and UVP**
- **Switching Frequency Setting**
- **Slew Rate Setting**
- **DVID Enhancement**
- **Acoustic Noise Suppression Function**
- **Support Fast V-Mode (FVM)**
- **Zero Loadline**
- **Rail Disable**
- **Smart Phase Management Adjustment**
- **Standard I²C Protocol Interface**
  - **Thermal Balance Adjustment**
- **Soldering Good Detection**
- **Small 68-Lead WQFN Package**

3 Applications

- IMVP9.2 Intel Core Power Supply
- Desktop/Notebook Computers
- AVP Step-Down Converters

4 Simplified Application Circuit





5 Ordering Information

RT3638AJ □□-□

- The configuration code identifier for the register setting stored in the internal NVM
- Package Type
  QW: WQFN-68L 8x8 (W-Type)
- Lead Plating System
  G: Richtek Green Policy Compliant(1)

Note 1.

Richtek products are Richtek Green Policy compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.

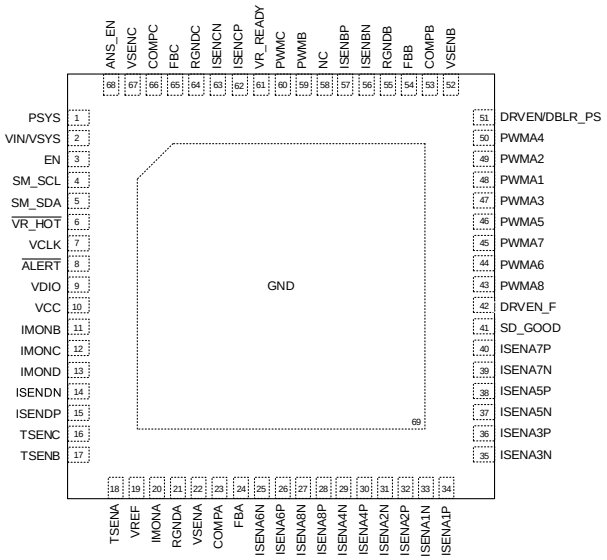
6 Marking Information

RT3638AJGQW : Product Code
YMDAN : Date Code

Table of Contents

7 Pin Configuration

(TOP VIEW)



WQFN-68L 8x8

8 Functional Pin Description

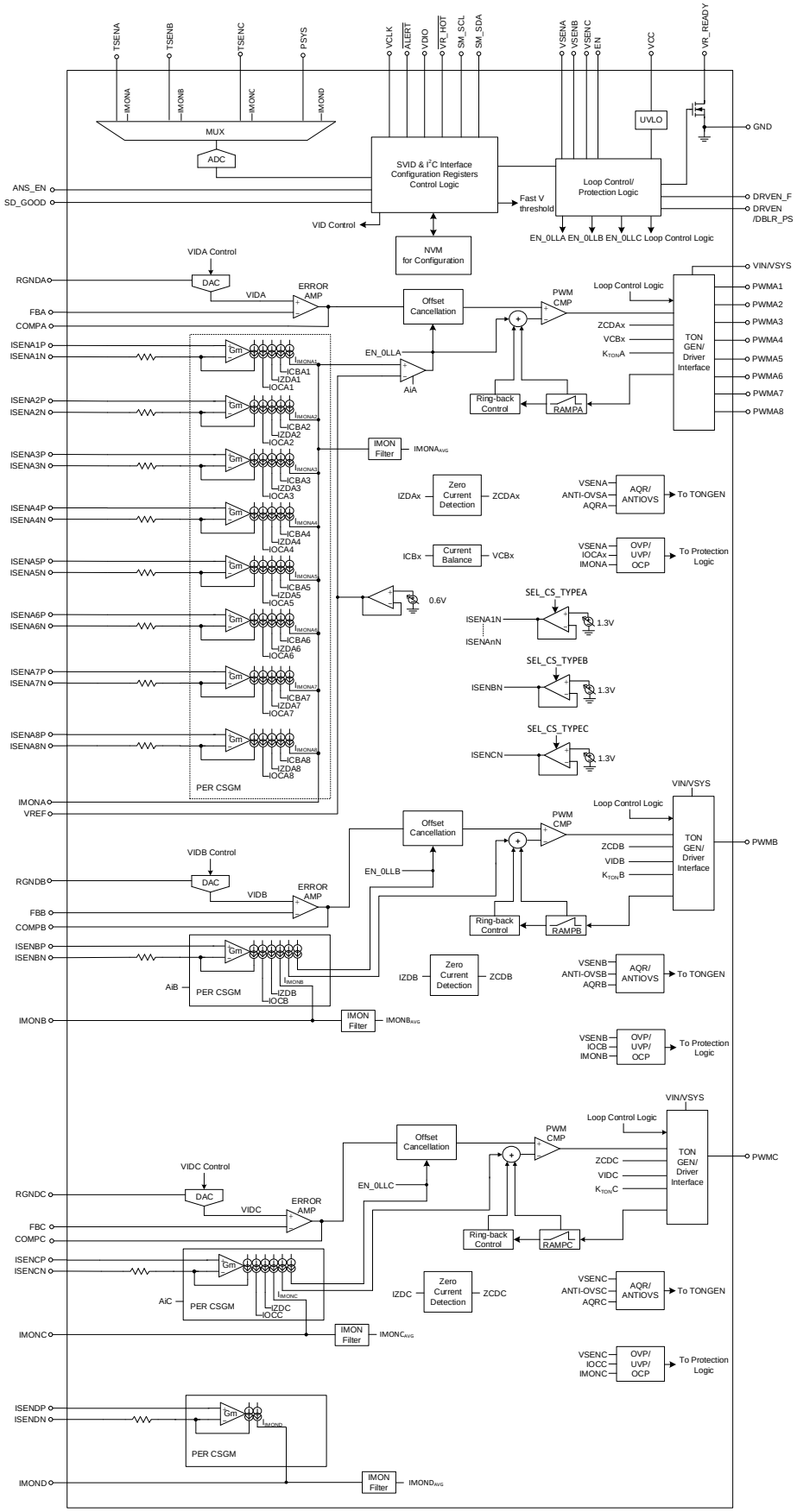
Pin No.	Pin Name	Pin Function
1	PSYS	System input power monitor. Place the PSYS resistor as close to the IC as possible. The PSYS function can be disabled by setting the voltage at the PSYS pin > (VCC – 0.5V). If the platform does not support the PSYS function, it is recommended to connect the PSYS pin to GND to avoid affecting system performance. The full scale 1.6V/3.2V of PSYS is programmable via the configuration register in NVM.
2	VIN/VSYS	Input voltage pin. Connect a low-pass filter of which time constant is at the switching frequency to this pin for setting on-time.
3	EN	VR enable control input.
4	SM_SCL	Clock input for the I^2C interface. If the I^2C communication is not used, connect the SM_SCL and SM_SDA pins to higher than 3.3V to achieve power saving.
5	SM_SDA	Data line for the I^2C interface. If the I^2C communication is not used, connect the SM_SCL and SM_SDA pins to higher than 3.3V to achieve power saving.
6	$\overline{\text{VR\_HOT}}$	Thermal monitor output. (Active low).
7	VCLK	Synchronous clock from the CPU.
8	$\overline{\text{ALERT}}$	SVID alert. (Active low).
9	VDIO	VR and CPU data transmission interface.
10	VCC	Controller power supply. Connect this pin to 5V and place an RC filter, R = 1Ω and C = 2.2μF. The decoupling capacitor should be placed as close to the PWM controller as possible. The recommended size of R_{VCC} is 0603.

Pin No.	Pin Name	Pin Function
11	IMONB	Rail B VR current monitor output for controller. This pin outputs a voltage proportional to the output current.
12	IMONC	Rail C VR current monitor output for controller. This pin outputs a voltage proportional to the output current.
13	IMOND	Rail D VR current monitor output for controller. This pin outputs a voltage proportional to the output current.
14	ISENDN	Negative input of current-sense amplifier for rail D.
15	ISENDP	Positive input of current-sense amplifier for rail D.
16	TSENC	Thermal sense input for rail C.
17	TSENB	Thermal sense input for rail B.
18	TSENA	Thermal sense input for rail A.
19	VREF	Fixed 0.6V output reference voltage. This voltage is used to offset the output voltage of all IMON pins. When the controller shuts down or sets all rails in PS4, the voltage source shuts down. An exact 0.47μF decoupling capacitor and a 3.9Ω resistor must be placed between this pin and GND.
20	IMONA	Rail A VR current monitor output for controller. This pin outputs a voltage proportional to the output current.
21	RGNDA	Return ground for rail A VR. This pin is the negative node of the differential remote voltage sense.
22	VSENA	Rail A VR voltage sense input. This pin is connected to the terminal of rail A VR output voltage.
23	COMPA	Rail A VR compensation. This pin is the error amplifier output pin.
24	FBA	Negative input of the error amplifier. This pin is for rail A VR output voltage feedback to the controller.
25	ISENA6N	Negative input of current-sense amplifier of phase 6 of rail A.
26	ISENA6P	Positive input of current-sense amplifier of phase 6 of rail A. Connect this pin to 5V can disable phase 6 of rail A.
27	ISENA8N	Negative input of current-sense amplifier of phase 8 of rail A.
28	ISENA8P	Positive input of current-sense amplifier of phase 8 of rail A. Connect this pin to 5V can disable phase 8 of rail A.
29	ISENA4N	Negative input of current-sense amplifier of phase 4 of rail A.
30	ISENA4P	Positive input of current-sense amplifier of phase 4 of rail A. Connect this pin to 5V can disable phase 4 of rail A.
31	ISENA2N	Negative input of current-sense amplifier of phase 2 of rail A.
32	ISENA2P	Positive input of current-sense amplifier of phase 2 of rail A. Connect this pin to 5V can disable phase 2 of rail A.
33	ISENA1N	Negative input of current-sense amplifier of phase 1 of rail A.
34	ISENA1P	Positive input of current-sense amplifier of phase 1 of rail A. Connect this pin to 5V can disable rail A.
35	ISENA3N	Negative input of current-sense amplifier of phase 3 of rail A.
36	ISENA3P	Positive input of current-sense amplifier of phase 3 of rail A. Connect this pin to 5V can disable phase 3 of rail A.
37	ISENA5N	Negative input of current-sense amplifier of phase 5 of rail A.
38	ISENA5P	Positive input of current-sense amplifier of phase 5 of rail A. Connect this pin to 5V can disable phase 5 of rail A.
39	ISENA7N	Negative input of current-sense amplifier of phase 7 of rail A.

Pin No.	Pin Name	Pin Function
40	ISENA7P	Positive input of current-sense amplifier of phase 7 of rail A. Connect this pin to 5V can disable phase 7 of rail A.
41	SD_GOOD	For soldering verification, connect this pin to 5V and turn on the EN pin. If the soldering is good, all rail outputs are Non-zero VBOOT. For the I^2C address setting, connect this pin to GND with a resistor.
42	DRVEN_F	External driver mode control and the output high level is VCC. After receiving the PS4 command, this pin will be in a floating state. For the discrete power MOSFET driver application, connecting a 100-kΩ resister to GND is required.
43	PWMA8	PWM output of phase 8 of rail A. The tri-state window 1.6V-2.2V/1.4V-2.1V is programmable via NVM.
44	PWMA6	PWM output of phase 6 of rail A. The tri-state window 1.6V-2.2V/1.4V-2.1V is programmable via NVM.
45	PWMA7	PWM output of phase 7 of rail A. The tri-state window 1.6V-2.2V/1.4V-2.1V is programmable via NVM.
46	PWMA5	PWM output of phase 5 of rail A. The tri-state window 1.6V-2.2V/1.4V-2.1V is programmable via NVM.
47	PWMA3	PWM output of phase 3 of rail A. The tri-state window 1.6V-2.2V/1.4V-2.1V is programmable via NVM.
48	PWMA1	PWM output of phase 1 of rail A. The tri-state window 1.6V-2.2V/1.4V-2.1V is programmable via NVM.
49	PWMA2	PWM output of phase 2 of rail A. The tri-state window 1.6V-2.2V/1.4V-2.1V is programmable via NVM.
50	PWMA4	PWM output of phase 4 of rail A. The tri-state window 1.6V-2.2V/1.4V-2.1V is programmable via NVM.
51	DRVEN/DBLR_PS	The DRVEN/DBLR_PS pin can be configured as a driver enable pin (DRVEN) or a phase doubler power state pin (DBLR_PS) by the internal NVM. As DRVEN, which is an external driver mode control when the PS4 command is received, this pin will be in a low state. The output high level is VCC. As DBLR_PS, which is an external driver mode control when the PS4 command is received, this pin will be in a high state. This pin can work with the RT9637 on 1 PWM drive 2 power stages. As the PS0 command is received, this pin will be in a low state. As the PS1 command is received, this pin will be in a floating state. As the PS2 or PS3 command is received, this pin will be in a high state.
52	VSENB	Rail B VR voltage sense input. This pin is connected to the terminal of rail B VR output voltage.
53	COMPB	Rail B VR compensation. This pin is an error amplifier output pin.
54	FBB	Negative input of the error amplifier. This pin is for rail B VR output voltage feedback to controller.
55	RGNDB	Return ground for rail B VR. This pin is the negative node of the differential remote voltage sense.
56	ISENBN	Negative input of current-sense amplifier of rail B.
57	ISENBP	Positive input of current-sense amplifier of rail B. Connect this pin to 5V can disable rail B.
58	NC	No internal connection. This pin is recommended to be floating.
59	PWMB	PWM output of rail B. The tri-state window 1.6V-2.2V/1.4V-2.1V is programmable via NVM.

Pin No.	Pin Name	Pin Function
60	PWMC	PWM output of rail C. The tri-state window 1.6V-2.2V/1.4V-2.1V is programmable via NVM.
61	VR_READY	VR ready indicator.
62	ISENCP	Positive input of current-sense amplifier of rail C. Connect this pin to 5V can disable rail C.
63	ISENCN	Negative input of current-sense amplifier of rail C.
64	RGNDC	Return ground for rail C VR. This pin is the negative node of the differential remote voltage sense.
65	FBC	Negative input of the error amplifier. This pin is for rail C VR output voltage feedback to controller.
66	COMPC	Rail C VR compensation. This pin is the error amplifier output pin.
67	VSENC	Rail C VR voltage sense input. This pin is connected to the terminal of rail C VR output voltage.
68	ANS_EN	Acoustic noise suppression function setting. Pull to VCC and configuration enabled, this function can be activated. This pin is not allowed to be floating.
69 (Exposed Pad)	GND	Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.

9 Functional Block Diagram



10 Absolute Maximum Ratings

(Note 2)

- VIN/VSYS to GND ---------- –0.3V to 28V
- VCC to GND ---------- –0.3V to 6.5V
- VDIO, VCLK, $\overline{\text{ALERT}}$ to GND

  DC ---------- –0.3V to 6.8V

  < 10ns ---------- –0.45V to 7.5V
- RGND to GND ---------- –0.3V to 0.3V
- Other Pins ---------- –0.3V to 6.8V
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C

Note 2. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

11 ESD Ratings

(Note 3)

- HBM (Human Body Model) ---------- 2kV

Note 3. Devices are ESD sensitive. Handling precautions are recommended.

12 Recommended Operating Conditions

(Note 4)

- VIN/VSYS to GND ---------- 4.5V to 24V
- Supply Input Voltage, VCC ---------- 4.5V to 5.5V
- Junction Temperature Range ---------- –40°C to 125°C

Note 4. The device is not guaranteed to function outside its operating conditions.

13 Thermal Information

(Note 5)

- WQFN-68L 8x8, θ_{JA} ---------- 26.3°C/W
- WQFN-68L 8x8, $\theta_{JC(Top)}$ ---------- 4.6°C/W

Note 5. For more information about thermal parameters, see the Application and Definition of Thermal Resistances report, AN061.

14 Electrical Characteristics

(VCC = 5V, typical values are referenced to T_J = 25°C, Min and Max values are referenced to T_J from −10°C to 105°C, unless otherwise specified.)

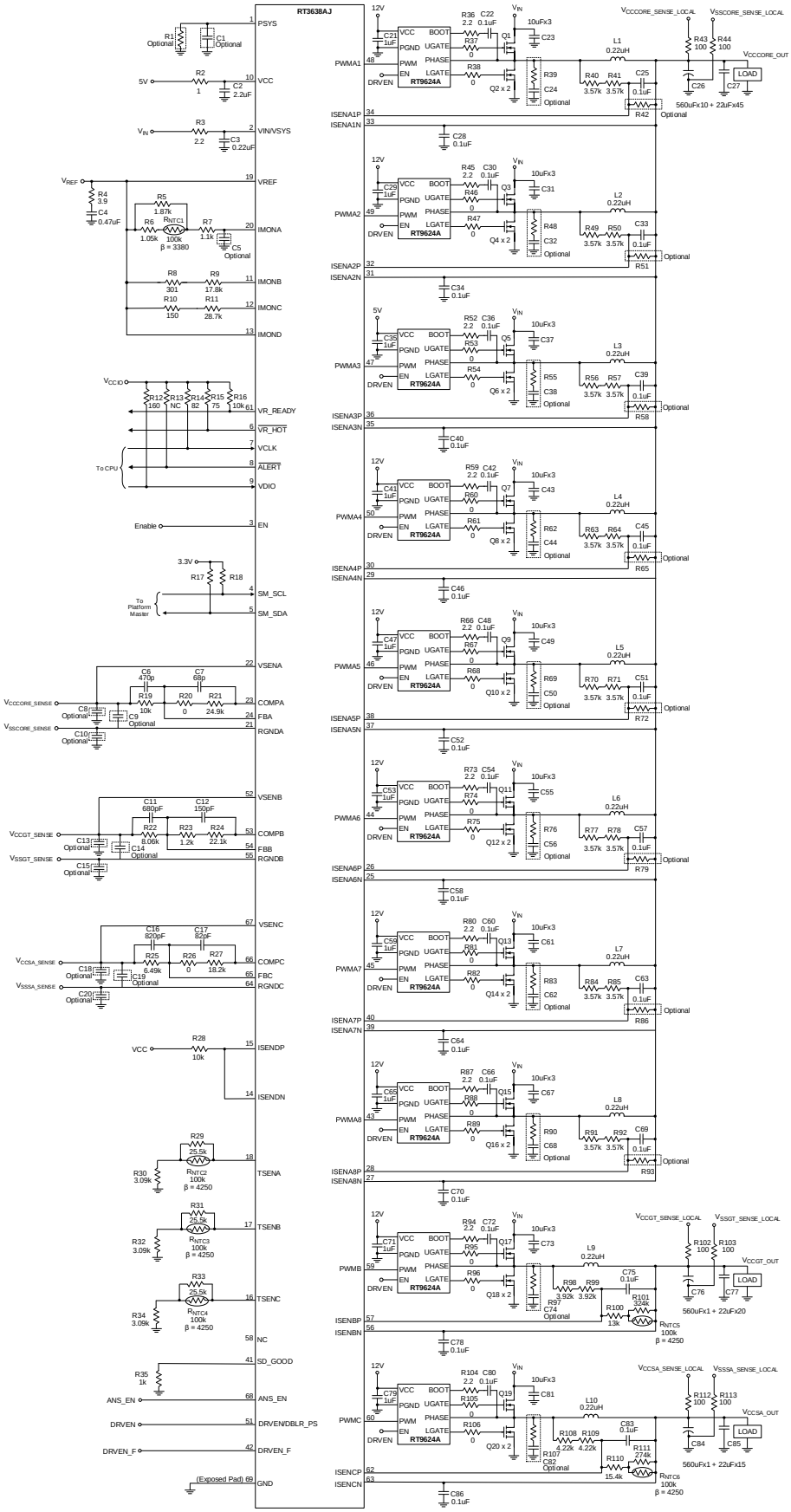
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Input						
Controller Supply Current	I_{VCC}	VCC = 5V, EN = H, no switching	--	19	--	mA
Controller Supply Current under PS4 All Calls	I_{VCC_PS4}	VCC = 5V, EN = H, PS4 all call	--	59	--	μA
VR Shutdown Current	I_{SHDN}	VCC = 5V, EN = L	--	43	--	μA
Per Phase Current Sense Amplifier						
Recommended Input Voltage Range for High Accuracy	V_{IN_PCS}	Recommend Input Voltage Range for High Accuracy	−10	--	80	mV
Current Sense Gain	GAIN_PCS		0.97	1	1.03	V/V
Current Sense Resistor	R_{INT}		--	1	--	kΩ
TON Setting Rail A						
ON-Time Setting	t_{ON}	V_{IN} = 12V, VID = 0.9V, freq. = 350kHz (K_{TONA} = 0.735)	--	214	--	ns
TON Setting Rail B/C						
ON-Time Setting	t_{ON}	V_{IN} = 12V, VID = 0.9V, freq. = 356kHz (K_{TONB}/K_{TONC} = 0.82)	--	233	--	ns
Protections						
VCC Power-ON Reset (POR)	$V_{CC\_POR\_R}$	Rising edge	4	4.3	4.45	V
	$\Delta V_{CC\_POR\_F\_HYS}$	Falling edge hysteresis	120	210	300	mV
VCC Power-ON Reset for NVM (POR_NVM)	$V_{CC\_POR\_NVM\_R}$	Rising edge	--	3.75	3.9	V
	$V_{CC\_POR\_NVM\_F}$	Falling edge	3.4	3.5	--	
Overvoltage Protection Threshold	V_{ROVP}	Respect to VID voltage VID > 1V SEL_DELTA_OVPx = 350mV	VID + 300	VID + 350	VID + 400	mV
	V_{AOVP}	VID ≤ 1V SEL_DELTA_OVPx = 350mV	1.00 + 300	1.00 + 350	1.00 + 400	mV
Soft-Start Overvoltage Protection Threshold (SS-OVP)	V_{SS-OVP}	Active while VRON recycle or PS4 exit and until PWM turn-on	2.42	2.45	2.48	V
Debounce Time of all OVP	DT_{OVP}		--	0.5	--	μs
Undervoltage Protection Threshold (UVP)	V_{UVP}	Active while VID settle and non-DACOFF	−700	−650	−600	mV
Debounce Time of UVP	DT_{UVP}		--	3	--	μs
EN and VR_READY						
VR Enable Threshold	V_{IH_EN}		0.7	--	--	V
VR Disable Threshold	V_{IL_ENF}		--	--	0.3	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Leakage Current of EN	I_{LEAK_EN}		–1	--	1	μA
Output Voltage Low of VR_READY	$V_{OL\_VR\_READY}$	I_{VR_READY} = 10mA	--	--	0.13	V
Acoustic Noise Suppression (ANS)						
ANS Enable Threshold	$V_{TH\_H\_ANS}$	VCC–V_{ANS} < 0.5V, ANS is enabled	--	--	0.5	V
ANS Disable Threshold	$V_{TH\_L\_ANS}$	VCC–V_{ANS} > 1V, ANS is disabled	1	--	--	V
Serial VID and $\overline{\text{VR\_HOT}}$						
SVID VCLK or VDIO Logic High Threshold	V_{IH_SVID}		0.65	--	--	V
SVID VCLK or VDIO Logic Low Threshold	V_{IL_SVID}		--	--	0.45	V
Leakage Current of VCLK/VDIO/ $\overline{\text{ALERT}}$ / $\overline{\text{VR\_HOT}}$	I_{LEAK_SVID}	VDIO = H, $\overline{\text{ALERT}}$ = H, $\overline{\text{VR\_HOT}}$ = H	–1	--	1	μA
Output Voltage Low of VDIO / $\overline{\text{ALERT}}$ / $\overline{\text{VR\_HOT}}$	V_{OL_VDIO}	I_{VDIO} = 10mA	0.04	--	0.13	V
	V_{OL_ALERT}	$I_{\overline{ALERT}}$ = 10mA				
	V_{OL_VRHOT}	$I_{\overline{VR\_HOT}}$ = 10mA				
I^2C Interface						
SCL or SDA High-Level Input Threshold Voltage	V_{IH_I2C}		1	--	--	V
SCL or SDA Low-Level Input Threshold Voltage	V_{IL_I2C}		--	--	0.6	
Standard/Fast Mode						
SCL Clock Rate	f_{SCL}	Standard mode	--	--	100	kHz
		Fast mode	--	--	400	
Hold Time (Repeated) Start Condition. After this Period, the First Clock Pulse is Generated	$t_{HD;STA}$		0.6	--	--	μs
Low Period of the SCL Clock	t_{LOW}		1.3	--	--	μs
High Period of the SCL Clock	t_{HIGH}		0.6	--	--	μs
Set-Up Time for a Repeated START Condition	$t_{SU;STA}$		0.6	--	--	μs
Data Hold Time	$t_{HD;DAT}$	Standard mode	0	--	--	μs
		Fast mode	0	--	0.9	
Data Set-Up Time	$t_{SU;DAT}$	Standard mode	250	--	--	ns
		Fast mode	100	--	--	
Set-Up Time for STOP Condition	$t_{SU;STO}$		0.6	--	--	μs
Bus Free Time Between a STOP and START Condition	t_{BUF}		1.3	--	--	μs
Rising Time of Both SDA and	t_R	Standard mode	--	--	300	ns

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
SCL Signals		Fast mode	20	--	300	
Falling Time of Both SDA and SCL Signals	t_F	Standard mode	--	--	300	ns
		Fast mode	20	--	300	
SDA Output Low Sink Current	I_{OL}	SDA voltage = 0.4V	2	--	--	mA
DIMON						
Digital IMON Set	dV_{IMONA_ICCMAX}	$V_{IMONA} - V_{VREF}$ = 0.4V; V_{VREF} = 0.6V	--	255	--	Decimal
	dV_{IMONB_ICCMAX}	$V_{IMONB} - V_{VREF}$ = 0.4V; V_{VREF} F = 0.6V	--	255	--	
	dV_{IMONC_ICCMAX}	$V_{IMONC} - V_{VREF}$ = 0.4V; V_{VREF} = 0.6V	--	255	--	
	dV_{IMOND_ICCMAX}	$V_{IMOND} - V_{VREF}$ =1.6V; V_{VREF} = 0.6V	--	255	--	
Thermal Monitor						
TSEN Voltage Threshold to Pull Low $\overline{VR\_HOT}$ (Asserts $\overline{VR\_HOT}$)	$V_{TSEN\_\overline{VR\_HOT}\_L}$	Within the range, $\overline{VR\_HOT}$ = L (1% resistance tolerance is considered)	--	0.600	0.620	V
TSEN Voltage Threshold to Pull High $\overline{VR\_HOT}$ (De-Asserts $\overline{VR\_HOT}$)	$V_{TSEN\_\overline{VR\_HOT}\_H}$	Within the range, $\overline{VR\_HOT}$ = H (1% resistance tolerance is considered)	0.608	0.628	0.649	V
TSEN Rises to Pull Low $\overline{ALERT}$	$V_{TSEN\_Status\_H}$	$\overline{ALERT}$ = L	0.608	0.628	0.649	V
TSEN Down to Pull Low $\overline{ALERT}$	$V_{TSEN\_Status\_L}$	$\overline{ALERT}$ = L	0.637	0.658	0.680	V
ITSEN						
Current Source from TSEN	I_{TSEN}	V_{TSEN} = 1.6V	78.8	80	81.2	μA
PSYS						
Digital IMON Reporting Code for PMAX	D_{PSYS_PMAX}	V_{PSYS} = 1.6V	--	255	--	Decimal
VSYS						
VSYS Input Voltage	V_{SYS_TH}	As V_{IN} = 24V, high byte	--	255	--	Decimal
		As V_{IN} = 12V, high byte	--	128	--	
PWM Driving Capability						
PWM Source Resistance	R_{PWM_SRC}		--	30	--	Ω
PWM Sink Resistance	R_{PWM_SNK}		--	10	--	Ω
PWM Output						
PWMx Output High Level		I_{OUT} = 4mA	VCC − 0.16	--	--	V
PWMx Output Low Level		I_{OUT} = 4mA	--	--	0.08	

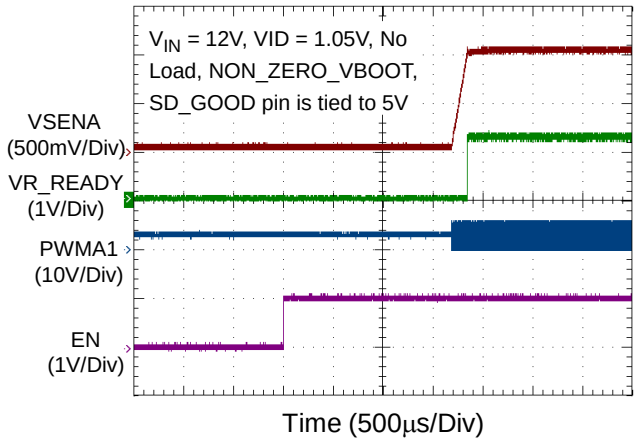
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
OSC						
Oscillator Frequency 20kHz			–5	--	5	%
V_{REF}						
VREF Voltage	V_{VREF}	Normal operation	0.59	0.6	0.61	V

15 Typical Application Circuit

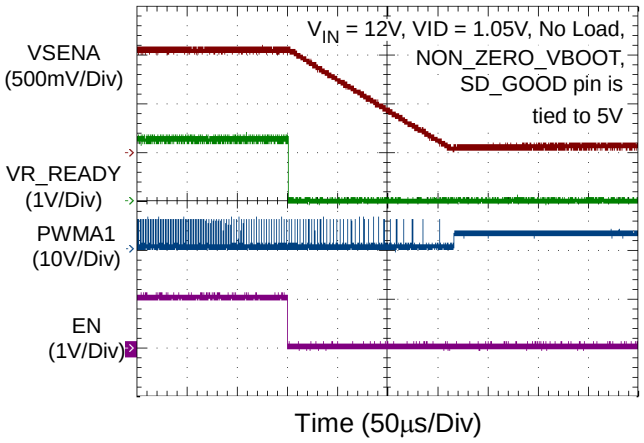


16 Typical Operating Characteristics

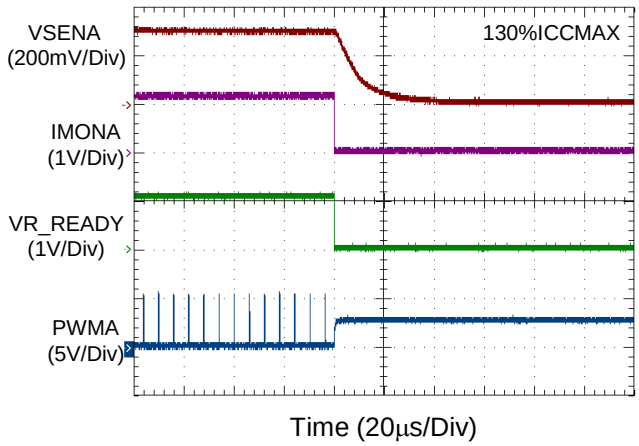
CORE VR Power On from EN



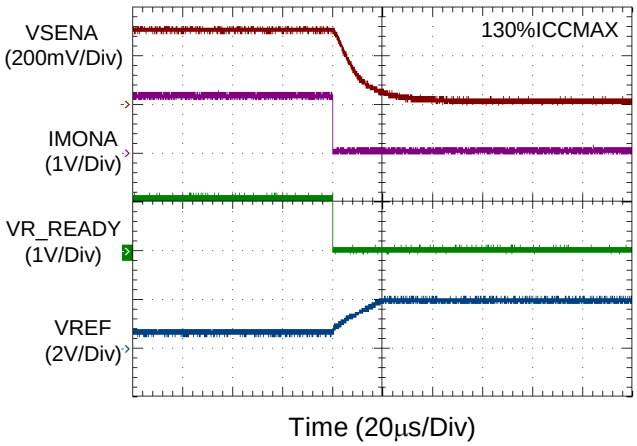
CORE VR Power Off from EN



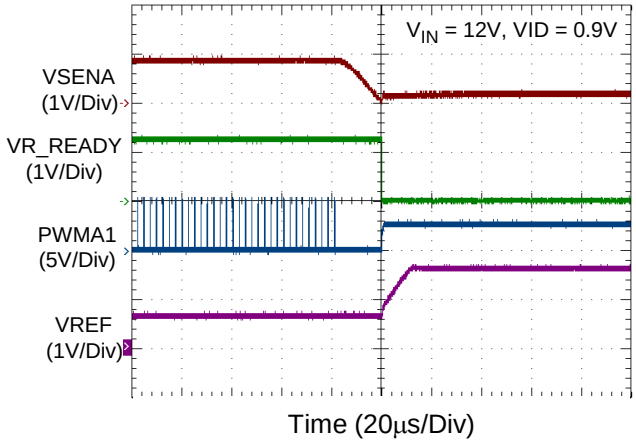
CORE VR OCP



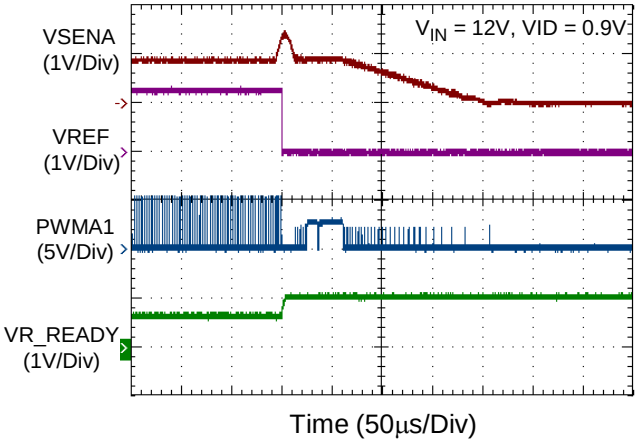
CORE VR OCP



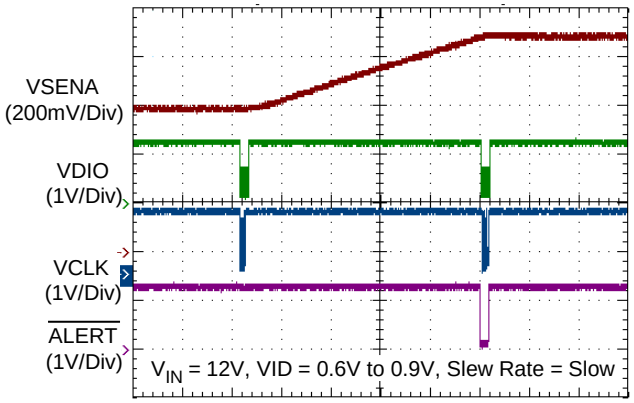
CORE VR UVP



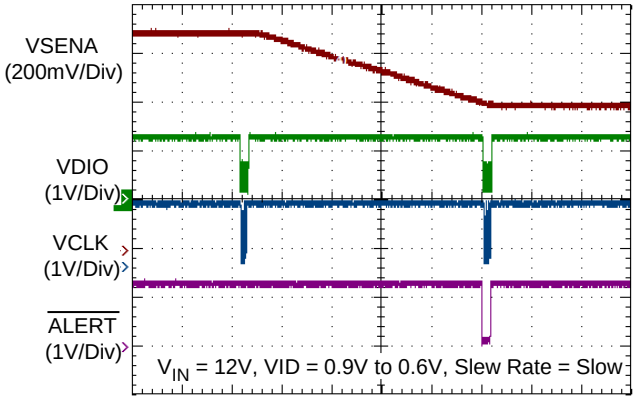
CORE VR OVP



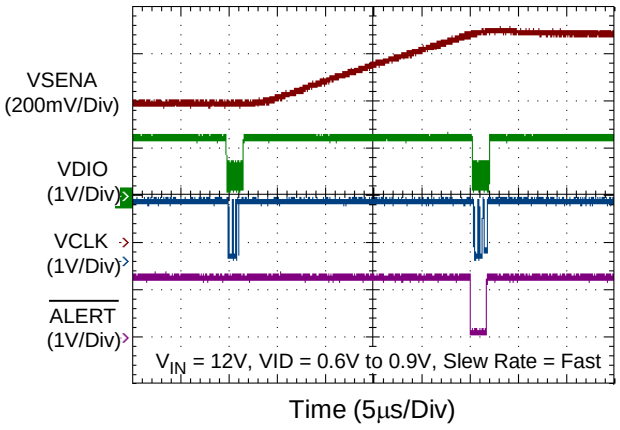
CORE VR Dynamic VID Up



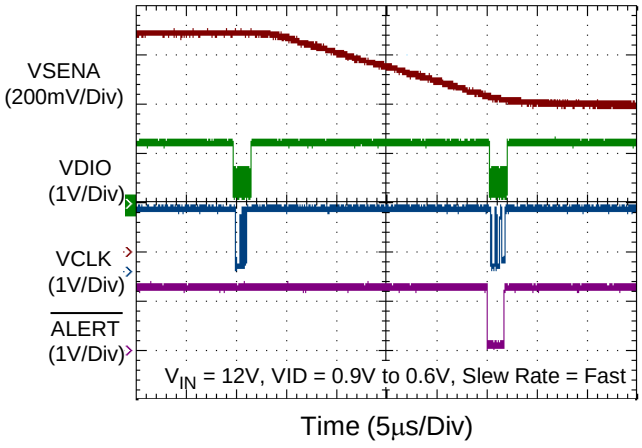
CORE VR Dynamic VID Down



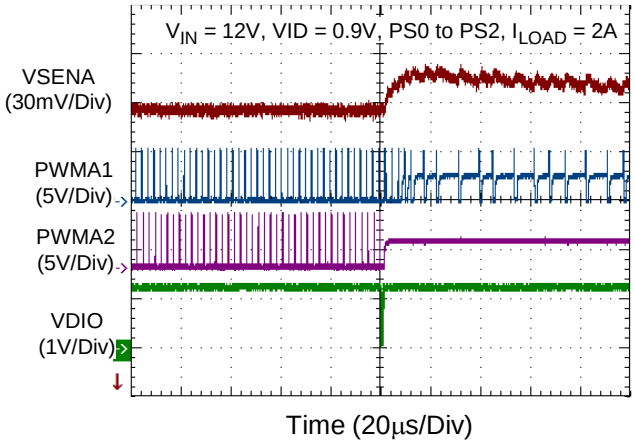
CORE VR Dynamic VID Up



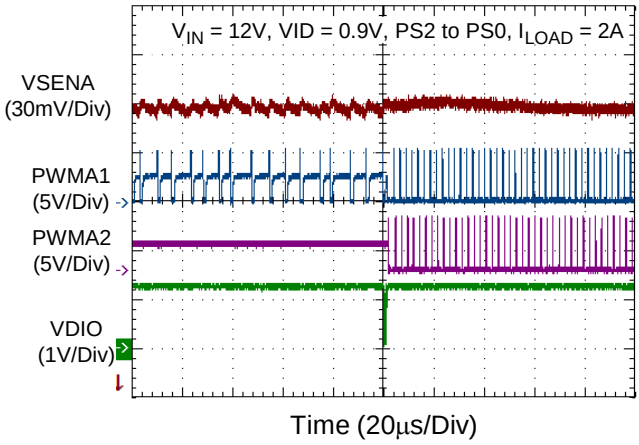
CORE VR Dynamic VID Down



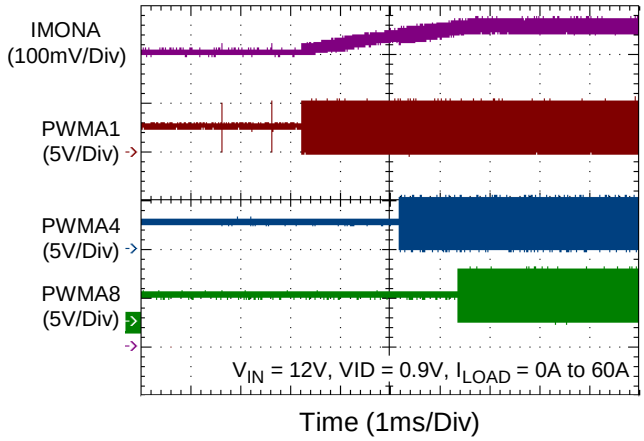
CORE VR Mode Transient



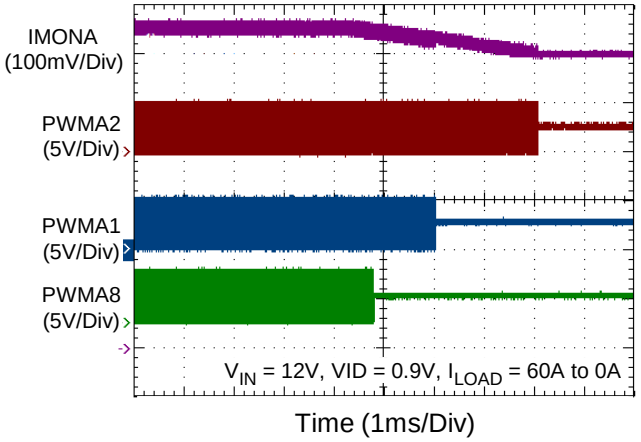
CORE VR Mode Transient



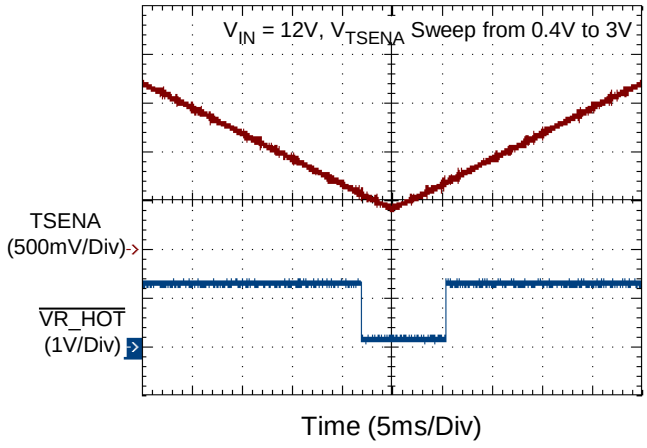
CORE VR Smart Phase Management



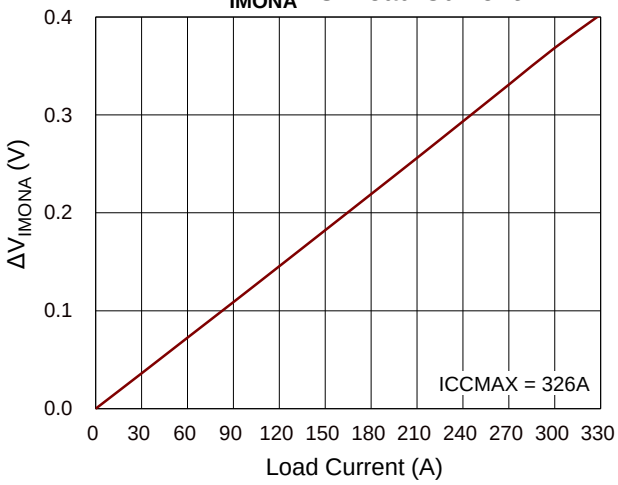
CORE VR Smart Phase Management



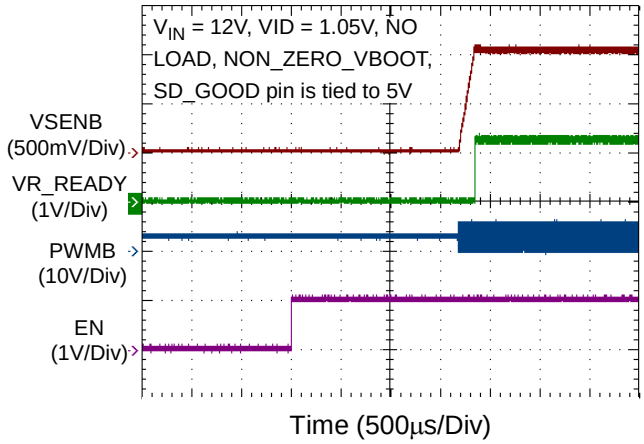
CORE VR Thermal Monitioring



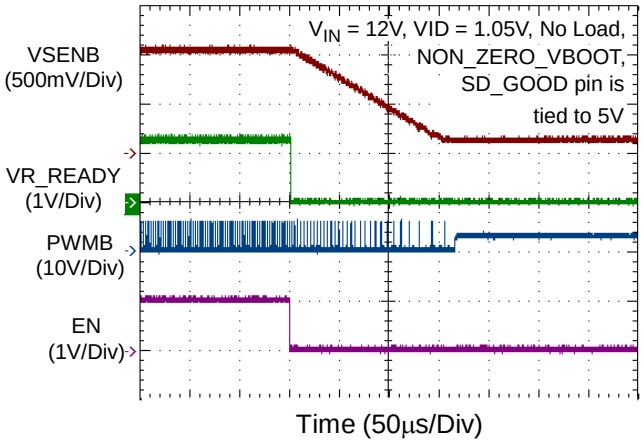
ΔV_{IMONA} vs. Load Current



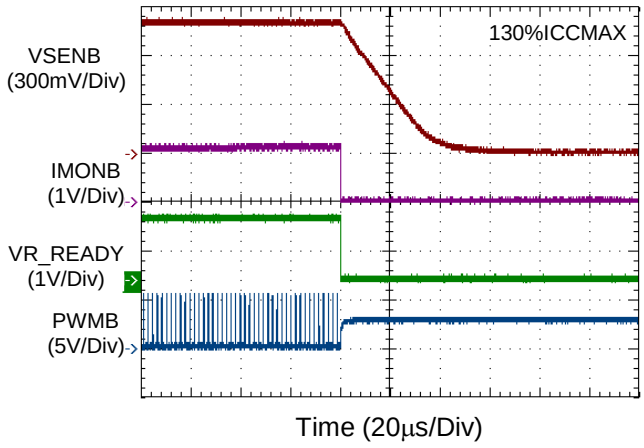
GT VR Power On from EN



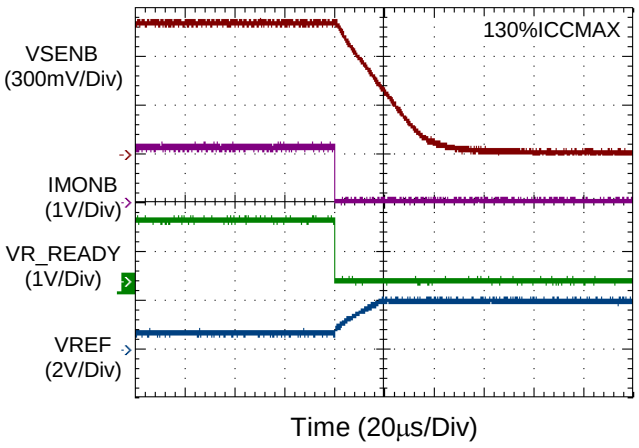
GT VR Power Off from EN



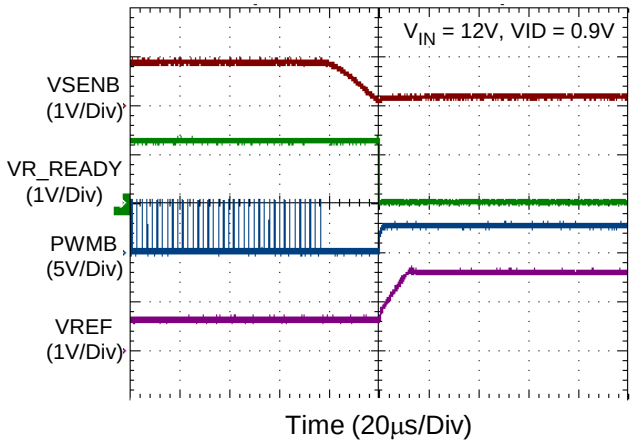
GT VR OCP



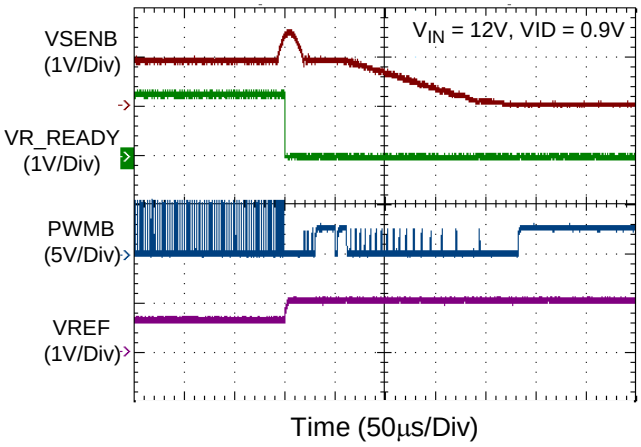
GT VR OCP



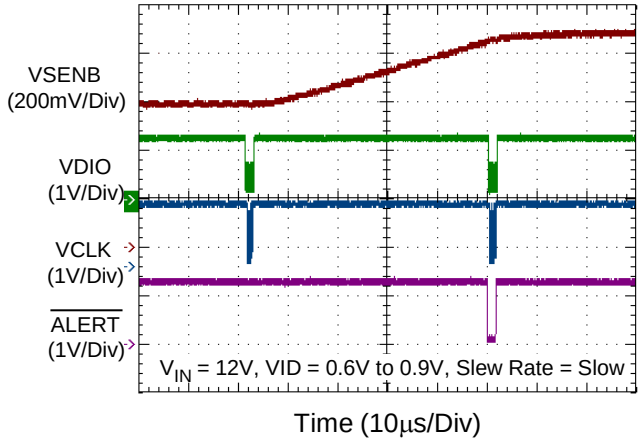
GT VR UVP



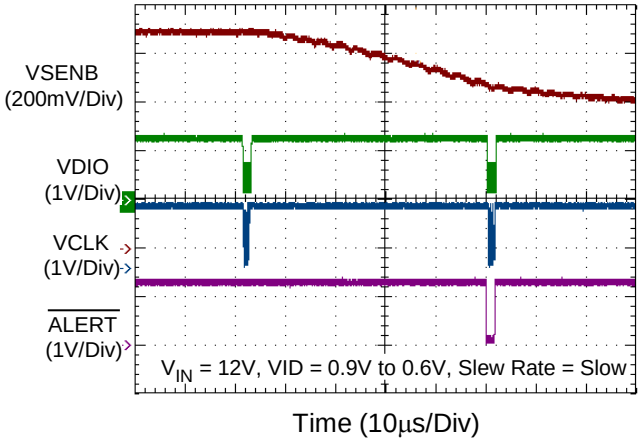
GT VR OVP



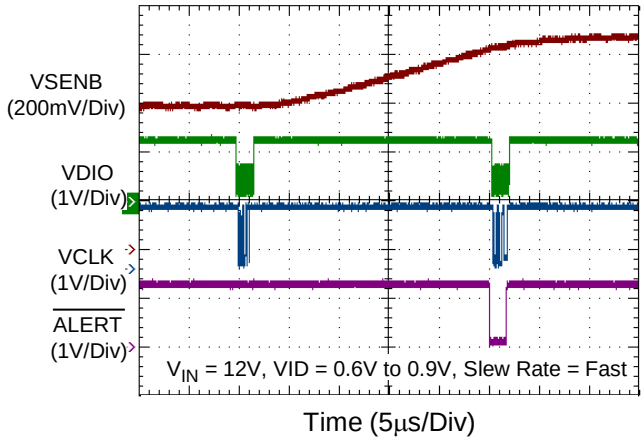
GT VR Dynamic VID Up



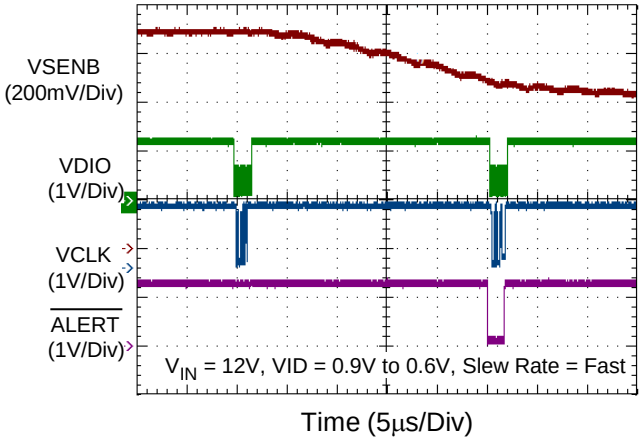
GT VR Dynamic VID Down



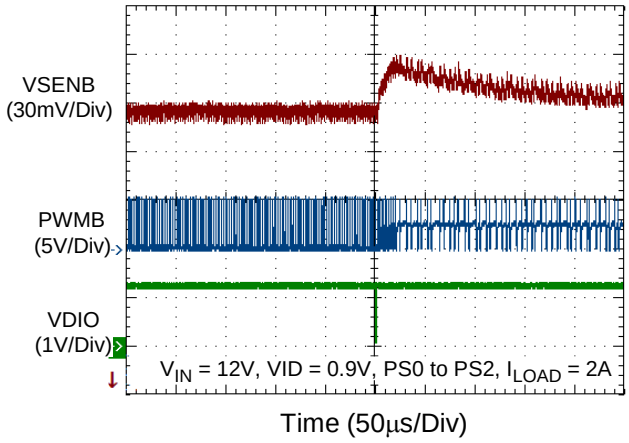
GT VR Dynamic VID Up



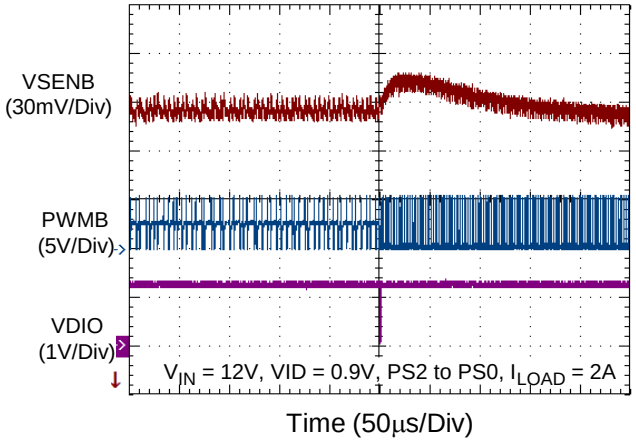
GT VR Dynamic VID Down



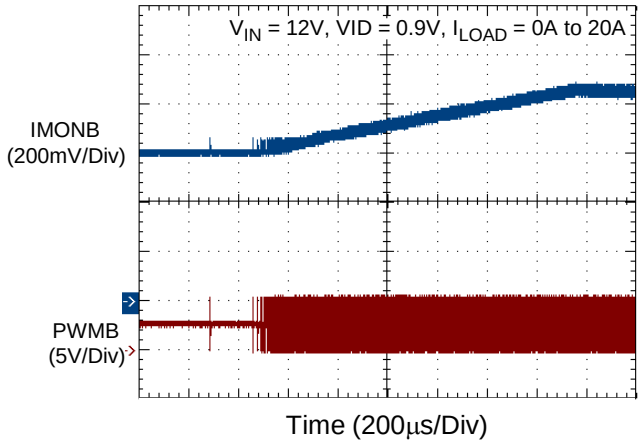
GT VR Mode Transient



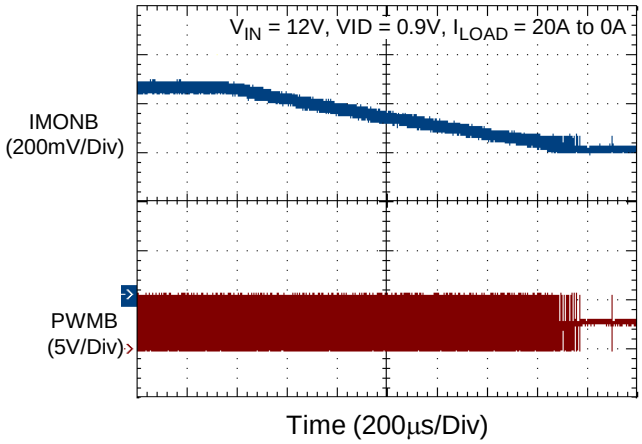
GT VR Mode Transient



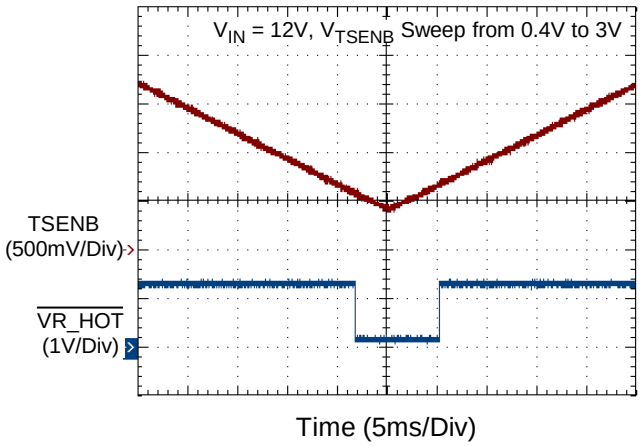
GT VR Smart Phase Management



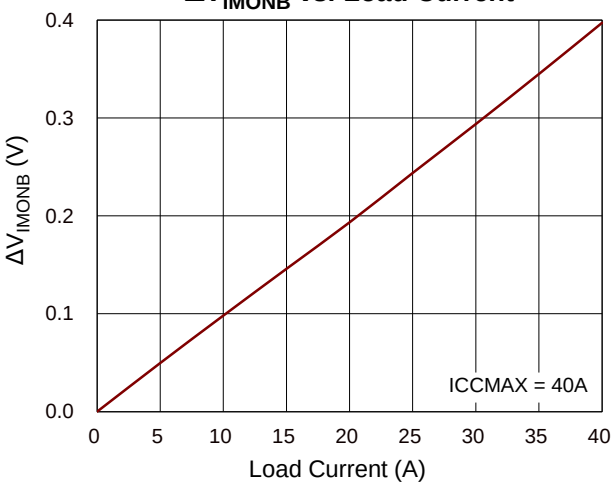
GT VR Smart Phase Management



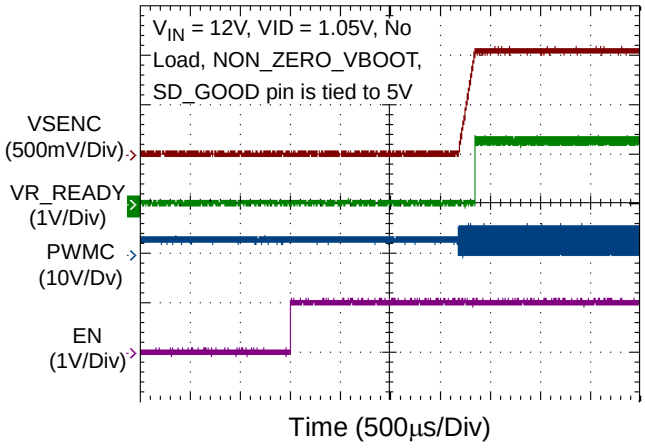
GT VR Thermal Monitioring



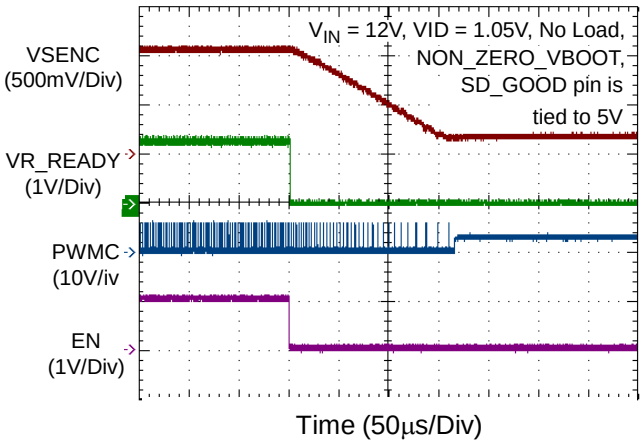
ΔVIMONB vs. Load Current



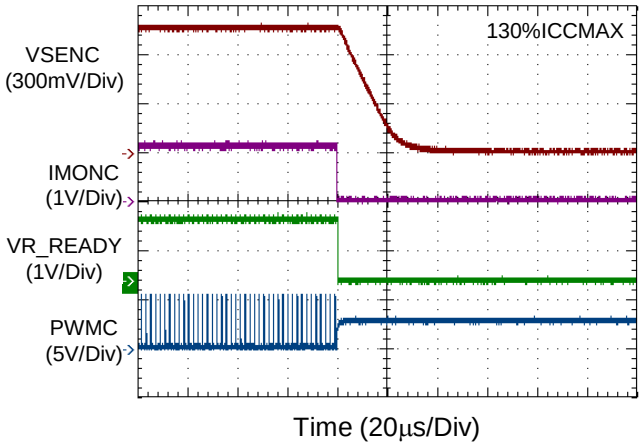
SA VR Power On from EN



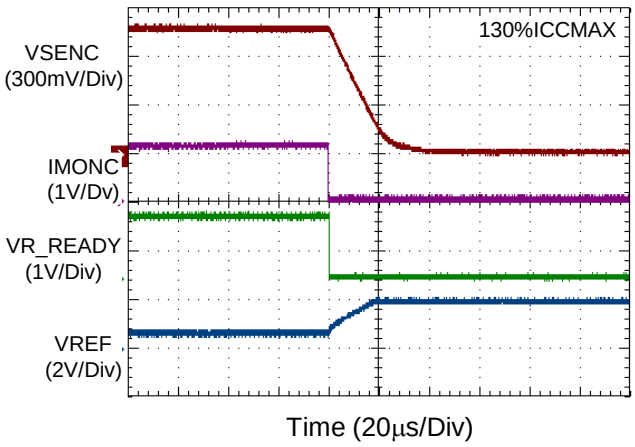
SA VR Power Off from EN



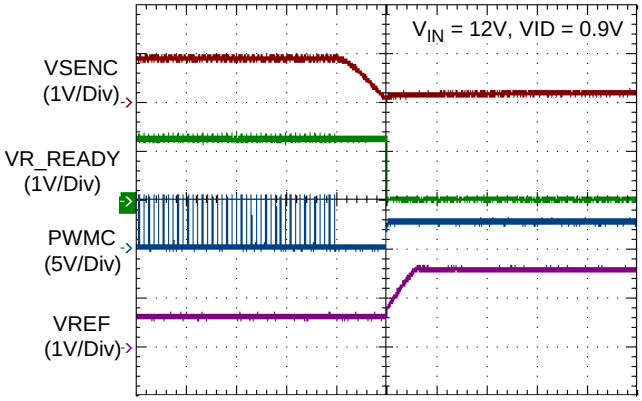
SA VR OCP



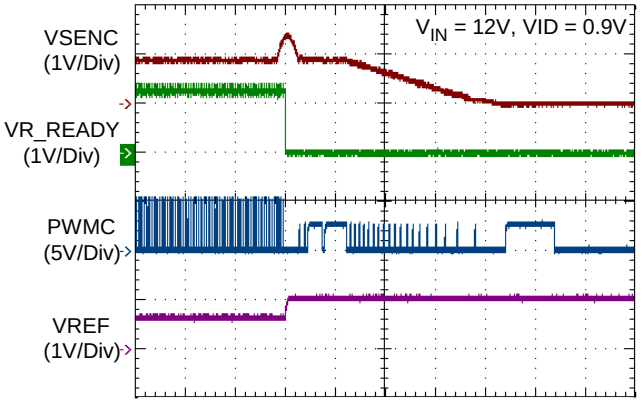
SA VR OCP



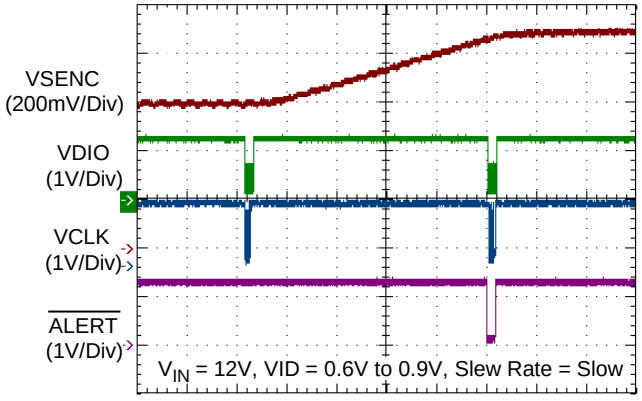
SA VR UVP



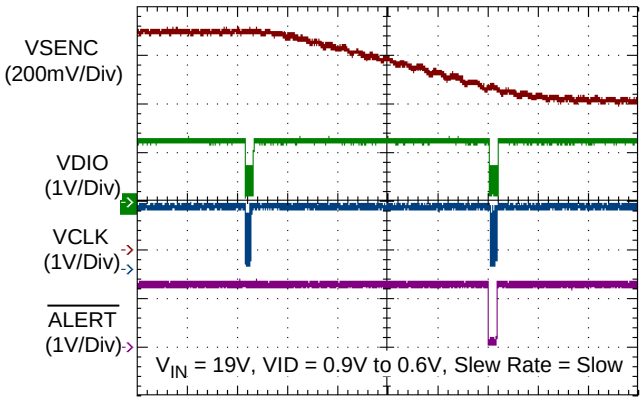
SA VR OVP



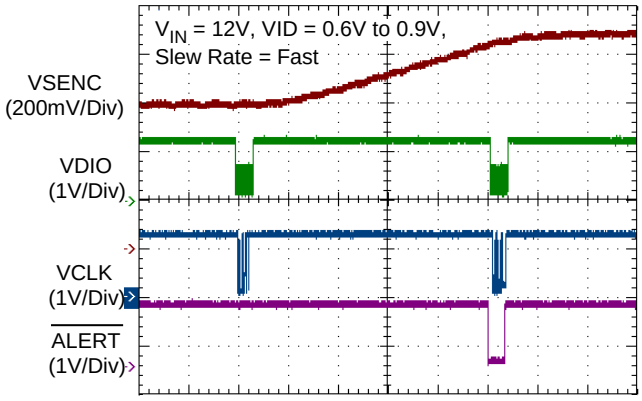
SA VR Dynamic VID Up



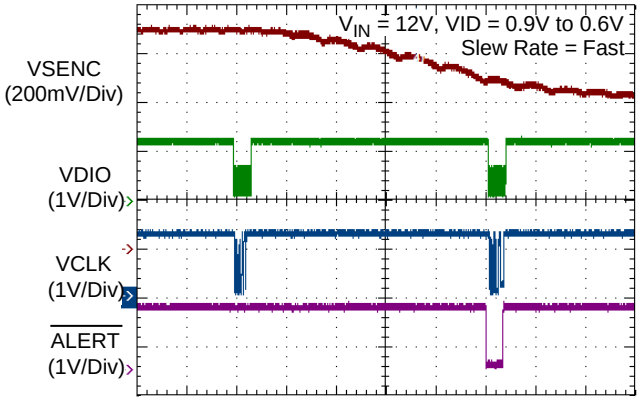
SA VR Dynamic VID Down



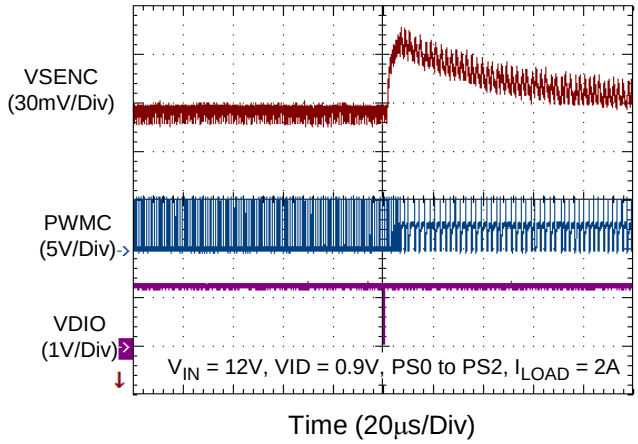
SA VR Dynamic VID Up



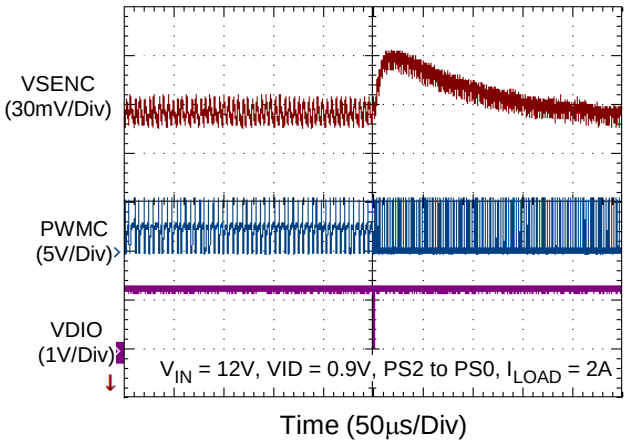
SA VR Dynamic VID Down



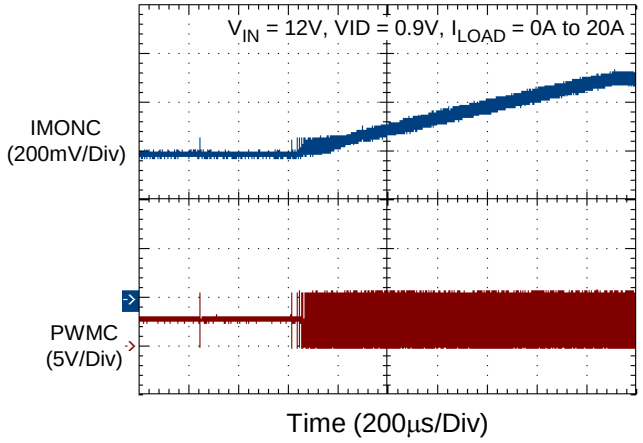
SA VR Mode Transient



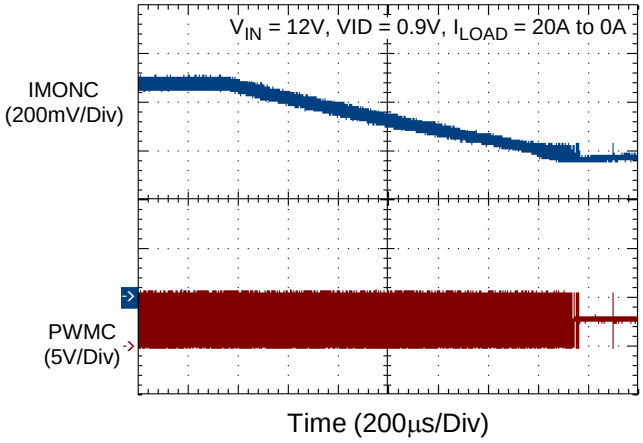
SA VR Mode Transient



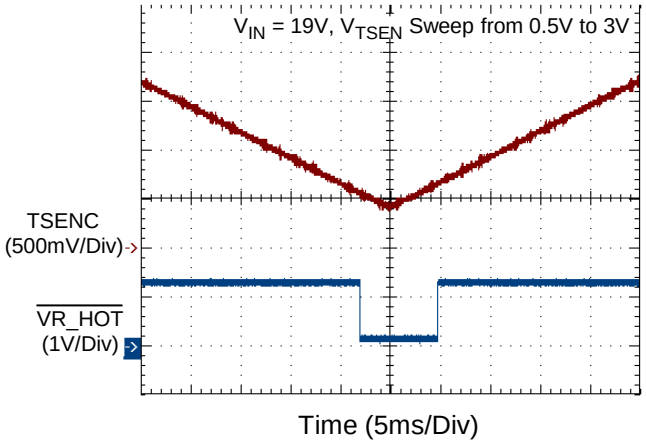
SA VR Smart Phase Management



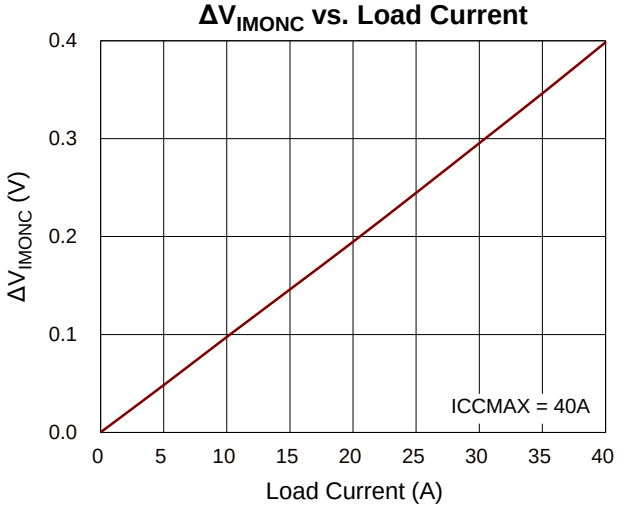
SA VR Smart Phase Management



SA VR Thermal Monitioring



ΔV_{IMONC} vs. Load Current



17 Operation

17.1 G-NAVP™ Control Mode

The RT3638AJ adopts G-NAVP™ (Green Native AVP), which is Richtek's proprietary topology. It is derived from the current mode constant-on-time control with a finite DC gain of the error amplifier and DC offset cancellation. The topology can achieve easy load line design and provide high DC accuracy and fast transient response. When the sensed current signal reaches the sensed voltage signal, the RT3638AJ generates a PWM pulse to achieve loop modulation. Figure 1 shows the basic G-NAVP™ behavior waveforms. The COMP signal is the sensed voltage that is the inverted and amplified signal of the output voltage. While the current load increases, COMP rises in response to the drop in output voltage, as shown in Figure 1. Then, this increase in COMP forces the PWM to turn on earlier and closer. While the inductor current reaches the load current, COMP enters another steady state of higher voltage, and the corresponding output voltage is in the steady state of lower voltage. The load line where the output voltage droops by an amount proportional to the load current, is achieved.

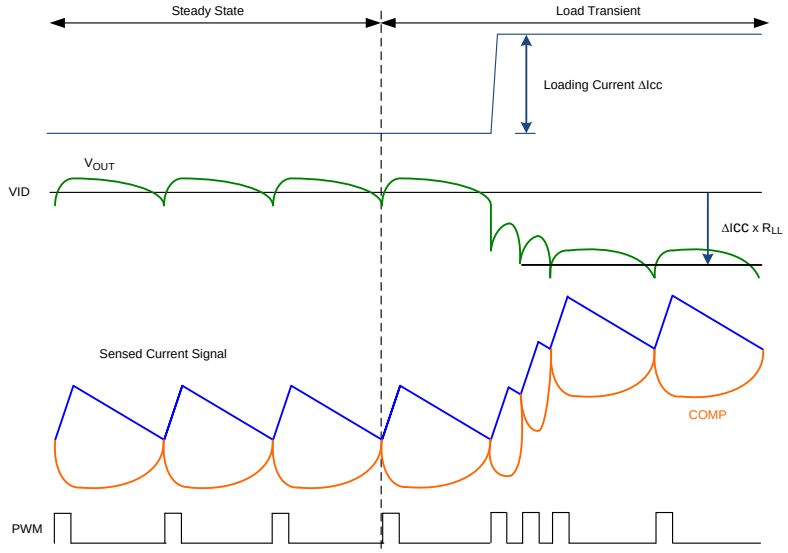


Figure 1. G-NAVP™ Behavior Waveform

17.2 SVID Interface, Control Logic, and Configuration Registers

The SVID Interface receives or transmits the SVID signal with CPU. The Control Logic executes commands (Read/Write registers, SetVID, SetPS) and sends the related signals to control VR. The Configuration Registers include function setting registers and registers required by the CPU.

17.3 IMON Filter

The IMON Filter is used to average the current signal using an analog low-pass filter. It outputs $IMON_{AVG}$ to the MUX of ADC for current reporting.

17.4 MUX and ADC

The MUX supports the inputs for TSENA, TSENB, TSENC, PSYS, $IMONA_{AVG}$, $IMONB_{AVG}$, $IMONC_{AVG}$, and $IMOND_{AVG}$. The ADC converts these analog signals to digital codes for reporting or function settings.

17.5 UVLO

The Under Voltage Lock Out (UVLO) detects the VCC voltage. As VCC exceeds the specified threshold, the controller sets Power-On Reset (POR) = high and waits EN. After both POR and EN are ready, the controller is enabled.

17.6 Loop Control and Protection Logic

The Loop Control and Protection Logic module controls the power-on/off sequence, protections, power state transition, and PWM sequence.

17.7 DAC

The DAC generates a reference VID voltage according to the VID code sent by Control Logic. According to a SetVID command, Control Logic dynamically changes the VID voltage to the target voltage with required slew rate.

17.8 ERROR AMP

The ERROR AMP inverts and amplifies the difference between the output voltage and the VID by setting an externally finite DC gain. The output signal is COMP for PWM triggers.

17.9 PER CSGM

The PER CSGM senses per-phase inductor current. The outputs are used for loop response, Current Balance, Zero Current Detection, current reporting, and overcurrent protection.

17.10 SUM CSGM

The SUM CSGM senses the total inductor current with RIMON gain adjustment. The output current ratio of the SUM CSGM can also be selected by the configuration registers. It supports a wide range of applications of DCR and load line adjustments. The output from the SUM CSGM is used for the PWM trigger.

17.11 RAMP

The RAMP helps loop stability and transient response.

17.12 PWM CMP

The PWM comparator compares the COMP signal with the sum current signal based on RAMP to trigger the PWM.

17.13 Offset Cancellation

The offset cancellation is based on VID, COMP voltage, and the current signal from SUM CSGM to control the accuracy of the output voltage.

17.14 Current Balance

Per-phase current sense signal is compared with the average sensed current. Based on the comparison, the PWM width for each phase is adjusted to optimize current and thermal balance.

17.15 Zero Current Detection

This features indicates when the inductor current of each phase crosses the predetermined threshold. The result is used for the DEM power saving and overshoot reduction (Anti-Overshoot Function).

17.16 AQR and ANTI-OVS

The AQR is a new generation of quick response mechanisms (Adaptive Quick Response, AQR) which detects the rising edge of the load and allows all PWMs to turn on. The PWM pulse width, when triggered by AQR, adjusts adaptively to the load level. The AQR trigger level can be set by the configuration registers. ANTI-OVS can help overshoot reduction which detects loading falling edge and forces all PWMs in tri-state until the zero current is detected.

17.17 TONGEN and Driver Interface

The PWM comparator output signal triggers TONGEN to generate a PWM pulse. The PWM sequence is controlled by Loop Control. The PWM pulse width is determined by the frequency setting, current balance output, and Adaptive Quick Response (AQR) settings. Once AQR is triggered, VR allows all PWMs to turn on at the same time. The driver interface provides high, low, and tri-state outputs to drive an external driver. In power-saving mode, the Driver Interface forces the PWM in a tri-state to turn off both the high-side and low-side power MOSFETs, according to Zero Current Detection output. In addition, the PWM state is controlled by Protection Logic. Different protections force the required PWM state.

17.18 SS-OVP OVP, UVP, SS-OCP, and OCP

The soft-start overvoltage protection, overvoltage protection, undervoltage protection, soft-start overcurrent protection, and overcurrent protection.

17.19 CRC Failure and Communication Failure

The cyclic redundancy check (CRC) failure and Communication failure.

18 Application Information

(Note 6)

The RT3638AJ includes three voltage rails: an 8-phase synchronous buck controller for rail A, a single-phase synchronous buck controller for rail B, and a single-phase synchronous buck controller for rail C. The output of each rail can be configured to support the desired phase assignments, with a maximum of 8 phases for rail A, single phases for rail B, and single phase for rail C. Supported output configurations include 8+1+1, 7+1+1, 6+1+1, among others. are supported. The RT3638AJ is designed to meet the specification of Intel IMVP9.2 compatible CPUs with a serial SVID control interface. The controller offers built-in non-volatile memory (NVM) and an I^2C interface to store customized configurations. The RT3638AJ is used in both desktop or notebook computers.

18.1 Power-ON Sequence

In order to confirm sufficient power supply for proper operation, the VR triggers UVLO if the VCC voltage drops below the threshold VCC_POR_R − ΔVCC_POR_F_HYS. The UVLO protection shuts down the controller and forces the high-side MOSFET and the low-side MOSFET off. When VCC > VCC_POR_R, the RT3638AJ sets POR = high and waits for EN signal. After POR = high and EN > 0.7V, the controller powers on (Chip Enable = H) and starts the VR internal settings, which include internal circuit offset correction and loading the data from the NVM to the configuration registers. Users can set multi-functions through the configuration registers via the I^2C interface. Figure 2 shows the typical timing of the controller power-on. The driver power (PVCC) is highly recommended to be established after the controller VCC. This can prevent current from flowing back to VCC from PVCC through the PWMx pin or the DRVEN/ DRVEN_F pin.

.

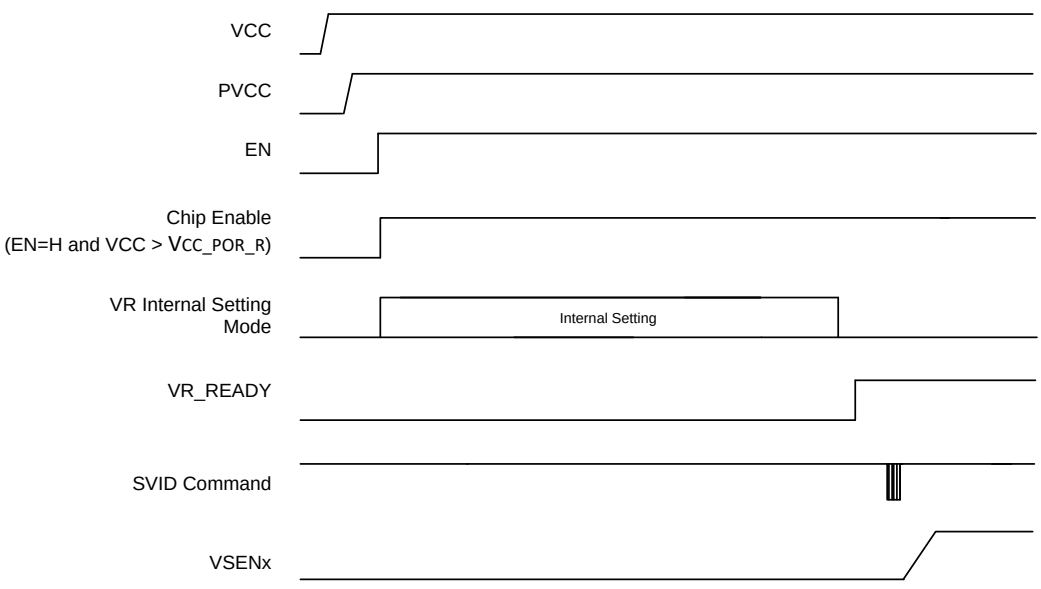


Figure 2. Typical Timing of Controller Power-ON

18.2 Maximum Active Phases Number Setting

The number of active phases is determined by the ISENxP voltage. The detection is only active and latched at Chip Enable rising edge (EN = H and VCC > 4.45V). If the voltage of ISENxP > (VCC − 0.5V), the maximum active phase number is (x-1). For example, connecting ISENA8P to VCC for setting a 7-phase operation or connecting ISEN7AP to VCC for setting a 6-phase operation. The unused ISENxN pins are recommended to be connected to VCC. However, for the SPS applications, the unused ISENxN pins must be floating. The unused PWMx pins can be floating. Figure 3 shows an example of a 7-phase operation.

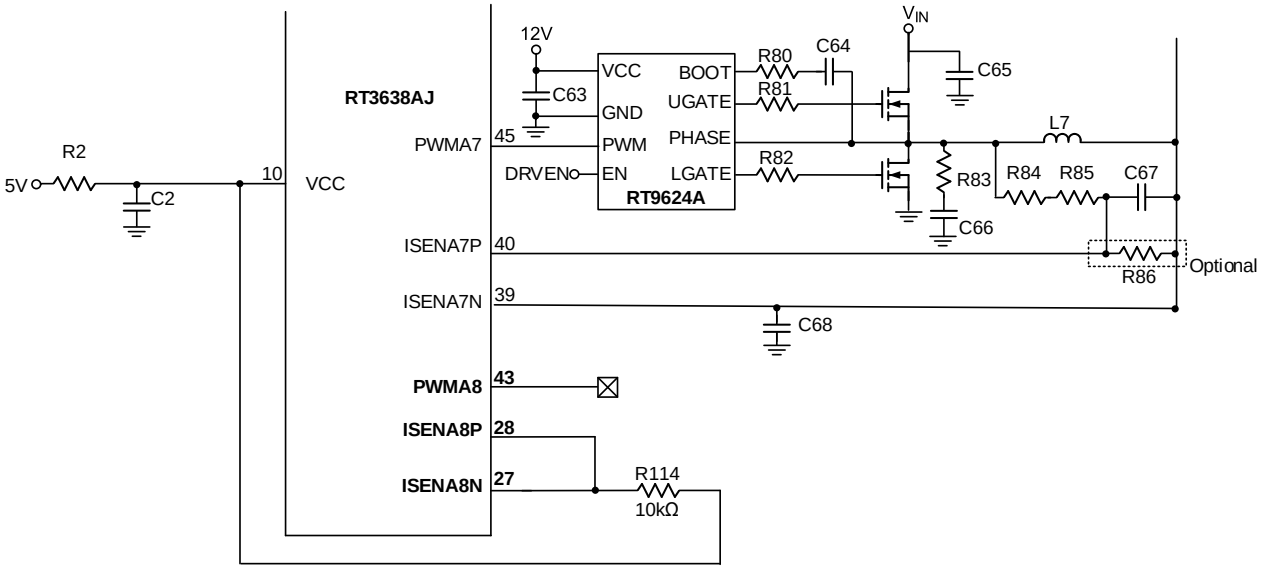


Figure 3. 7-Phases Operation Settings

18.3 Rail Disable

Connect ISENA1P to VCC for disabling rail A. The unused ISENAxN pins are recommended to connect to VCC. The unused RGNDA pin is recommended to connect to GND and the unused PWMx pins can be floating. Connect ISENBP to VCC for disabling rail B. The unused ISENBN pin is recommended to connect to VCC. The unused RGNDB pin is recommended to connect to GND and the unused PWMB pin can be floating. Connect ISENCP to VCC programs for disabling rail C. The unused ISENCN pin is recommended to connect to VCC. The unused RGNDC pin is recommended to connect to GND and the unused PWMC pin can be floating. Connect the PSYS pin to (VCC − 0.5V) for disabling the input power domain rail. Hence, any commands about this rail will be rejected. The unused ISENDP pin and ISENDN pin are recommended to connect to VCC.

18.4 Acoustic Noise Suppression

The RT3638AJ supports the acoustic noise suppression function for reducing acoustic noise induced by the piezoelectric effect from MLCC. As output voltage transitions occur, especially in dynamic VID operations, the vibrating MLCC produces acoustic noise. If the vibrating frequency falls into the audible band, the noise level is related to the output voltage transition amplitude. Therefore, the RT3638AJ adopts an acoustic noise suppression function which can be enabled through the configuration register via I^2C to reduce ΔV when SetVID down and SetVID Decay down in DEM mode.

18.5 NVM Configuration Mechanism

The RT3638AJ provides multiple parameters for platform setting and BOM optimization. These parameters can be

set through the configuration registers via I^{2}C. While POR = high and the command to load the NVM is received, VR starts loading data from the NVM to the configuration registers and function settings. Once the loading process is complete, the user configuration and NVM programing are available. Keep EN = L when NVM is programing. When EN > 0.7V, VR loads the data from the NVM again. After loading, VR proceeds internal settings. Figure 4 shows the simplified VR initialization and programming timing diagram. The intuitive RTPro Designer™ graphical user interface (GUI) is provided for user configuration, including unlocking, page setting, and programming. All setting functions are summarized in the section of Functional Register Description. The setting functions that support on-line tuning are summarized in Table 1. To change the power-on default values, users need to access the setting page. Contact Richtek for additional information on this graphical user interface.

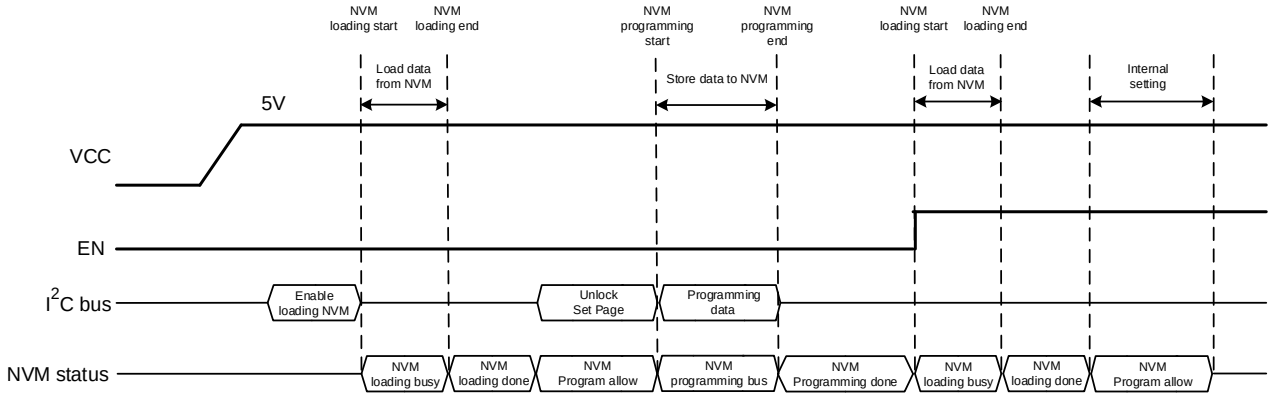


Figure 4. Simplified VR Initialization and Programing Timing Diagram

Table 1. Setting Function that Support Online Tuning

Register Address	Function	Support On-line Tuning by General Register
0x23[7]	EN_SPMB	0xB6[5]
0x23[6]	EN_SPMC	0xC6[5]
0x27[3]	EN_SPMA	0xA3[3]
0x27[1]	EN_UVA	0x98[1]
0x2B[7]	SEL_SUM_OCP_DEB_TIMEA	0x98[5]
0x2F[2]	EN_SS_OCPA	0x98[4]
0x2B[6]	SEL_SUM_OCP_DEB_TIMEB	0xAF[5]
0x2F[1]	EN_SS_OCPB	0xAF[4]
0x2C[7]	SEL_SUM_OCP_DEB_TIMEC	0xBF[5]
0x2F[0]	EN_SS_OCPC	0xBF[4]
0x15[6:4]	SEL_KTONA	0x9F[2:0]
0x46[2]	EN_ANSA	0xA7[4]
0x17[3:0]	SEL_SMALL_LLA	0xA7[3:0]
0x15[2:0]	SEL_KTONB	0xB5[2:0]
0x46[1]	EN_ANSB	0xB6[4]
0x18[7:4]	SEL_SMALL_LLB	0xB6[3:0]
0x16[6:4]	SEL_KTONC	0xC5[2:0]
0x46[0]	EN_ANSC	0xC6[4]
0x18[3:0]	SEL_SMALL_LLC	0xC6[3:0]
0x1B[7]	SEL_ANS_BEHAV	0xCC[3]

18.6 I²C Address Setting

The RT3638AJ provides multiple I²C addresses to support multiple devices connected on a single I²C bus. To properly set the I²C address (7-bit or 8-bit format), connect resistors with 1% tolerance from the SD_GOOD pin to ground. The required resistance is listed in Table 2. The controller sends the first target address followed by the write bit (0b). For example, the 8-bit target address is formed by appending the write bit (0b) to the 7-bit address:

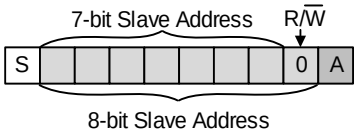


Table 2. I²C Address Setting (7-bit or 8-bit format)

I²C Address (7-bit)	I²C Address (8-bit)	Resistance (kΩ)
		Typical
0x20	0x40	1
0x21	0x42	24.9
0x22	0x44	60.4
0x23	0x46	121

18.7 Thermal Monitoring and Indicator

Thermal monitoring is processed by the TSENx pin. The block diagram of the thermal monitoring network is shown in Figure 5. The voltage of the TSENx pin is defined in Thermal Voltage, which can be calculated by the following formula:

Thermal Voltage = 80μA x (R1+ R2// R_{NTC}).

A higher temperature causes a lower Thermal Voltage. R_{NTC} = 100kΩ with β = 4250K is recommended. With proper R2 network design, the Thermal Voltage versus temperature can meet the specifications in Table 3. Among them, 97°C and 100°C must be followed to ensure the function of the thermal alert and $\overline{VR\_HOT}$. For example, when Thermal Voltage is equal to 0.6V, it means the temperature has reached 100°C. $\overline{VR\_HOT}$ is pulled to low accordingly. The RT3638AJ is based on Thermal Voltage to report the temperature zone register. The data is updated every 75μs and the averaging period is 600μs. The resistance tolerance of thermal monitoring network is recommended to be less than 1%. The NTC thermistor is recommended to be placed near the hot spot of the PCB.

For thermal monitoring network design suggestions, refer to the intuitive RTPro Designer™ graphical user interface.

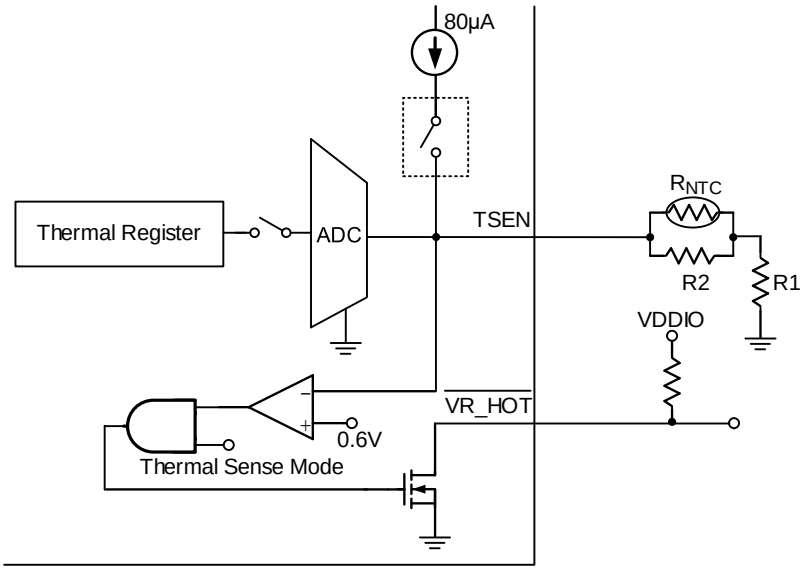


Figure 5. Thermal Monitoring Block Diagram

Table 3. Temperature Zone versus Thermal Voltage and Temperature (R_{NTC} = 100kΩ, β = 4250K)

Temperature Zone	Thermal Voltage	Temperature
FFh	0.600V	100°C
7Fh	0.628V	97°C
3Fh	0.658V	94°C
1Fh	0.690V	91°C
0Fh	0.725V	88°C
07h	0.761V	85°C
03h	0.800V	82°C
01h	0.900V	75°C

18.8 System Input Power Monitoring (PSYS)

The RT3638AJ provides the PSYS function to monitor the system input power and report to the CPU via the SVID interface. The block diagram is shown in Figure 6. The PSYS meter measures the system input current and outputs a proportional current signal I_{PSYS}. R_{PSYS} is designed for the maximum PSYS voltage = 1.6V corresponding to 100% of the system input power. The PSYS threshold can be set through SVID (0 to 1.6V corresponding to 00h to FFh). If the input power is higher than the critical threshold, controller asserts $\overline{VR\_HOT}$.

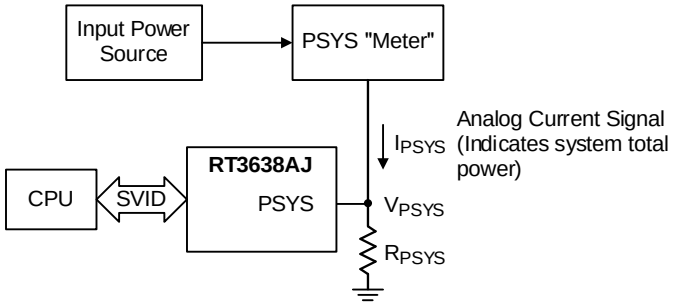


Figure 6. PSYS Function Block Diagram

18.9 System Input Voltage Monitoring (VSYS)

The RT3638AJ provides an optional VSYS function to monitor the system input voltage. The VSYS threshold can be set through SVID (0 to 24V corresponding to 00h to FFh). If the input voltage is lower than the critical threshold, the controller asserts $\overline{\text{VR\_HOT}}$.

18.10 Zero Loadline

The RT3638AJ supports a zero loadline function. When the zero loadline is enabled, the output voltage is determined only by the VID target and does not droop along with the loading current. Moreover, The RT3638AJ provides AC-droop control to effectively suppress load transient ring back and reduce overshoot in zero loadline applications. Figure 7 shows the load transient without AC-droop control. Without AC-droop control, extra ring back ΔV2 on the output voltage can be seen due to the charging of C area. Figure 8 shows the condition with AC-droop control. When the output loading increases, the controller changes the VID target to a short-term voltage target temporarily. The short-term voltage target is related to the transient loading current ΔI_{CC} and can be represented as follows:

Short_Term_Voltage_Target = VID - ΔI_{CC} × RLL

The method for setting RLL is the same as the loadline system. Then, the voltage target recovers to the original VID target slowly. AC-droop control can help to decrease the peak inductor current. Hence, the ring back ΔV2 can be suppressed. The overshoot amplitude is reduced to only ΔV3.

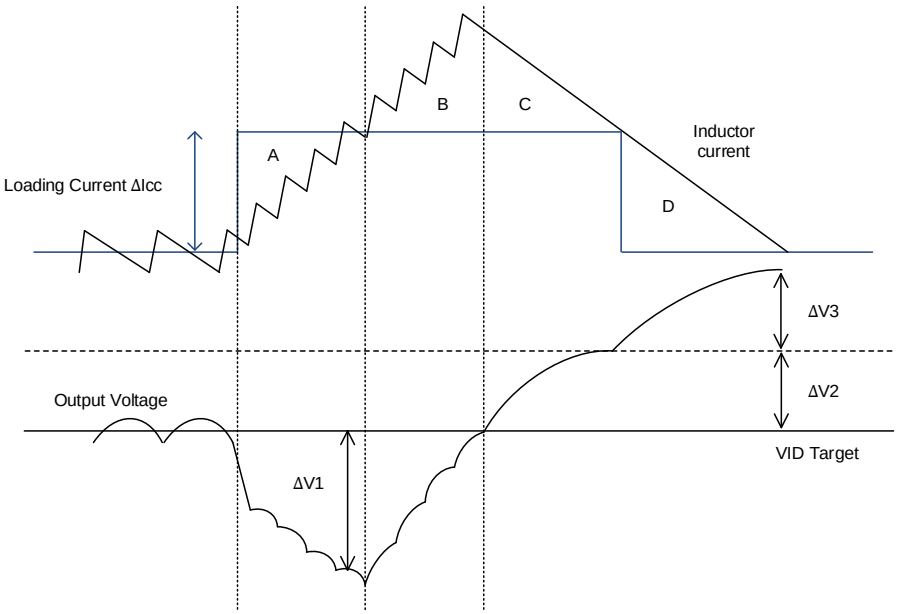


Figure 7. Zero Loadline without AC-Droop Control

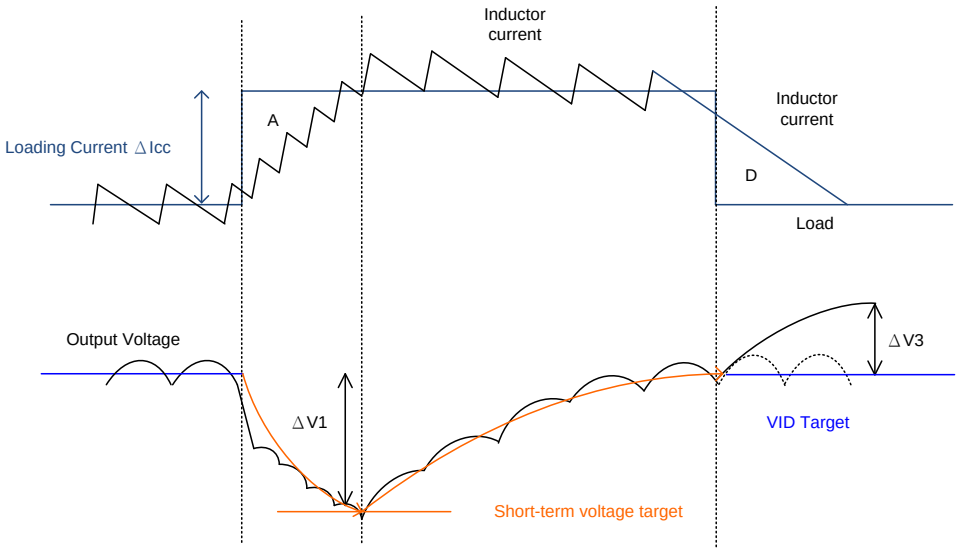


Figure 8. Zero Loadline with AC-Droop Control

18.11 Current Sensing

The RT3638AJ supports two different current sense mechanisms, one is DCR current sensing and the other is Smart Power Stage (SPS) current sensing.

18.12 DCR Current Sense

To achieve higher efficiency, the RT3638AJ adopts inductor DCR current sense to acquire per phase current signal, as illustrated in Figure 9. An external low-pass filter (R_{X1}, R_{X2} and C_X), reconstructs the inductor current I_{LX}. The RC time constant (R_{X1}//R_{X2}) x C_X should match the inductor time constant $\frac{L_X}{DCR}$. In order to get better transient performance and current reporting, R_{X1}, R_{X2} and C_X may need to be adjusted case-by-case. If the RC network time constant is equal to the inductor time constant, an ideal load transient waveform can be achieved. If the RC network time constant is larger than the inductor time constant, a sluggish droop can be seen on VSEN during load transients. On the other hand, if the RC network is smaller than the inductor time constant, an undesired current spike during load transients induces an undershoot on VSEN. This undershoot fails to meet the specification and may falsely trigger overcurrent protection (SUM-OCP). Figure 10 shows the output waveforms for these three cases of the RC network time constant. The R_{X1} is highly recommended to use two 0603 size resistors in series to enhance the I_{OUT} reporting accuracy. The C_X is suggested to be a 0.1µF X7R/0603 due to its low de-rating value at high frequency. The per phase current is derived as follows:

$$I_{CS,PERx} = \frac{V_{CSIN}}{R_{INT.}} = \frac{I_{Lx} \times DCR}{R_{INT.}}$$

The R_{X2} is optional for preventing V_{CSIN} exceeding the input range of the current sense amplifier. With R_{X2}, the per phase current is modified as follows:

$$I_{CS,PERx} = \frac{V_{CSIN}}{R_{INT.}} = \frac{I_{Lx} \times DCR}{R_{INT.}} \times \frac{R_{X2}}{R_{X1}+R_{X2}}$$

The current signal $I_{CS,PERx}$ is mirrored for loadline control, current reporting, current balance, and zero current detection. The mirrored current I_{IMONx} is 1.25 times of $I_{CS,PERx}$

($I_{IMONx}=A_{MIRROR}\times I_{CS,PERx}$, $A_{MIRROR}=1.25$)

The current sense lines must be routed as a differential pair from the inductor to the controller on the same layer.

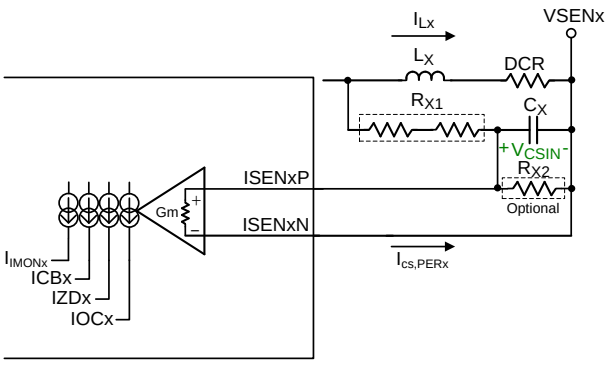


Figure 9. Inductor DCR Current Sense

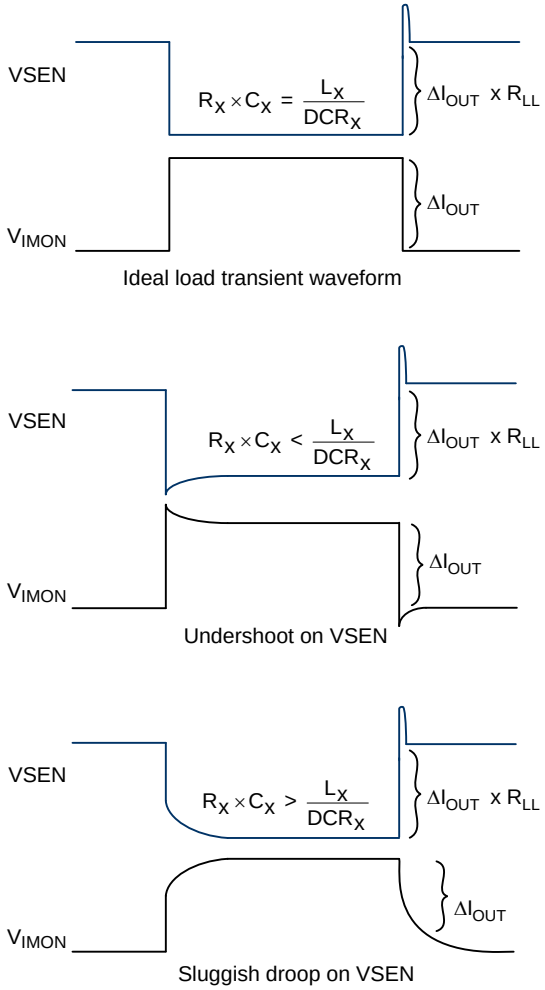


Figure 10. Three Cases of RC Network Time Constant

18.13 Total Current Sense

The total current is the sum of per phase current. With the $R_{IMONx,EQ}$ network, I_{IMONx} is converted to a voltage signal V_{IMONx} and is offset by V_{VREF} for better accuracy. V_{VREF} is a 0.6-V voltage source derived from the VREF pin in

normal operation. Figure 11 shows an 8-phase total current sense configuration. The relationship between V_{IMONx} and the inductor current I_{Lx} is asfollows:

$$V_{IMONx}\text{-}V_{VREF}=(I_{Lx1}+I_{Lx2}+ \ldots +I_{Lx8})\times \frac{DCR}{R_{INT.}}\times 1.25\times R_{IMONx}$$

$V_{IMONx} - V_{VREF}$ is proportional to the output current and is used for output current reporting, loadline loop-control, and protection. For reporting purposes, $V_{IMONx} - V_{VREF}$ is averaged by an analog low-pass filter, then sensed by an 8-bit ADC. ICCMAXx is corresponding to 0xFF. The $R_{IMONx,EQ}$ should follow dV_{IMONx_ICCMAX} to the design. The RT3638AJ provides customized ICCMAXx setting up to 510A. Refer to SET_ICCMAXx and SET_ICCMAX_ADDx. For loadline loop-control, $V_{IMONx} - V_{VREF}$ is scaled by the Ai gain, which can be selected using SEL_Ai_GAINx. Detailed applications are introduced in the Loadline Setting (R_{LL}) section.

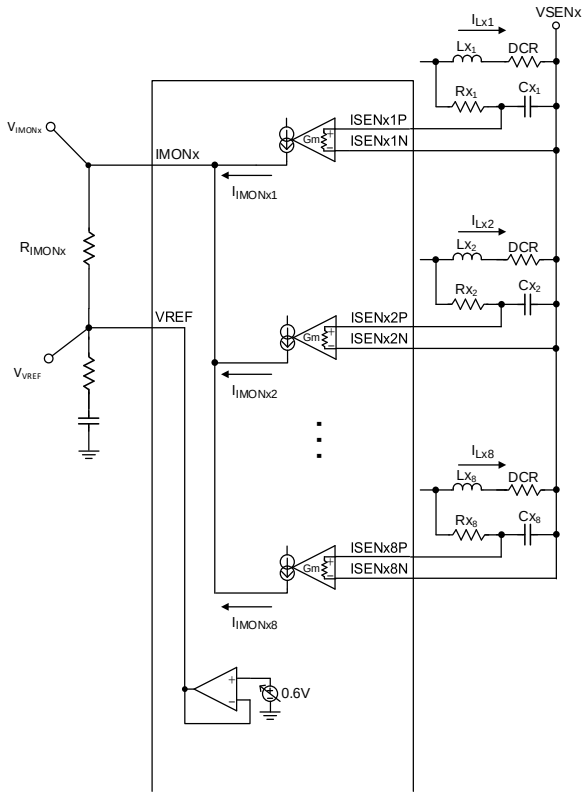


Figure 11. Total DCR Current Sense

18.14 Smart Power Stage (SPS) Current Sensing

To SPS current sensing, the setting function SEL_CS_TYPEx needs to be enabled and ISENxN operates as the output terminals, which offer the reference voltage of 1.3V for the reference inputs of SPS. A capacitor of 0.22μF to 1μF is suggested to be connected between ISENxN to GND. Figure 12 shows the implementation of a single-phase SPS current sensing report. The V_{IMON_X} and current reporting from SPS can be calculated using the following equation:

$$V_{IMONx}\text{-}V_{VREF}=I_{OUT\_SPS}\times \frac{R_{SENSE}}{1k\Omega}\times 1.25\times R_{IMONx}$$

For multi-phase considerations, the ISENxN of each phase is suggested to be connected together. Figure 13 shows the implementation of a multi-phase SPS current sensing report. The V_{IMON} and current reporting from SPS can be calculated using the following equation:

$$V_{IMONx}\text{-}V_{VREF}=(I_{OUT\_SPS1}+I_{OUT\_SPS2}+\cdots+I_{OUT\_SPS8})\times\frac{R_{SENSE}}{1k\Omega}\times1.25\times R_{IMONx}$$

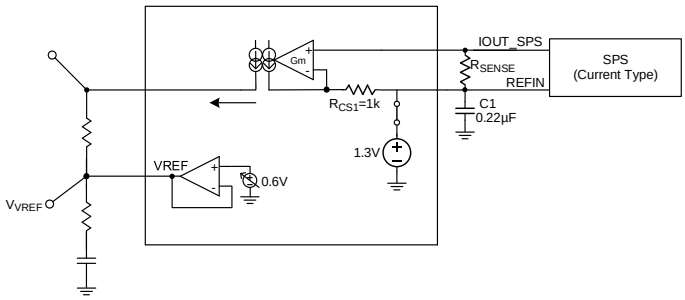


Figure 12. SPS Current Sensing

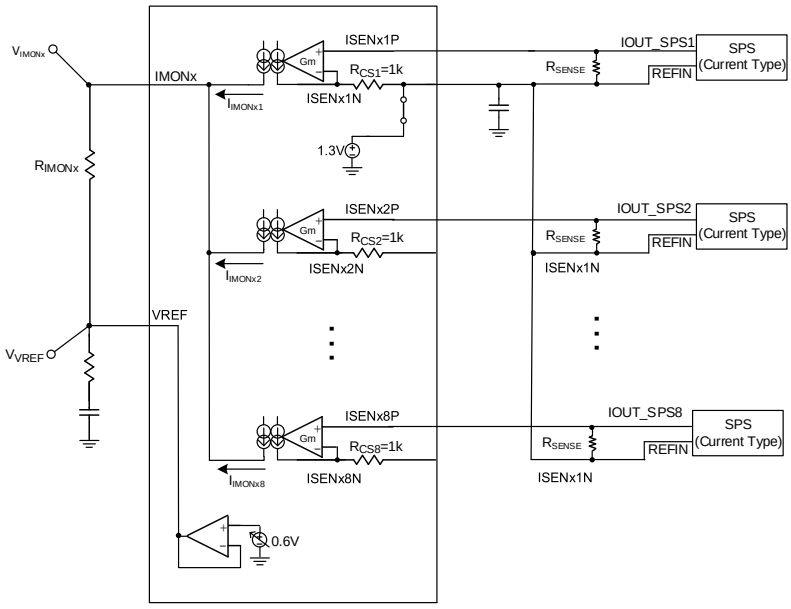


Figure 13. Total SPS Current Sensing

18.15 Thermal Compensation for Current Sense

Since the copper wire in an inductor is a positive temperature coefficient component, temperature compensation is necessary for the DCR inductor current sense. For a single-phase design, like rail B, a simple and effective way is adopted in Figure 14. An NTC thermistor is added into the current sense network. It is suggested to be placed near the inductor of the power stage to be well-compensated. The single-phase thermal compensation equation can be derived as follows:

$$V_{IMONB}\text{-}V_{VREF}=I_{LB}\times\frac{DCR}{R_{INT.}}\times\frac{R_S+R_P//R_{NTC}}{R+(R_S+R_P//R_{NTC})}\times1.25\times R_{IMONB}$$

For design suggestions calculated using this equation, refer to the intuitive RTPro Designer™ graphical user interface.

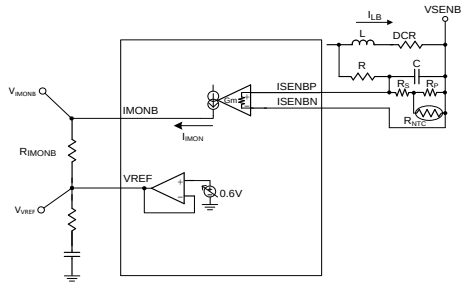


Figure 14. Single-Phase Thermal Compensation

For multi-phase designs like rail A, the RT3638AJ adopts a patented total current sense method with thermal compensation, as shown in Figure 15, which requires only one NTC thermistor. The NTC thermistor is combined in the network of the IMONA pin. It is suggested to be placed around the inductor of the first phase as close as possible. The multi-phase thermal compensation equation can be derived as follows:

$$V_{IMONA}-V_{VREF}=(I_{LA1}+I_{LA2}+\ \ldots\ +I_{LA8})\times\frac{DCR}{R_{INT.}}\times1.25\times R_{IMON,EQA}$$

For design suggestions calculated using this equation, refer to the intuitive RTPro Designer™ graphical user interface.

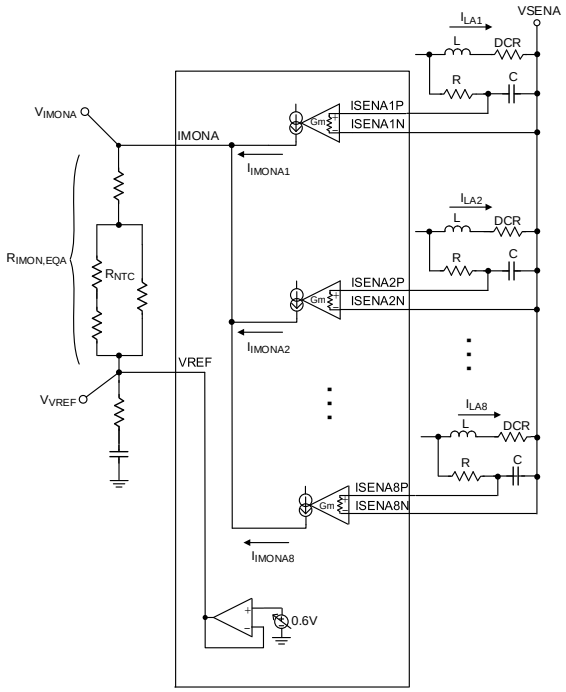


Figure 15. Multi-Phase Thermal Compensation

18.16 Loadline Setting (R_{LL})

The loadline system is adopted in CPU VR applications for power saving and output capacitance reduction. With a loadline system, the output voltage decreases proportionally to the increasing load current. The R_{LL} is defined as the slope of the straight line of V-I curve, as shown in Figure 16. The RT3638AJ provides the voltage and current loop

gain for adjusting R_{LL}. Figure 17 shows the voltage and current loop circuits. The R_{LL} formula is described as follows:

$$R_{LL} = \frac{\text{Current Loop Gain}}{\text{Voltage Loop Gain}} = \frac{DCR}{R_{INT.}} \times R_{IMON,EQ} \times \frac{A_i}{\frac{R_{EA2}}{R_{EA1}}} \times \frac{15}{4}$$

where A_i is the current gain which can be selected by SEL_Ai_GAINx. $\frac{R_{EA2}}{R_{EA1}}$ is the ERROR AMP gain and suggested to design within 2.5 to 3.5 for better transient response. The desired R_{LL} can be designed with the proper Ai and $\frac{R_{EA2}}{R_{EA1}}$.

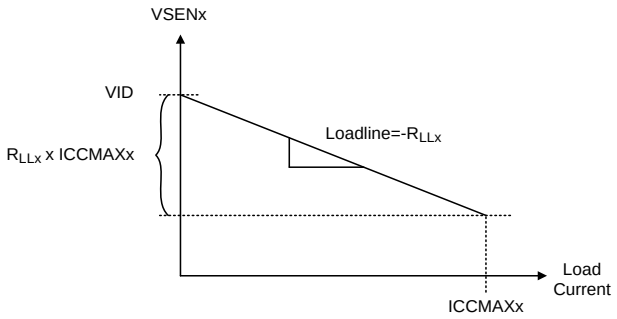


Figure 16. V-I Curve

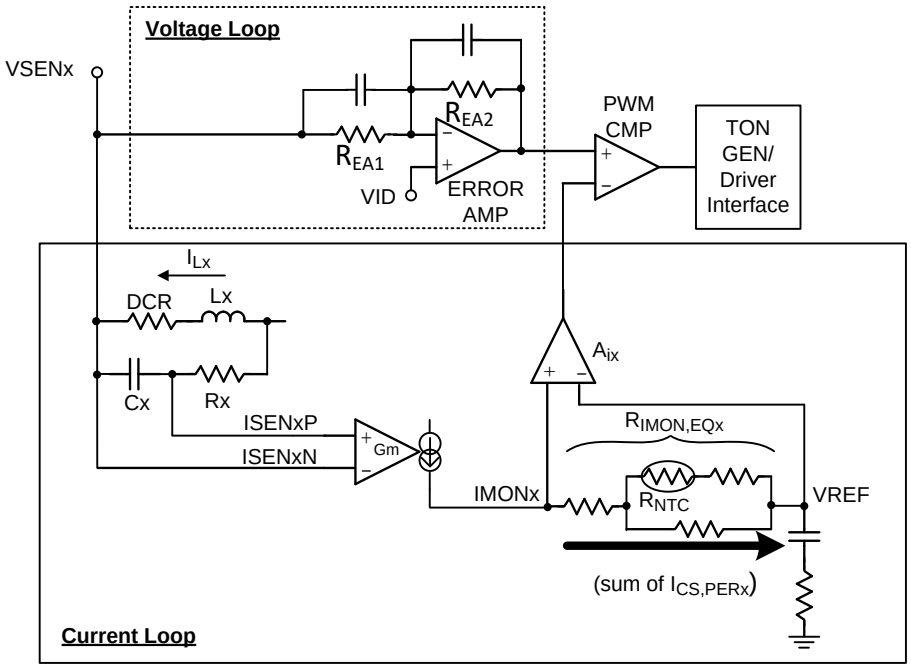


Figure 17. Voltage and Current Loop Circuit

18.17 Dynamic VID (DVID) Compensation

During a DVID up or down transition, the additional current is required to charge or discharge the output capacitors. This charging or discharging current approximates to the DVID slew rate multiplied by the output capacitance. With a loadline system, the additional charging or discharging current results in an undesired voltage droop so that the output voltage may not get in the tolerance band within the specified time. This voltage droop or lift can be estimated

by the formula: DVID Slew Rate x Output Capacitance x R_{LL}. This phenomenon is called the droop effect. Figure 18 shows the droop effect during a DVID up and down. The RT3638AJ provides an internal current source on the FBx pin to compensate for the droop effect. The compensation is equal to I_{DVID_LIFT} or I_{DVID_DROOP} times of R_{EA1}. For a DVID up, the amount of I_{DVID_LIFT} can be selected by SEL_I_DVID_LIFTx. Figure 19 reveals how the DVID up compensation works. Similarly, the amount of I_{DVID_DROOP} is also changeable via SEL_I_DVID_DROOPx for a DVID down, as shown in Figure 20. Compensation is also adjustable by changing R_{EA1}. When the DAC settles, a recovery time is needed for the inductor current settling to the DC load current. Output capacitors keep charging or discharging during this period (the magnitude is related to the inductor, capacitors, and VID). Thus, the DVID compensation is suggested to be less than DVID slew rate x output capacitance (de-rating should be considered). However, if the output capacitance is excessively large to compensate, adding a resistor and capacitor in series between FBx to GND can achieve a similar effect. Moreover, the compensator, which is the RC network of the ERROR AMP, also affects the behavior of DVID. The DVID compensation should be adjusted case-by-case.

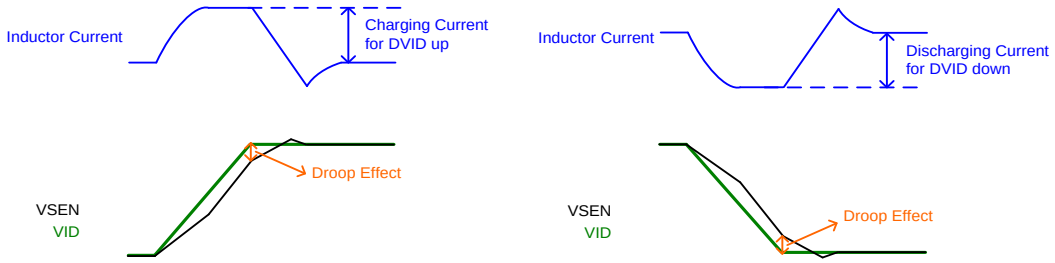


Figure 18. Droop Effect of DVID Up and Down Transitions

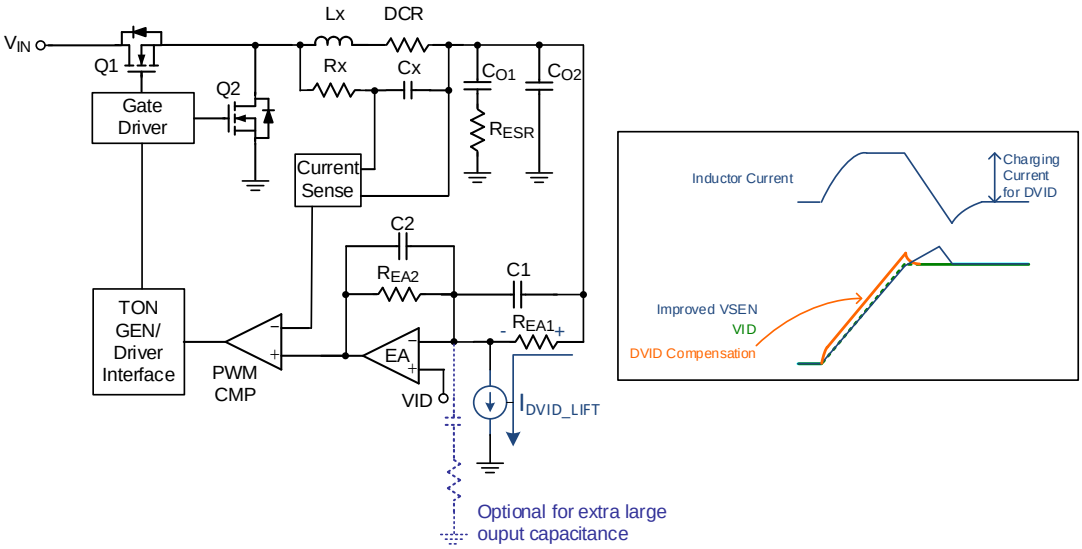


Figure 19. DVID Up Compensation

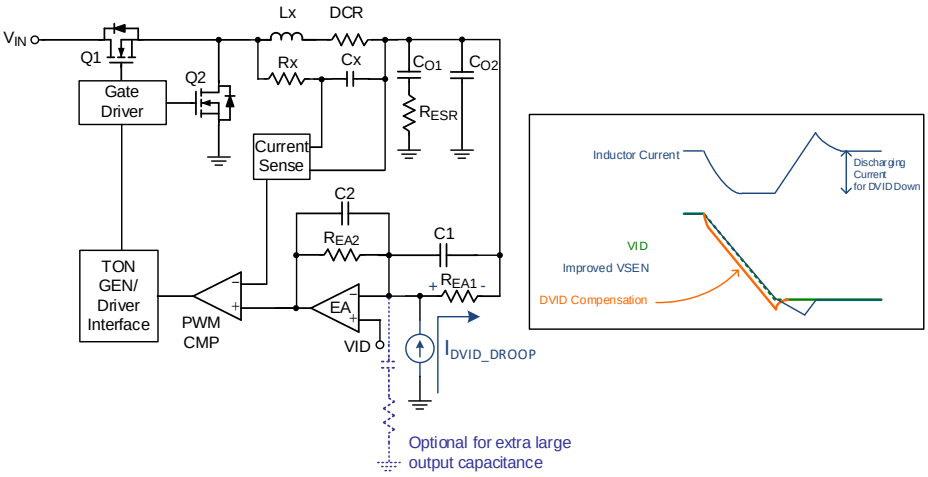


Figure 20. DVID Down Compensation

18.18 Ripple Compensation During DVID Transition

For better efficiency, the magnitude of the output voltage ripple will be different in low VID and high VID conditions due to the frequency control. The ripple difference may affect the output voltage reaching the tolerance band in time during DVID slew up and down caused by the DC offset cancellation mechanism, as shown in Figure 21. The RT3638AJ provides the ripple compensation during DVID transitions to eliminate the influence of the ripple difference by adding auxiliary compensation current when VID is between 0.3V to 0.9V, as shown in Figure 22. The ripple compensation can be selected from the registers EN_2X_RIPPLE_COMPx and SEL_RIPPLE_COMPx.

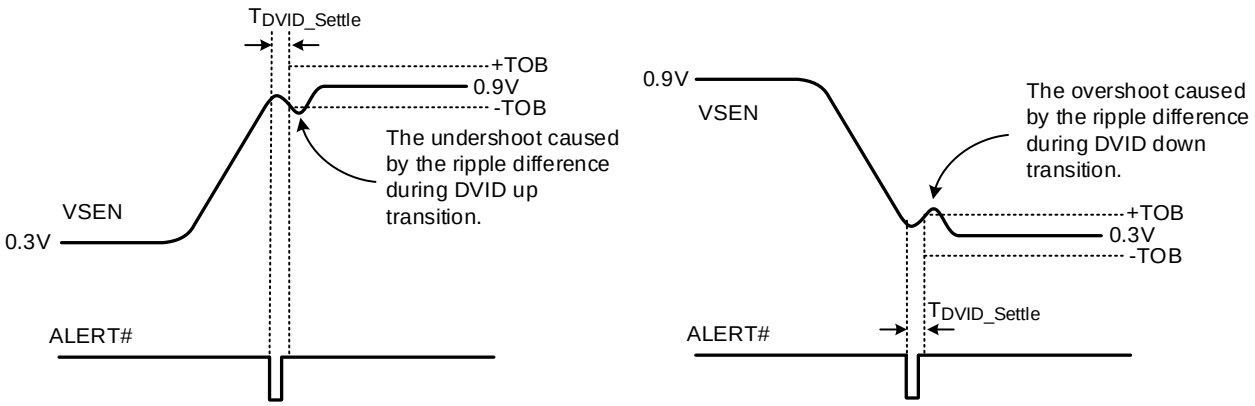


Figure 21. Ripple Difference Effect during DVID Up/Down Transition

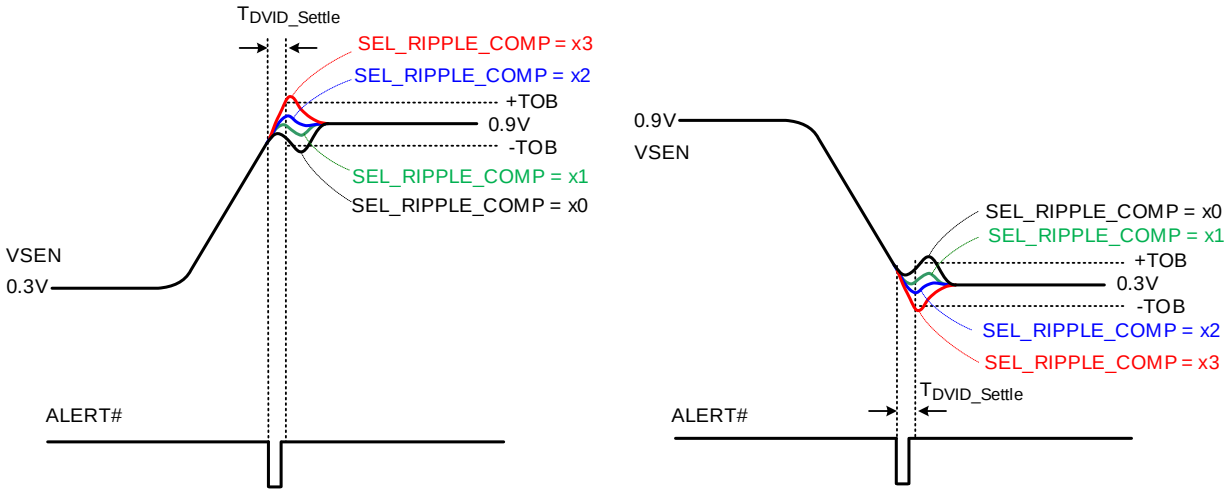


Figure 22. Ripple Compensation during DVID Up/Down Transition

18.19 Compensator Design

Benefiting from the G-NAVP™ topology, a simple type II compensator is sufficient for the RT3638AJ to meet the ACLL requirements. This one-pole one-zero compensator is illustrated in Figure 23. In order to meet IMVP9.2 specifications, it is suggested to adjust the positions of pole and zero based on the ring back level during load transients. For design suggestions, refer to the intuitive RTPro Designer™ graphical user interface.

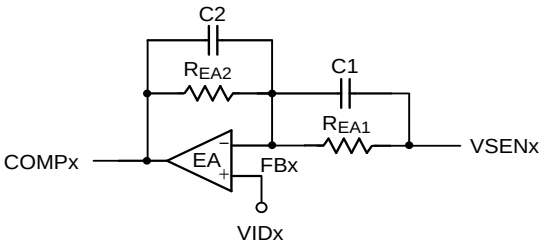


Figure 23. Type II Compensator

18.20 Differential Remote Sense

The RT3638AJ provides a differential remote sense to eliminate the effects of voltage drops due to the PCB traces, CPU internal power routes, and socket contacts. The RT3638AJ senses the on-die pins of CPU, VCC_SENSE, and VSS_SENSE, to provide accurate voltage at the remote CPU side. While the CPU is not mounted on the system, typically two 100-Ω resistors are required to provide the output voltage feedback. The circuit of the remote sense is shown in Figure 24.

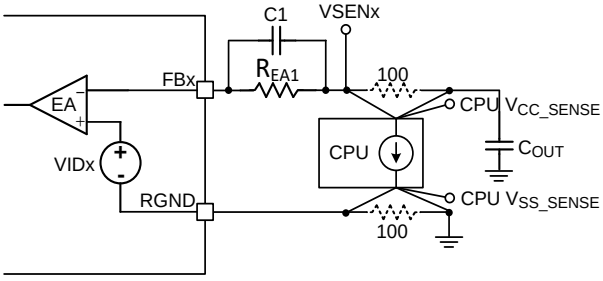


Figure 24. Remote Sense Circuit

18.21 Switching Frequency Setting

The G-NAVP™ topology is a kind of current mode constant-on-time control. It generates an adaptive T_{ON} of the PWM according to the input voltage VIN for better line regulation. T_{ON} is also adaptive to the VID voltage to achieve a constant switching frequency. The constant switching frequency operation simplifies the thermal estimation. K_{TON} is also a factor of T_{ON}, which is selectable via SEL_KTONx. The bit field definitions and the T_{ON} formula are listed in Table 4 and Table 5.

Table 4. T_{ON} Formula

Rail A	Rail B and C (VID Table = 5mV)	Rail B and C (VID Table = 10mV)
VID > 0.9V, $t_{ON} = 2\mu \times \frac{VID}{k_{TONA} \times V_{IN}} + 10ns$	VID > 0.9V, $t_{ON} = 2.206\mu \times \frac{VID}{k_{TONx} \times (V_{IN} - 0.9V)} + 15ns$	VID > 1.8V, $t_{ON} = 2.206\mu \times \frac{VID}{k_{TONx} \times (V_{IN} - 1.8V)} + 15ns$
VID ≤ 0.9V, $t_{ON} = 2\mu \times \frac{0.9V}{k_{TONA} \times V_{IN}} + 10ns$	0.3V < VID ≤ 0.9V, $t_{ON} = 1.9854\mu \times \frac{1}{k_{TONx} \times (V_{IN} - VID)} + 15ns$	0.3V < VID ≤ 1.8V, $t_{ON} = 1.9854\mu \times \frac{2}{k_{TONx} \times (V_{IN} - VID)} + 15ns$
	VID ≤ 0.3V, $t_{ON} = 1.9854\mu \times \frac{1}{k_{TONx} \times (V_{IN} - 0.3V)} + 15ns$	VID ≤ 0.3V, $t_{ON} = 1.9854\mu \times \frac{2}{k_{TONx} \times (V_{IN} - 0.3V)} + 15ns$

Table 5. Bit Field Definition of K_{TONx}

Bits \ Field Name	K_{TONA}	K_{TONB} and K_{TONC}
000	0.525	0.82
001	0.630	0.91
010	0.735	1.00
011	0.840	1.09
100	0.945	1.18
101	1.050	1.27
110	1.153	1.36
111	1.260	1.55

The switching frequency can be derived from t_{ON} as follows. The losses of the power stage and driver are considered.

$$Freq = \frac{VID + \frac{I_{CC}}{N} \times (DCR + \frac{R_{ONLS,max}}{n_{LS}} - N \times R_{LL})}{\left[V_{IN} + \frac{I_{CC}}{N} \times \left(\frac{R_{ONLS,max}}{n_{LS}} - \frac{R_{ONHS,max}}{n_{HS}}\right)\right] \times (t_{ON} - t_D + t_{ON,VAR}) + \frac{I_{CC}}{N} \times \frac{R_{ONLS,max}}{n_{LS}} \times t_D}$$

VID : VID Voltage
V_{IN} : Input Voltage
I_{CC} : Load Current
N : Phase Numbers
$R_{ONHS,max}$: Maximum High-Side $R_{DS,ON}$

n_{HS} : High-Side MOSFET Numbers
$R_{ON_{LS,max}}$: Maximum Low-Side $R_{DS,ON}$
n_{LS} : Low-Side MOSFET Numbers
t_D : High-Side MOSFET Delay Time plus Rising Time
$t_{ON,VAR}$: Variation of t_{ON}
DCR : Inductor DCR
R_{LL} : Loadline

18.22 Adaptive Quick Response (AQR)

The RT3638AJ provides Adaptive Quick Response (AQR) for optimizing transient response. The output voltage falling slew rate is detected and compared with the AQR threshold. When the slew rate is larger than the threshold, the PWM turns on to deliver more power to output portion. The PWM width is adaptive to the load step. The registers SEL_MPH_AQR_THx and SEL_1PH_AQR_THx are provided to select the threshold in multi-phase and single-phase operations. Refer to the following equation to set the initial AQR threshold.

$$\text{AQR threshold} = -4u \times \frac{dVSENx}{dt}$$

Note that the falling slew rate at steady state and recovery of overshoot should be considered for preventing false triggering AQR.

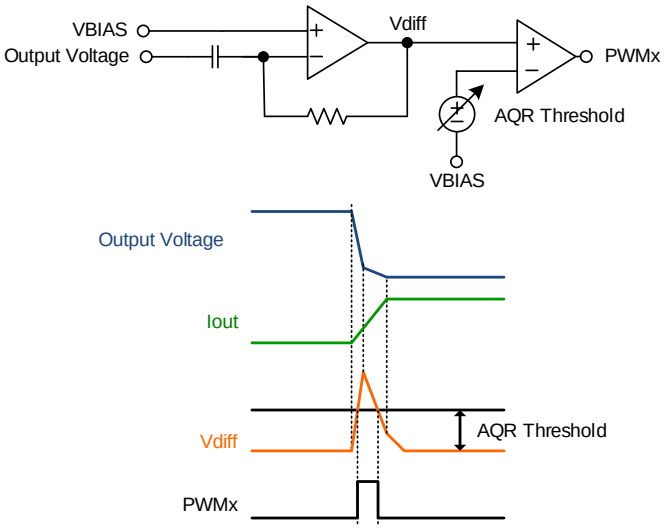


Figure 25. Adaptive Quick Response Mechanism

18.23 Anti-Overshoot (ANTI-OVS)

The RT3638AJ provides Anti-Overshoot function (ANTI-OVS) to suppress output voltage overshoot. The variation of COMPx is used to compare with the ANTI-OVS threshold. When the overshoot exceeds the threshold, all PWMs enter tri-state to turn off high-side and low-side MOSFETs. Since the low-side MOSFET is turned off, the continued positive inductor current flows through the body diode. The forward voltage of the body diode helps to discharge the inductor current faster and decrease the overshoot. Use the register SEL_ANTI_OVS_THx to select the threshold. Note that since COMPx is affected by the compensator, the final settings should be adjusted case-by-case.

$$\Delta COMP \times \frac{4}{3} = \Delta VSENx \times \frac{R_{EA2}}{R_{EA1}} \times \frac{4}{3} > \text{ANTI-OVS Threshold}$$

18.24 ACLL Performance Enhancement

The RT3638AJ provides another function Adaptive Ramp (AR) for improving undershoot of ACLL. Two AR thresholds for multi-phase and single-phase are compared with COMPx. In a multi-phase operation, when COMPx rises and reaches the threshold then triggers AR, the falling slew rate of RAMPx becomes sharper and the next PWM is generated earlier. The operation principle is in Figure 26. In a single-phase operation, when AR is triggered, an additional PWM pulse is generated directly, as shown in Figure 27. The registers SEL_MPH_AR_THx and SEL_1PH_AR_THx are provided for setting the threshold in multi-phase and single-phase operations. Moreover, a positive offset can be added on DAC or LPF. Refer to Table 43 and Table 44 for the detailed settings of registers 0x32 and 0x33, respectively. Note that the final settings should be adjusted case-by-case.

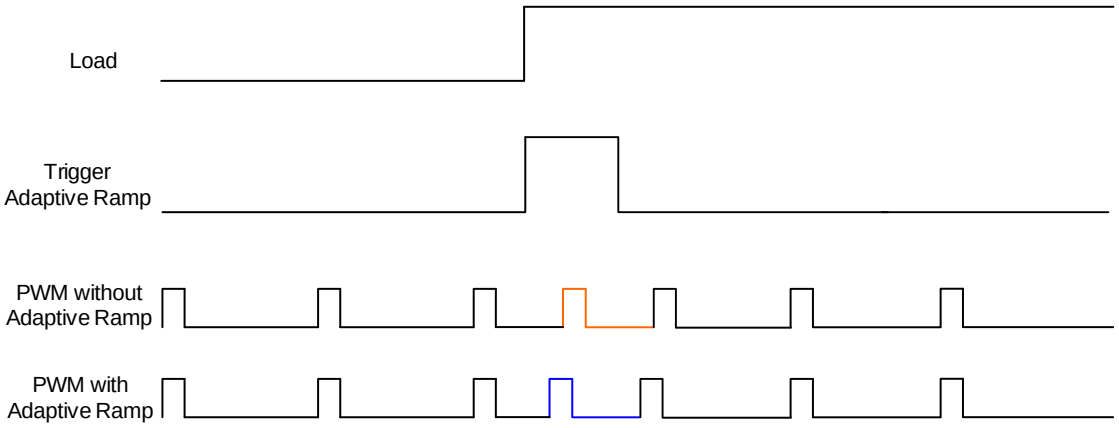


Figure 26. Adaptive Ramp Behavior in Multi-Phase Operation

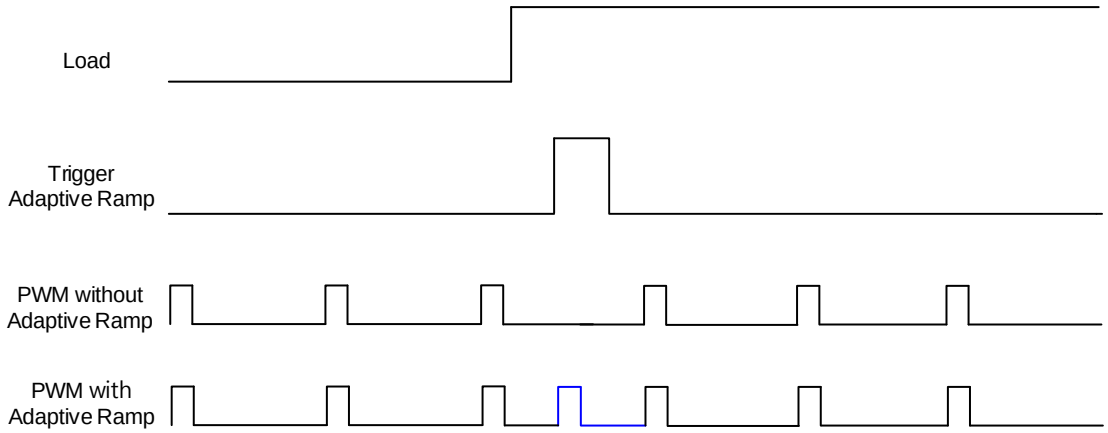


Figure 27. Adaptive Ramp Behavior in Single-Phase Operation

18.25 Current Limit

This function is designed for intel's Fast V-Mode operation. When the load current exceeds the VR current threshold set in the SVID register, the VR will limit the output current to the value specified in the SVID register and increment one count value in the SVID register. The RT3638AJ supports the $\overline{\text{VRHOT}}$ behavior during current limit. It can be disabled by EN_FASTV_VRHOT_ASSERTION, and has different logic while receiving the SetVID command by setting EN_FASTV_VRHOT_DEASSERTION.

18.26 Smart Phase Management (SPM)

The RT3638AJ provides the Smart Phase Management (SPM) to improve light-load efficiency and for the fast phase adding and phase shedding. The SPM function can be enabled and disabled via the I^2C register EN_SPMx. The controller compares V_{IMON} with the threshold and hysteresis of SPM to decide the number of phase adding and phase shedding. The IMON pin voltage (V_{IMON}) represents the total current. The threshold and hysteresis of SPM can be adjusted through the NVM registers of SEL_SPM_THx and SEL_SPM_HYSx, as shown in Figure 28. For example, for rail A, set the SEL_SPM_THA8 = 40% of ICCMAXA to drive the 8-phase operation when the V_{IMON} exceeds 40% of ICCMAX of rail A. Moreover, the SEL_SPM_THx can be derating using the SEL_SPM_TH_RATIO setting. The hysteresis of SPM can be adjusted through the NVM register of SEL_SPM_HYSx. For example, setting the SEL_SPM_HYSA7 = 5% of ICCMAXA with SEL_SPM_THA7 = 40% of ICCMAXA, will drive the 7-phase operation when the V_{IMON} falls below 35% of ICCMAXA (SEL_SPM_THA7 – SEL_SPM_HYSA7). Moreover, the SEL_SPM_HYSx can be extended using the EN_2X_SPM_HYS setting. The controller enters the diode emulation mode (DEM) automatically when the inductor current drops below the zero-current detection threshold (ZCD). There is no delay time during phase adding from a lower to a higher phase number operation. The delay time during the phase shedding from a higher to a lower phase number operation can be set through the SEL_SPM_SHED_DLYx setting,as shown in Figure 29. In addition to comparing the output current, the RT3638AJ is designed to operate at full phase immediately during three specific events: a DVID up, a DVID down, and when the AQR function is triggered during transient response.

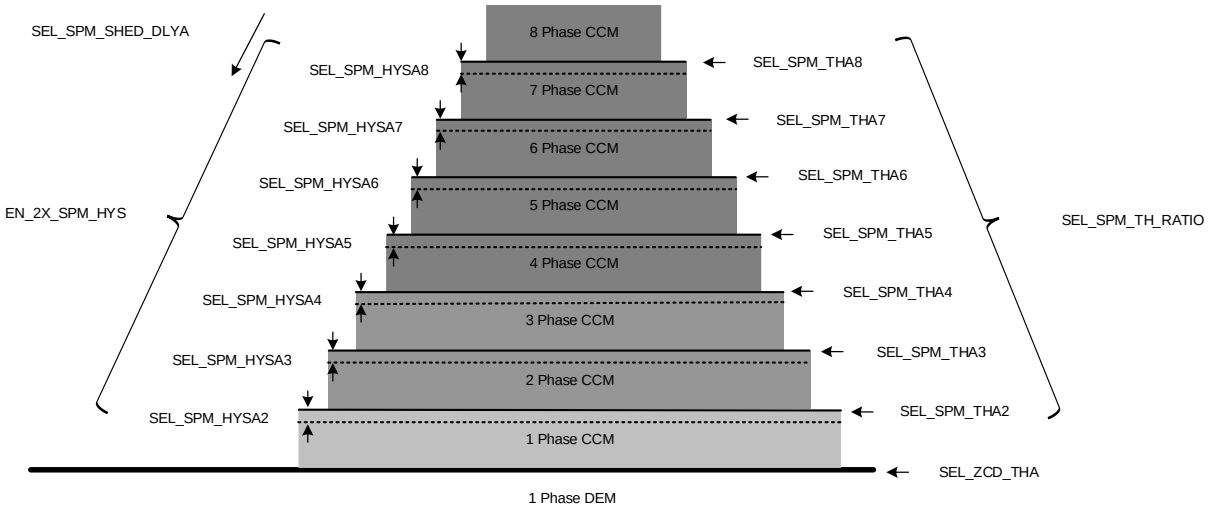


Figure 28. Smart Phase Management Rail A 8-phase Operator Phase Diagram

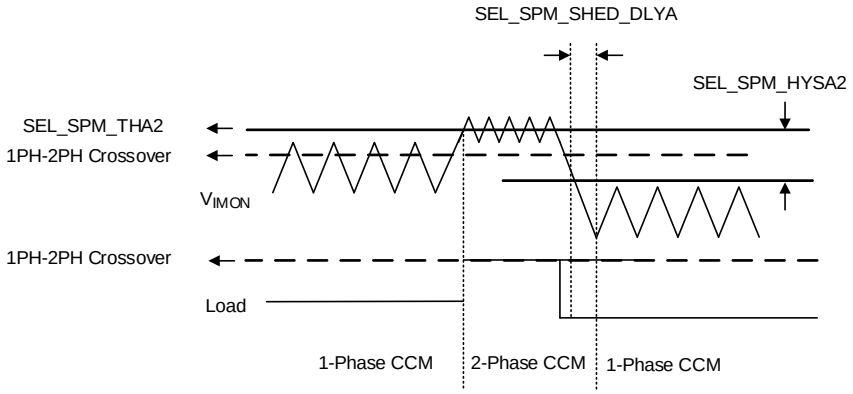


Figure 29. Smart Phase Management Up and Down Phase Diagram

18.27 Overcurrent Protection (OCP)

The RT3638AJ provides two overcurrent protection mechanisms: soft-start period (SS-OCP) and normal operation (SUM-OCP) for protecting the power stage. Once OCP is triggered, VR_READY is de-asserted and the PWM enters a tri-state condition to turn high-side and low-side MOSFETs off. Also, the protection flag rises to 2V of VREF and asserts the OCx bit in the I^2C command PROT_FLAGx.

The SS-OCP threshold can be configured via SET_SS_OCPx. The debounce time of SS-OCP is around 0.5μs. The detection window of SS-OCP is the soft-start period plus extra 60μs. The threshold formula is shown as follows:

$$V_{IMONx} = \frac{SET\_SS\_OCPx}{ICCMAXx} \times dVIMONx\_ICCMAX + V_{VREF}$$

For example, for rail A, parameters are assumed as follows:

ICCMAXA = 280A,

SET_SS_OCPA = 560A = 0x8C,

$$V_{IMONA} = \frac{560}{280} \times 0.4 + 0.6 = 1.4V$$

The SUM-OCP threshold can be configured via SET_SUM_OCPx. The debounce time is also adjustable via SUM_OCP_DEB_TIMEx. SUM-OCP is masked for 80μs after settling of the DVID transition. The SUM-OCP behavior is depicted in Figure 30. The threshold formula is shown as follows:

$$V_{IMONx} = \frac{SET\_SUM\_OCPx}{ICCMAXx} \times dVIMONx\_ICCMAX \times \frac{Current\ Operation\ Phase}{Maximum\ Operation\ Phase} + V_{VREF}$$

For example, for rail A, parameters are assumed as follows:

ICCMAXA = 280A,

SET_SUM_OCPA = 280x1.3 = 364A = 0x5B,

Current Operation Phase = 8,

Maximum Operation Phase = 8,

$$V_{IMONA} = \frac{364}{280} \times 0.4 \times \frac{8}{8} + 0.6 = 1.12V$$

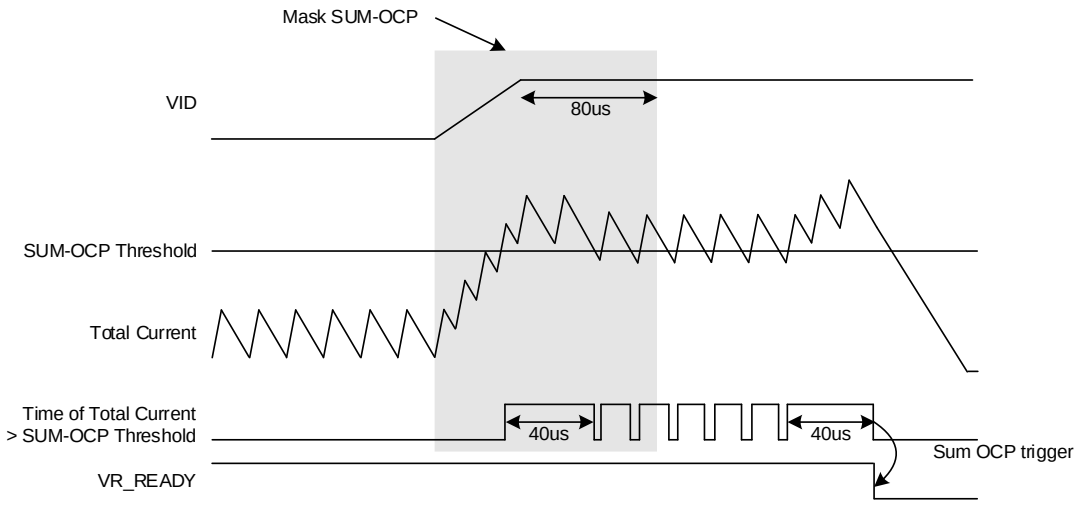


Figure 30. SUM-OCP Behavior

18.28 Undervoltage Protection (UVP)

The RT3638AJ features built-in UVP. The UVP threshold is set to DAC minus 650mV. The debounce time is 3μs. When UVP is triggered, the PWM enters a tri-state condition to turn high-side and low-side MOSFETs off. Also, the protection flag rises to 1.5V of VREF and asserts the UVx bit in the I^2C command PROT_FLAGx. UVP is masked for 80μs after DVID has stabilized. The mechanism is illustrated in Figure 31.

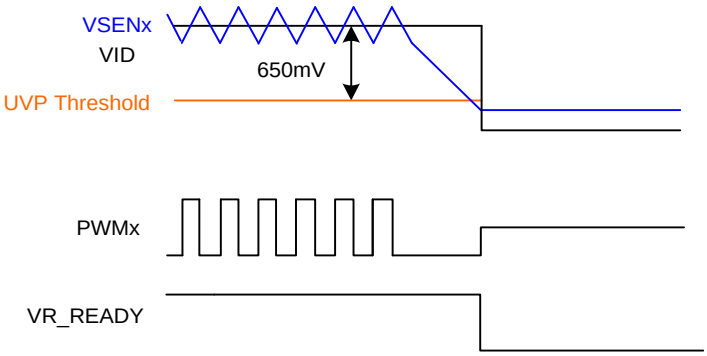


Figure 31. UVP Behavior

Table 6. Summary of OVP and UVP

Protection Type	Protection Threshold	Protection Flag	Protection Action	DVID Mask Time	Protection Reset
SS-OCP	$V_{IMONx}=\frac{SET\_SS\_OCPx}{ICCMAXx}\times dVIMONx\_ICCMAX+V_{VREF}$	V_{VREF} = 2V	PWM tri-state, VR_READY latched low	DVID+ 80μs	VCC/EN Toggle
SUM-OCP	$V_{IMONx}=\frac{SET\_SUM\_OCPx}{ICCMAXx}\times dVIMONx\_ICCMAX \times \frac{Current\ Operation\ Phase}{Maximum\ Operation\ Phase}+V_{VREF}$				
UVP	VID-650mV Rail A supports 650mV and 850mV UV threshold in SEL_UV_THA	V_{VREF} = 1.5V			

18.29 Overvoltage Protection (OVP)

The RT3638AJ provides two overvoltage protection mechanisms: absolute overvoltage protection (AOVP) for the soft-start period and relative overvoltage protection (ROVP) for normal operation. The debounce time of OVP is around 0.5μs. Once OVP is triggered, VR_READY is de-asserted and the PWM outputs a low state first. When VID is below the OVP threshold minus 0.35V, the PWM enters a tri-state condition. After 60μs since OVP is triggered, the PWM outputs pulse with a limited high level at the tri-state level to decrease VID with slow slew rate. Also, the protection flag rises to 1V of VREF and asserts the OVx bit in the I^2C command PROT_FLAGx. OVP is masked in internal setting mode, When DAC is disabled and in PS4. The summary of OVP is in Table 7.

AOVP is used to detect the soft-start period and ends at the first PWM pulse of DVID settles. The AOVP threshold can be configured via SEL_SS_OVPx. The behavior is illustrated in Figure 32.

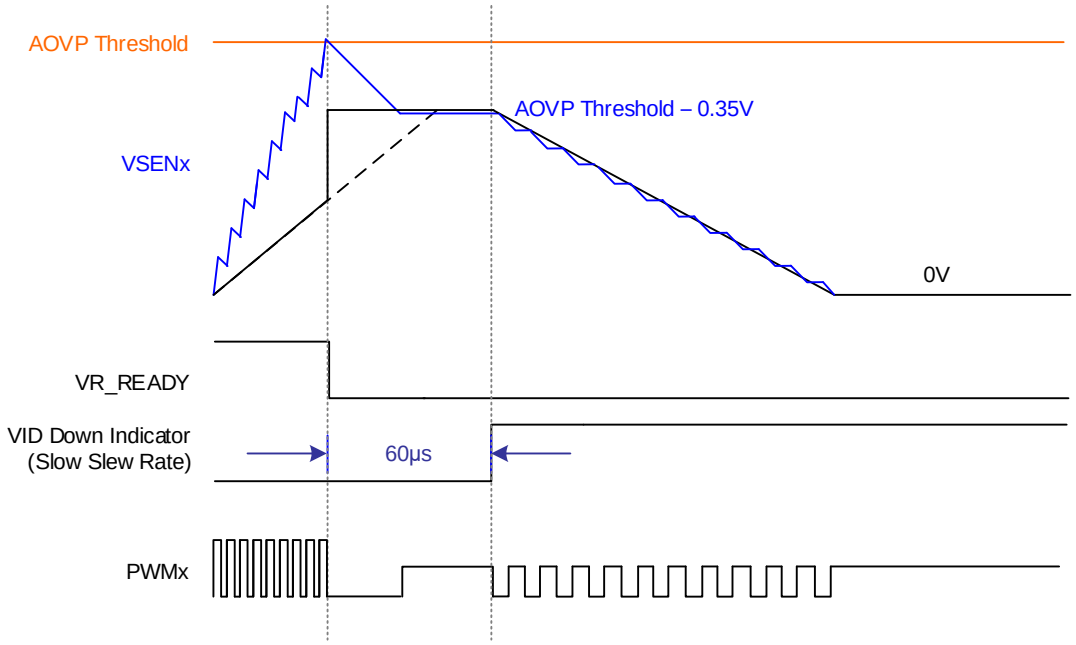


Figure 32. AOVP Behavior

ROVP is functional in normal operation. The threshold is set to DAC plus 350mV. The behavior is illustrated in Figure 33.

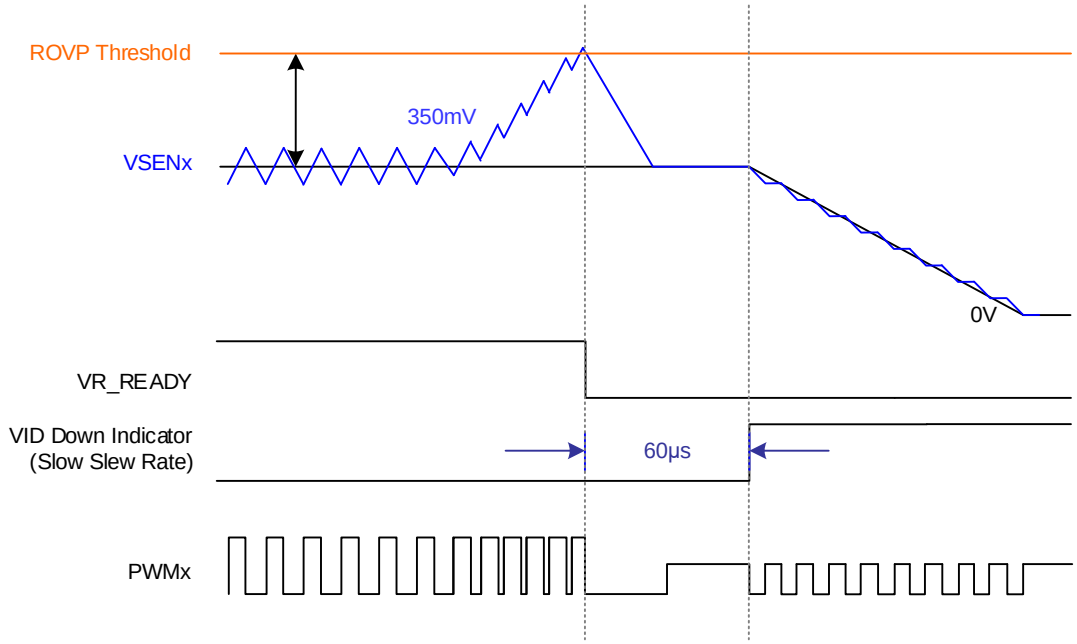


Figure 33. ROVP Behavior

Table 7. Summary of OVP

VID Condition	OVP Threshold	Example	Protection Flag	Protection Reset
VID = 0 (EN = L, internal setting mode, DAC off, PS4)	OVP is masked	NA	V_{VREF} = 1V	VCC/EN Toggling
DVID up from 0V to 1st PWM pulse of DVID settles	Set by SEL_SS_OVPx + SEL_DELTA_OVPx	SEL_SS_OVPx = 2.1V SEL_DELTA_OVPx = 350mV SS-OVP Threshold = 2.45V		
DVID period from non-zero VID (DAC ≠ 0)	DAC > 1.0V, DAC + SEL_DELTA_OVPx	DAC = 1.2V SEL_DELTA_OVPx = 350mV ROVP Threshold = 1.55V		
	DAC ≤ 1.0V, 1V + SEL_DELTA_OVPx	DAC = 0.9V SEL_DELTA_OVPx = 400mV AOVP Threshold = 1.4V		

18.30 CRC Failure

The RT3638AJ begins NVM loading once VCC surpasses it's the rising POR_NVM threshold. The RT3638AJ will download NVM into the control registers. A CRC check ensures the completion of the configuration download from NVM to the RT3638AJ control registers. During the configuration download, if there is a CRC failure the controller will not exit the Inactive state and will assert the I^2C register NVM_PROGRAM_STATUS [0].

18.31 Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the

difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula:

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a WQFN-68L 8x8 package, the thermal resistance, θ_{JA}, is 26.3°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below:

$P_{D(MAX)}$ = (125°C – 25°C) / (26.3°C/W) = 3.8W for a WQFN-68L 8x8 package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curve in Figure 34 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

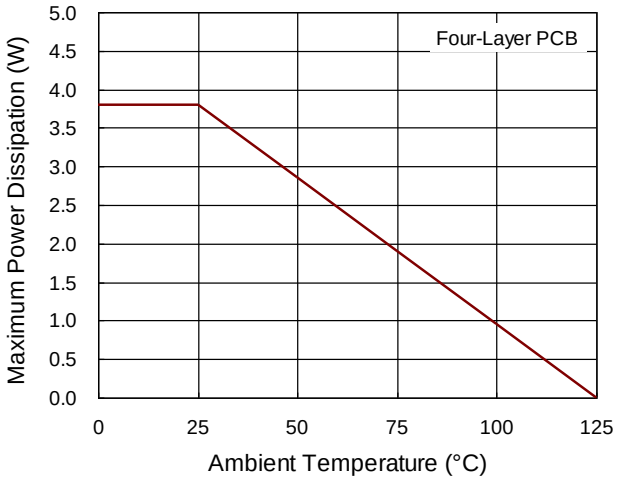


Figure 34. Derating Curve of Maximum Power Dissipation

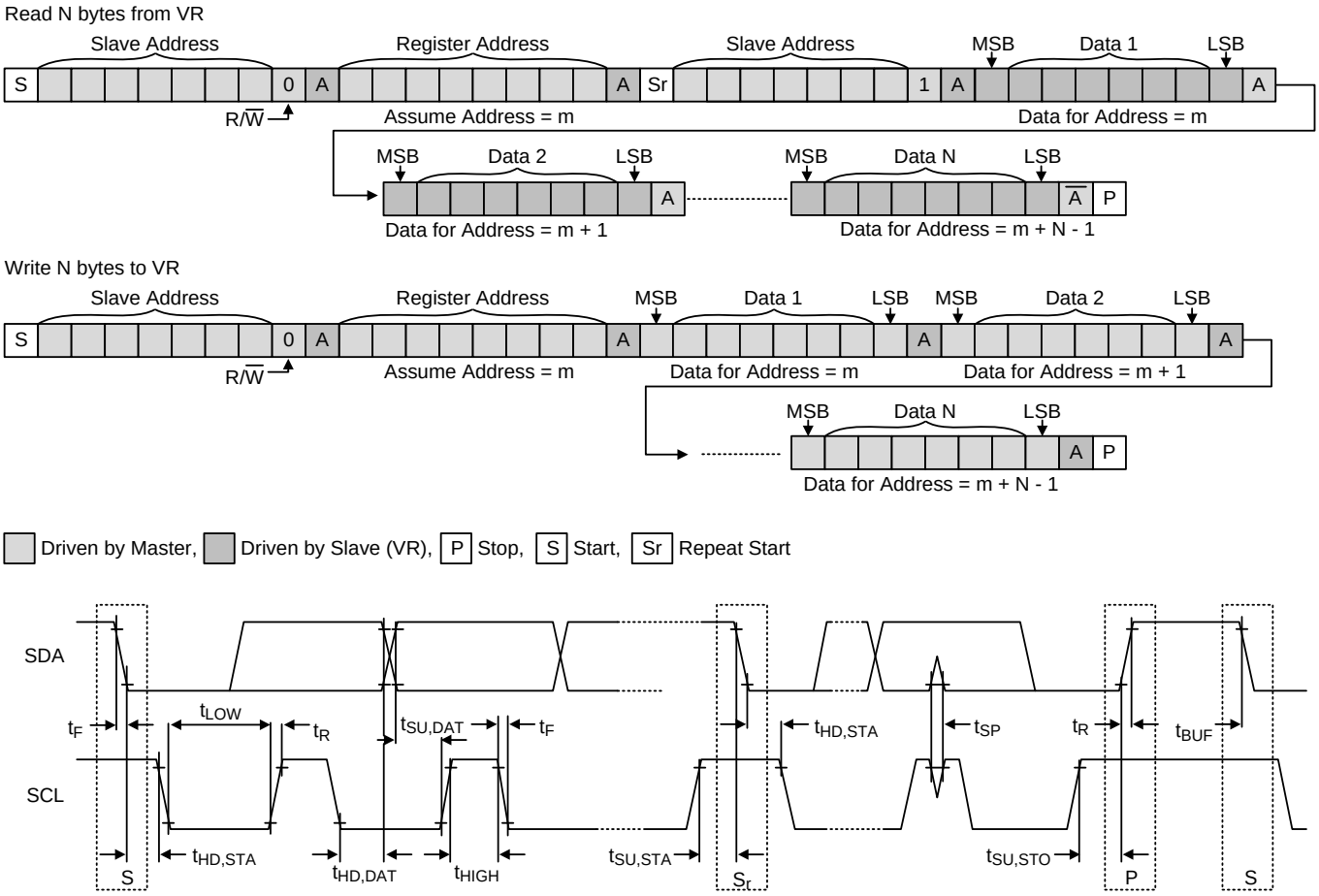
Note 6. The information provided in this section is for reference only. The customer is solely responsible for the designing, validating, and testing your product incorporating Richtek's product and ensure such product meets applicable standards and any safety, security, or other requirements.

19 Functional Register Description

The I^{2}C target address is configured by connecting the SD_GOOD pin to GND using a resistor. Refer to Table 2 for detailed descriptions.

This I^{2}C interface does not have a stretch function.

The I^{2}C interface supports standard target mode (100kbps) and fast mode (400kbps). The write or read bit stream (N > 1) is shown below:



All reserved bit(s) must be kept at their default values.

Table 8. Register List

Page	Address	Register Name	Default	Type	Paged	NVM
0x82	0x10	SET_ICCMAXA	0xC8	RW	Yes	Yes
0x82	0x11	SET_ICCMAX_RATIOA & EN_0LLA & EN_0LLB & EN_0LLC & EN_FASTV_VRHOT_ASSERTION & SEL_FAST_SR	0x8C	RW	Yes	Yes
0x82	0x12	SET_ICCMAXB	0x3D	RW	Yes	Yes
0x82	0x13	SET_ICCMAXC	0x27	RW	Yes	Yes
0x82	0x14	SET_ICCMAXD	0x21	RW	Yes	Yes
0x82	0x15	SEL_VBOOT_CONFIGA & SEL_KTONA & SEL_VBOOT_CONFIGB & SEL_KTONB	0x34	RW	Yes	Yes
0x82	0x16	SEL_VBOOT_CONFIGC & SEL_KTONC & SEL_PWM_HIZ_VOL & SEL_CS_TYPEA & SEL_CS_TYPEB & SEL_CS_TYPEC	0x48	RW	Yes	Yes
0x82	0x17	EN_FASTV_VRHOT_DEASSERTION & SEL_VID_TABLEA & SEL_VID_TABLEB & SEL_VID_TABLEC & SEL_SMALL_LLA	0x80	RW	Yes	Yes
0x82	0x18	SEL_SMALL_LLB & SEL_SMALL_LLC	0x00	RW	Yes	Yes
0x82	0x19	SEL_Ai_GAINA & SEL_Ai_GAINB & SEL_Ai_GAINC	0x3B	RW	Yes	Yes
0x82	0x1A	SEL_MPH_AR_THA & SEL_MPH_AQR_THA	0x43	RW	Yes	Yes
0x82	0x1B	SEL_ANS_BEHAV & SEL_1PH_AR_THA & SEL_1PH_AQR_THA	0x23	RW	Yes	Yes
0x82	0x1C	SEL_1PH_AR_THB & SEL_1PH_AQR_THB	0x1F	RW	Yes	Yes
0x82	0x1D	SEL_1PH_AR_THC & SEL_1PH_AQR_THC	0x1F	RW	Yes	Yes
0x82	0x1E	SEL_ZCD_THA	0x24	RW	Yes	Yes
0x82	0x1F	EN_MT_TO_X1_RAMPA & SEL_ZCD_THB	0x1D	RW	Yes	Yes
0x82	0x20	EN_EX_1UA_LPF_INITA & SEL_ZCD_THC	0x1D	RW	Yes	Yes
0x82	0x21	SET_SS_OCPA	0xC8	RW	Yes	Yes

Page	Address	Register Name	Default	Type	Paged	NVM
0x82	0x22	SEL_LPF_INITA & SET_SS_OCPB	0x19	RW	Yes	Yes
0x82	0x23	EN_SPM_DEFAULTB & EN_SPM_DEFAULTC & SET_SS_OCPC	0x19	RW	Yes	Yes
0x82	0x24	SEL_FASTV_CLAMPA & EN_FASTV_EX_TOFFBC & SEL_FASTV_TOFFB & SEL_FASTV_DLYB	0x1A	RW	Yes	Yes
0x82	0x25	EN_2X_RIPPLE_COMPA & SEL_RIPPLE_COMPA & SEL_FASTV_TOFFC & SEL_FASTV_DLYC	0x0A	RW	Yes	Yes
0x82	0x26	SEL_I_DVID_LIFTA & SEL_I_DVID_LIFTB	0x54	RW	Yes	Yes
0x82	0x27	SEL_I_DVID_LIFTC & EN_SPM_DEFAULTA & SEL_UV_THA & EN_UVA	0x53	RW	Yes	Yes
0x82	0x28	SEL_DELTA_OVPA & SEL_DELTA_OVPB & SEL_DELTA_OVPC	0x00	RW	Yes	Yes
0x82	0x29	Reserved	0x80	RW	Yes	Yes
0x82	0x2A	SEL_PSYS_LEVEL & SEL_DRVEN_F & EN_DRVEN_TO_DRVEN_F & EN_RT_SPS & SEL_FASTV_DLYA	0x45	RW	Yes	Yes
0x82	0x2B	SEL_SUM_OCP_DEB_TIMEA & SEL_SUM_OCP_DEB_TIMEB & SET_SUM_OCPB	0xD4	RW	Yes	Yes
0x82	0x2C	SEL_SUM_OCP_DEB_TIMEC & SET_SUM_OCPC	0xCC	RW	Yes	Yes
0x82	0x2D	EN_2X_KTON & EN_AR_LIFT_VIDB & SEL_SS_OVPA & SEL_SS_OVPB & SEL_SS_OVPC	0x40	RW	Yes	Yes
0x82	0x2E	SEL_ANTI_OVS_THA & SEL_ANTI_OVS_THB	0xBF	RW	Yes	Yes
0x82	0x2F	EN_AR_LIFT_VIDC & SEL_ANTI_OVS_THC & EN_QR_LIFT_VIDB & EN_SS_OCPA & EN_SS_OCPB & EN_SS_OCPC	0xF7	RW	Yes	Yes

Page	Address	Register Name	Default	Type	Paged	NVM
0x82	0x30	EN_EX_10MV_LIFT_VIDA & SEL_1PH_QR_MODEA & SEL_1PH_QR_WIDTHA & SEL_LIFT_VIDA & SEL_MPH_QR_MODEA & SEL_MPH_QR_WIDTHA	0x0E	RW	Yes	Yes
0x82	0x31	EN_EX_TONA & SEL_EX_TON_WIDTHA & SEL_EX_TON_THA	0xE7	RW	Yes	Yes
0x82	0x32	EN_MPH_QR_LIFT_VIDA & EN_1PH_QR_LIFT_VIDA & EN_MPH_AR_LIFT_VIDA & EN_1PH_AR_LIFT_VIDA & SEL_QR_LIFT_VID_RECOVERY_TIMEA & SEL_AR_LIFT_VID_RECOVERY_TIMEA & SEL_QR_LIFT_VIDA & SEL_AR_LIFT_VIDA	0x1B	RW	Yes	Yes
0x82	0x33	EN_MPH_QR_LIFT_LPFA & EN_1PH_QR_LIFT_LPFA & EN_ MPH_AR_LIFT_LPFA & EN_1PH_AR_LIFT_LPFA & EN_MPH_LIFT_LPFA & EN_1PH_LIFT_LPFA	0x91	RW	Yes	Yes
0x82	0x34	EN_HF_ACLL_QRA & SEL_HF_ACLL_QR_FREQA & EN_HF_ACLL_SQRA & SEL_HF_ACLL_SQR_FREQA	0xCA	RW	Yes	Yes
0x82	0x35	EN_EX_25MV_FLT _RAMPB & SEL_HF_ACLL_QR_FREQB	0x79	RW	Yes	Yes
0x82	0x36	SEL_QR_WIDTHB & SEL_FLT_RAMPB	0xC7	RW	Yes	Yes
0x82	0x37	EN_QR_LIFT_VIDC & EN_EX_TONB & SEL_EX_TON_WIDTHB & SEL_EX_TON_THB	0x01	RW	Yes	Yes
0x82	0x38	EN_EX_25MV_FLT_RAMPC & SEL_HF_ACLL_QR_FREQC	0x79	RW	Yes	Yes
0x82	0x39	SEL_QR_WIDTHC & SEL_FLT_RAMPC	0xC7	RW	Yes	Yes
0x82	0x3A	EN_EX_TONC & SEL_EX_TON_WIDTHC & SEL_EX_TON_THC	0x01	RW	Yes	Yes
0x82	0x3B	SEL_PH_TYPEA & SEL_PH_TYPEB & SEL_PH_TYPEC	0x00	RW	Yes	Yes
0x82	0x3C	SET_SUM_OCPA	0x82	RW	Yes	Yes
0x82	0x3D	SET_IMON_RPT_OFSA	0x80	RW	Yes	Yes
0x82	0x3E	SET_IMON_RPT_OFSB	0x00	RW	Yes	Yes
0x82	0x3F	SET_IMON_RPT_OFSC	0x00	RW	Yes	Yes

Page	Address	Register Name	Default	Type	Paged	NVM
0x82	0x40	SEL_PSK_LIFT_VID	0xCF	RW	Yes	Yes
0x82	0x41	EN_AUTO_TONA & SEL_AUTO_TON_MAXA & EN_AUTO_TONB & SEL_AUTO_TON_MAXB	0xBB	RW	Yes	Yes
0x82	0x42	EN_AUTO_TONC & SEL_AUTO_TON_MAXC	0xB8	RW	Yes	Yes
0x82	0x43	Reserved	0xFF	RW	Yes	Yes
0x82	0x44	SEL_HOLD_LPF_THA & SEL_HOLD_LPF_THB & SEL_HOLD_LPF_THC	0xCB	RW	Yes	Yes
0x82	0x45	SEL_RST_LPF_CURRA & SEL_RST_LPF_CURRB & SEL_RST_LPF_CURRC	0xB3	RW	Yes	Yes
0x82	0x46	EN_ANSA & EN_ANSB & EN_ANSC	0xF8	RW	Yes	Yes
0x82	0x47	SEL_I_DVID_DROOPA & SEL_LIFT_VIDB & SEL_I_DVID_DROOPB	0x82	RW	Yes	Yes
0x82	0x48	SEL_LIFT_VIDC & SEL_I_DVID_DROOPC	0x1F	RW	Yes	Yes
0x82	0x49	SEL_MPH_LPF_LIMITA & SEL_MPH_LPF_LIMIT_HYSA	0x72	RW	Yes	Yes
0x82	0x4A	SEL_1PH_LPF_LIMITA & SEL_1PH_LPF_LIMIT_HYSA	0x34	RW	Yes	Yes
0x82	0x4B	Reserved	0x17	RW	Yes	Yes
0x82	0x4C	Reserved	0x71	RW	Yes	Yes
0x82	0x4D	SEL_1PH_LPF_LIMITB & SEL_1PH_LPF_LIMITC	0x47	RW	Yes	Yes
0x82	0x4E	SEL_LPF_INITB & SEL_LPF_INITC	0x22	RW	Yes	Yes
0x82	0x50	SET_VBOOTA	0x00	RW	Yes	Yes
0x82	0x51	Reserved	0xA1	RW	Yes	Yes
0x82	0x52	SET_VBOOTB	0x00	RW	Yes	Yes
0x82	0x53	Reserved	0xA1	RW	Yes	Yes
0x82	0x54	SET_VBOOTC	0x00	RW	Yes	Yes
0x82	0x55	Reserved	0xA1	RW	Yes	Yes
0x82	0x56	EN_2X_RIPPLE_COMPB & SEL_RIPPLE_COMPB & EN_2X_RIPPLE_COMPC & SEL_RIPPLE_COMPC	0x00	RW	Yes	Yes
0x82	0x57	SEL_SPM_HYSA2 & SEL_SPM_THA2	0x5E	RW	Yes	Yes
0x82	0x58	SEL_SPM_HYSA3 & SEL_SPM_THA3	0x3C	RW	Yes	Yes

Page	Address	Register Name	Default	Type	Paged	NVM
0x82	0x59	SEL_SPM_HYSA4 & SEL_SPM_THA4	0x3A	RW	Yes	Yes
0x82	0x5A	SEL_SPM_HYSA5 & SEL_SPM_THA5	0x39	RW	Yes	Yes
0x82	0x5B	SEL_SPM_HYS6 & SEL_SPM_THA6	0x38	RW	Yes	Yes
0x82	0x5C	SEL_SPM_HYS7 & SEL_SPM_THA7	0x35	RW	Yes	Yes
0x82	0x5D	SEL_SPM_HYS8 & SEL_SPM_THA8	0x33	RW	Yes	Yes
0x82	0x5E	EN_2X_SPM_HYS & SEL_SPM_TH_RATIO & SEL_SPM_SHED_DLYA	0xAC	RW	Yes	Yes
0x82	0x5F	SEL_ZCD_HYSB & SEL_ZCD_HYSC	0x05	RW	Yes	Yes
0x82	0x60	SEL_ANS_PS4_BEHAV & EN_DBLR_SPM_1PH_CCM & EN_SPS_TSENA & EN_SPS_TSENB & EN_SPS_TSENC	0x38	RW	Yes	Yes
0x82	0x61	SEL_SPM_SHED_DLYB & SEL_SPM_SHED_DLYC & SEL_PIN51_CONFIG & EN_2X_Ai_GAINA	0x00	RW	Yes	Yes
0x82	0x62	SET_SPS_TSEN_RPT_OFSA	0x20	RW	Yes	Yes
0x82	0x63	SET_SPS_TSEN_RPT_OFSB	0x20	RW	Yes	Yes
0x82	0x64	SET_SPS_TSEN_RPT_OFSC	0x20	RW	Yes	Yes
0x82	0x65	Reserved	0x00	RW	Yes	Yes
0x82	0x66	EN_RAIL	0x00	RW	Yes	Yes
0x82	0x67	Reserved	0x00	RW	Yes	Yes
0x82	0x68	Reserved	0x00	RW	Yes	Yes
0x82	0x69	Reserved	0x00	RW	Yes	Yes
0x82	0x6A	Reserved	0x00	RW	Yes	Yes
0x82	0x6B	Reserved	0x00	RW	Yes	Yes
0x82	0x6C	Reserved	0x00	RW	Yes	Yes
0x82	0x6D	Reserved	0x00	RW	Yes	Yes
0x82	0x6E	Reserved	0x00	RW	Yes	Yes
0x82	0x6F	Reserved	0x00	RW	Yes	Yes
0x82	0x70	SET_CODE_VER_LB	0x00	RW	Yes	Yes
0x82	0x71	SET_CODE_VER_HB	0x00	RW	Yes	Yes
0x82	0x72	Reserved	0x00	RW	Yes	Yes
0x82	0x73	Reserved	0x00	RW	Yes	Yes
0x82	0x74	SET_PRODUCT_ID	0x38	RW	Yes	Yes

Page	Address	Register Name	Default	Type	Paged	NVM
0x82	0x75	Reserved	0x00	RW	Yes	Yes
0x82	0x76	Reserved	0x00	RW	Yes	Yes
0x82	0x77	Reserved	0x00	RW	Yes	Yes
0x82	0x78	Reserved	0x00	RW	Yes	Yes
0x82	0x79	Reserved	0x00	RW	Yes	Yes
0x82	0x7A	Reserved	0x00	RW	Yes	Yes
0x82	0x7B	Reserved	0x00	RW	Yes	Yes
0x82	0x7C	Reserved	0x00	RW	Yes	Yes
0x82	0x7D	Reserved	0x00	RW	Yes	Yes
0x82	0x7E	Reserved	0x00	RW	Yes	Yes
0x82	0x7F	CRC	N/A	R	Yes	No
Global	0x90	CBGA12	0x44	RW	No	No
Global	0x91	CBGA34	0x44	RW	No	No
Global	0x92	CBGA56	0x44	RW	No	No
Global	0x93	CBGA78	0x44	RW	No	No
Global	0x94	VFIXA_LB	0x83 (VID1) 0xA1 (VID2)	RW	No	No
Global	0x95	VFIXA_HB	0x00	RW	No	No
Global	0x96	VOFSA	0x00	RW	No	No
Global	0x97	TEMP_ALERTA & TEMP_VRHOTA	0x66	RW	No	No
Global	0x98	EN_PROTA	0x63	RW	No	No
Global	0x99	PROT_FLAGA	0x00	R	No	No
Global	0x9A	ILOAD_RPTA	N/A	R	No	No
Global	0x9B	PSYS_RPT	N/A	R	No	No
Global	0x9C	TEMP_RPTA	N/A	R	No	No
Global	0x9E	VOFS_LOADA	0x80	RW	No	No
Global	0x9F	ILOAD_RPT_RATIOA & FORCE_PS0A & KTONA	N/A	RW	No	No
Global	0xA0	EN_FVM	0x70	RW	No	No
Global	0xA3	EN_SPMA	0x00	RW	No	No
Global	0xA4	PRODUCT_ID	0x38	RO	No	No
Global	0xA7	EN_ANSA & SEL_SMALL_LLA	0x00	RW	No	No
Global	0xA8	VOFS_LOAD_OFSA	0x00	RW	No	No
Global	0xA9	LLA	0x0A	RW	No	No
Global	0xAA	EN_VFIX	0x00	RW	No	No
Global	0xAB	VFIXB_LB	0x83 (VID1) 0xA1 (VID2)	RW	No	No
Global	0xAC	VFIXB_HB	0x00	RW	No	No

Page	Address	Register Name	Default	Type	Paged	NVM
Global	0xAD	VOFSB	0x00	RW	No	No
Global	0xAE	TEMP_ALERTB & TEMP_VRHOTB	0x66	RW	No	No
Global	0xAF	EN_PROTB	0x63	RW	No	No
Global	0xB0	PROT_FLAGB	0x00	R	No	No
Global	0xB1	ILOAD_RPTB	N/A	R	No	No
Global	0xB2	TEMP_RPTB	N/A	R	No	No
Global	0xB4	VOFS_LOADB	0x80	RW	No	No
Global	0xB5	ILOAD_RPT_RATIOB & FORCE_PS0B & KTONB	N/A	RW	No	No
Global	0xB6	EN_SPMB & EN_ANSB & SMALL_LLB	N/A	RW	No	No
Global	0xB8	VOFS_LOAD_OFSB	0x00	RW	No	No
Global	0xB9	LLB	0x0A	RW	No	No
Global	0xBA	LLC	0x0A	RW	No	No
Global	0xBB	VFIXC_LB	0x83 (VID1) 0xA1 (VID2)	RW	No	No
Global	0xBC	VFIXC_HB	0x00	RW	No	No
Global	0xBD	VOFSC	0x00	RW	No	No
Global	0xBE	TEMP_ALERTC & TEMP_VRHOTC	0x66	RW	No	No
Global	0xBF	EN_PROTC	0x63	RW	No	No
Global	0xC0	PROT_FLAGC	00h	R	No	No
Global	0xC1	ILOAD_RPTC	N/A	R	No	No
Global	0xC2	TEMP_RPTC	N/A	R	No	No
Global	0xC4	VOFS_LOADC	0x80	RW	No	No
Global	0xC5	ILOAD_RPT_RATIOC & FORCE_PS0C & KTONC	N/A	RW	No	No
Global	0xC6	EN_SPMC & EN_ANSC & SMALL_LLC	N/A	RW	No	No
Global	0xC7	ILOAD_RPT_RATIOD	0x00	RW	No	No
Global	0xC8	VOFS_LOAD_OFSC	0x00	RW	No	No
Global	0xCC	SEL_ANS & WD_STAT & EN_WD & WDT	N/A	R/RW	No	No
Global	0xCD	ILOAD_RPTD	N/A	R	No	No
Global	0xEC	NVM_PROGRAM_STATUS	N/A	R	No	No
Global	0xEF	PAGE	0x80	RW	No	No
Global	0xF1	ENTER_CONFIG_MODE	N/A	W	No	No

Page	Address	Register Name	Default	Type	Paged	NVM
Global	0xFC	UNLOCK_NVM	N/A	W	No	No

Table 9. SET_ICCMAXA

Address: 0x10								
Bit	7	6	5	4	3	2	1	0
Field	SET_ICCMAXA							
Default	1	1	0	0	1	0	0	0
Type	RW							

Bit	Name	Description
7:0	SET_ICCMAXA	Set ICCMAX of rail A which can be set from 00h to FFh, representing 0A to 255A. For example, SET_ICCMAXA = 0x64, ICCMAXA = 100A SET_ICCMAXA = 0xFF, ICCMAXA = 255A

Table 10. SET_ICCMAX_RATIOA, EN_0LLA, EN_0LLB, EN_0LLC, EN_FASTV_VRHOT_ASSERTION, and SEL_FAST_SR

Address: 0x11								
Bit	7	6	5	4	3	2	1	0
Field	SET_ICCMAX_RATIOA	EN_0LLA	EN_0LLB	EN_0LLC	EN_FASTV_VRHOT_ASSERTION	Reserved	SEL_FAST_SR	
Default	1	0	0	0	1	1	0	0
Type	RW	RW	RW	RW	RW	RW	RW	

Bit	Name	Description
7	SET_ICCMAX_RATIOA	Extend the ICCMAX range of rail A. The effective ICCMAX can be encoded at 2 amps per bit by setting ICCMAX_ADDA 0: ICCMAX = SET_ICCMAXA, 1: ICCMAX = SET_ICCMAXA x 2 For example,SET_ICCMAX_RATIOA = 1 and SET_ICCMAXA = 0x64 ICCMAXA = 100 x 2 = 200A
6	EN_0LLA	Enable zero loadline of rail A 0: Disable, 1: Enable
5	EN_0LLB	Enable zero loadline of rail B 0: Disable, 1: Enable
4	EN_0LLC	Enable zero loadline of rail C 0: Disable, 1: Enable
3	EN_FASTV_VRHOT_ASSERTION	Enable $\overline{\text{VR\_HOT}}$ assertion during Fast V-Mode current limiting 0: Disable, 1: Enable
2	Reserved	Default value is 1
1:0	SEL_FAST_SR	Select DVID fast slew rate 00: 10mV/μs, 01: 24mV/μs, 10: 36mV/μs, 11: 48mV/μs

Table 11. SET_ICCMAXB

Address: 0x12								
Bit	7	6	5	4	3	2	1	0
Field	SET_ICCMAXB							
Default	0	0	1	1	1	1	0	1
Type	RW							

Bit	Name	Description
7:0	SET_ICCMAXB	Set ICCMAX of rail B which can be set from 00h to FFh representing 0A to 255A. For example, SET_ICCMAXB = 0x64, ICCMAXB = 100A SET_ICCMAXB = 0xFF, ICCMAXB = 255A

Table 12. SET_ICCMAXC

Address: 0x13								
Bit	7	6	5	4	3	2	1	0
Field	SET_ICCMAXC							
Default	0	0	1	0	0	1	1	1
Type	RW							

Bit	Name	Description
7:0	SET_ICCMAXC	Set ICCMAX of rail C which can be set from 00h to FFh representing 0A to 255A. For example, SET_ICCMAXC = 0x64, ICCMAXC = 100A SET_ICCMAXC = 0xFF, ICCMAXC = 255A

Table 13. SET_ICCMAXD

Address: 0x14								
Bit	7	6	5	4	3	2	1	0
Field	SET_ICCMAXD							
Default	0	0	1	0	0	0	0	1
Type	RW							

Bit	Name	Description
7:0	SET_ICCMAXD	Set ICCMAX of rail D which can be set from 00h to FFh representing 0A to 255A. For example, SET_ICCMAXD = 0x64, ICCMAXD = 100A SET_ICCMAXD = 0xFF, ICCMAXD = 255A

Table 14. SEL_VBOOT _CONFIGA, SEL_KTONA, SEL_VBOOT_CONFIGB, and SEL_KTONB

Address: 0x15								
Bit	7	6	5	4	3	2	1	0
Field	SEL_VBOOT _CONFIGA	SEL_KTONA			SEL_VBOOT_ CONFIGB	SEL_KTONB		
Default	0	0	1	1	0	1	0	0
Type	RW	RW			RW	RW		

Bit	Name	Description
7	SEL_VBOOT_CONFIGA	Select VBOOT configuration of rail A 0: VBOOTA = 1.05V when connecting the SD_GOOD pin to 5V VBOOTA = 0V when connecting the SD_GOOD pin to GND with a resistor 1: VBOOTA = 1.05V when connecting the SD_GOOD pin to 5V VBOOTA = SET_VBOOTA (non-zero VBOOT) when connecting the SD_GOOD pin to GND with a resistor
6:4	SEL_KTONA	Select SEL_KTONA for required switching frequency of rail A. Refer to the section Switching Frequency Setting for the details.
3	SEL_VBOOT_CONFIGB	Select VBOOT configuration of rail B 0: VBOOTB = 1.05V when connecting the SD_GOOD pin to 5V VBOOTB = 0V when connecting the SD_GOOD pin to GND with a resistor 1: VBOOTB = 1.05V when connecting the SD_GOOD pin to 5V VBOOTB = SET_VBOOTB (non-zero VBOOT) when connecting the SD_GOOD pin to GND with a resistor
2:0	SEL_KTONB	Select SEL_KTONB for required switching frequency of rail B. Refer to the section Switching Frequency Setting for the details.

Table 15. SEL_VBOOT _CONFIGC, SEL_KTONC, SEL_PWM_HIZ_VOL, SEL_CS_TYPEA, SEL_CS_TYPEB, and SEL_CS_TYPEC

Address: 0x16								
Bit	7	6	5	4	3	2	1	0
Field	SEL_VBOOT _CONFIGC	SEL_KTONC			SEL_PWM_ HIZ_VOL	SEL_CS_ TYPEA	SEL_CS _TYPEB	SEL_CS _TYPEC
Default	0	1	0	0	1	0	0	0
Type	RW	RW			RW	RW	RW	RW

Bit	Name	Description
7	SEL_VBOOT_CONFIGC	Select VBOOT configuration of rail C 0: VBOOTC = 1.05V when connecting the SD_GOOD pin to 5V VBOOTC = 0V when connecting the SD_GOOD pin to GND with a resistor 1: VBOOTC = 1.05V when connecting the SD_GOOD pin to 5V VBOOTC = SET_VBOOTC (Non-zero VBOOT) when connecting the SD_GOOD pin to GND with a resistor
6:4	SEL_KTONC	Select SEL_KTONC for required switching frequency of rail C. Refer to the section Switching Frequency Setting for the details.
3	SEL_PWM_HIZ_VOL	Select the tri-state voltage level of PWM 0: 1.6V to 2.2V, 1: 1.4V to 2.1V
2	SEL_CS_TYPEA	Select current sense type of rail A 0: DCR current sense is adopted, 1: SPS module is adopted.
1	SEL_CS_TYPEB	Select current sense type of rail B 0: DCR current sense is adopted, 1: SPS module is adopted.
0	SEL_CS_TYPEC	Select current sense type of rail C 0: DCR current sense is adopted, 1: SPS module is adopted.

Table 16. EN_FASTV_VRHOT_DEASSERTION, SEL_VID_TABLEA, SEL_VID_TABLEB, SEL_VID_TABLEC, and SEL_SMALL_LLA

Address: 0x17								
Bit	7	6	5	4	3	2	1	0
Field	EN_FASTV_VRHOT_DEASSERTION	SEL_VID_TABLEA	SEL_VID_TABLEB	SEL_VID_TABLEC	SEL_SMALL_LLA			
Default	1	0	0	0	0	0	0	0
Type	RW	RW	RW	RW	RW			

Bit	Name	Description
7	EN_FASTV_VRHOT_DEASSERTION	Enable revisiting the status of Fast V-Mode to de-assert VR_HOT while receiving the SetVID command 0: Disable, 1: Enable
6	SEL_VID_TABLEA	Select VID table of rail A 0: 5mV VID table, 1: 10mV VID table
5	SEL_VID_TABLEB	Select VID table of rail B 0: 5mV VID table, 1: 10mV VID table
4	SEL_VID_TABLEC	Select VID table of rail C 0: 5mV VID table, 1: 10mV VID table
3:0	SEL_SMALL_LLA	Select small loadline of rail A 0000: 100%, 0001: 95%, 0010: 90%, 0011: 85%, 0100: 80%, 0101: 75%, 0110: 70%, 0111: 65%, 1000: 60%, 1001: 55%, 1010: 50%, 1011: 40%, 1100: 30%, 1101: 20%, 1110: 10%, 1111: 0%

Table 17. SEL_SMALL_LLB and SEL_SMALL_LLC

Address: 0x18								
Bit	7	6	5	4	3	2	1	0
Field	SEL_SMALL_LLB				SEL_SMALL_LLC			
Default	0	0	0	0	0	0	0	0
Type	RW				RW			

Bit	Name	Description
7:4	SEL_SMALL_LLB	Select small loadline of rail B 0000: 100%, 0001: 95%, 0010: 90%, 0011: 85%, 0100: 80%, 0101: 75%, 0110: 70%, 0111: 65%, 1000: 60%, 1001: 55%, 1010: 50%, 1011: 40%, 1100: 30%, 1101: 20%, 1110: 10%, 1111: 0%
3:0	SEL_SMALL_LLC	Select small loadline of rail C 0000: 100%, 0001: 95%, 0010: 90%, 0011: 85%, 0100: 80%, 0101: 75%, 0110: 70%, 0111: 65%, 1000: 60%, 1001: 55%, 1010: 50%, 1011: 40%, 1100: 30%, 1101: 20%, 1110: 10%, 1111: 0%

Table 18. SEL_Ai_GAINA, SEL_Ai_GAINB, and SEL_Ai_GAINC

Address: 0x19								
Bit	7	6	5	4	3	2	1	0
Field	Reserved		SEL_Ai_GAINA		SEL_Ai_GAINB		SEL_Ai_GAINC	
Default	0	0	1	1	1	0	1	1
Type	RW		RW		RW		RW	

Bit	Name	Description
7:6	Reserved	Default value 0b00, not change
5:4	SEL_Ai_GAINA	Select Ai gain of rail A 00: 0.25, 01: 0.5, 10: 0.75, 11: 1
3:2	SEL_Ai_GAINB	Select Ai gain of rail B 00: 1, 01: 1.25, 10: 1.5, 11: 2
1:0	SEL_Ai_GAINC	Select Ai gain of rail C 00: 1, 01: 1.25, 10: 1.5, 11: 2

Table 19. SEL_MPH_AR_THA and SEL_MPH_AQR_THA

Address: 0x1A								
Bit	7	6	5	4	3	2	1	0
Field	SEL_MPH_AR_THA			SEL_MPH_AQR_THA				
Default	0	1	0	0	0	0	1	1
Type	RW			RW				

Bit	Name	Description
7:5	SEL_MPH_AR_THA	Select multi-phase adaptive ramp threshold of rail A SEL_MPH_AR_THA[7] = 0, 000: 275mV, 001: 225mV, 010: 175mV, 011: Disable SEL_MPH_AR_THA[7] = 1, 100: 300mV, 101: 250mV, 110: 200mV, 111: Disable
4:0	SEL_MPH_AQR_THA	Select multi-phase adaptive quick response threshold of rail A 00000: 240mV, 00001: 320mV, 00010: 400mV, 00011: 480mV, 00100: 560mV, 00101: 640mV, 00110: 720mV, 00111: 800mV, 01000: 880mV, 01001: 960mV, 01010: 1040mV, 01011: 1120mV, 01100: 1200mV, 01101: 1280mV, 01110: 1360mV, 01111: 1440mV, 10000: 1520mV, 10001: 1600mV, 10010: 1680mV, 10011: 1760mV, 10100: 1840mV, 10101: 1920mV, 10110: 2000mV, 10111: 2080mV, 11000: 2160mV, 11001: 2240mV, 11010: 2320mV, 11011: 2400mV, 11100: Disable, 11101: Disable, 11110: Disable, 11111: Disable

Table 20. SEL_ANS_BEHAV, SEL_1PH_AR_THA, and SEL_1PH_AQR_THA

Address: 0x1B								
Bit	7	6	5	4	3	2	1	0
Field	SEL_ANS_BEHAV	SEL_1PH_AR_THA		SEL_1PH_AQR_THA				
Default	0	0	1	0	0	0	1	1
Type	RW	RW		RW				

Bit	Name	Description
7	SEL_ANS_BEHAV	Acoustic noise suppression function behavior 0: Only DVID up is allowed, no action for DVID down 1: DVID down with extremely slow slew rate (0.00613mV/μs)
6:5	SEL_1PH_AR_THA	Select single-phase adaptive ramp threshold of rail A 00: 175mV, 01: 150mV, 10: 125mV, 11: Disable
4:0	SEL_1PH_AQR_THA	Select single-phase adaptive quick response threshold of rail A 00000: 40mV, 00001: 80mV, 00010: 120mV, 00011: 160mV, 00100: 200mV, 00101: 240mV, 00110: 280mV, 00111: 320mV, 01000: 360mV, 01001: 400mV, 01010: 440mV, 01011: 480mV, 01100: 520mV, 01101: 560mV, 01110: 600mV, 01111: 640mV, 10000: 680mV, 10001: 720mV, 10010: 760mV, 10011: 800mV, 10100: 840mV, 10101: 880mV, 10110: 920mV, 10111: 960mV, 11000: 1000mV, 11001: 1040mV, 11010: 1080mV, 11011: 1120mV, 11100: 1160mV, 11101: 1200mV, 11110: 1240mV, 11111: Disable

Table 21. SEL_1PH_AR_THB and SEL_1PH_AQR_THB

Address: 0x1C								
Bit	7	6	5	4	3	2	1	0
Field	SEL_1PH_AR_THB			SEL_1PH_AQR_THB				
Default	0	0	0	1	1	1	1	1
Type	RW			RW				

Bit	Name	Description
7:5	SEL_1PH_AR_THB	Select adaptive ramp threshold of rail B 000: Disable, 001: 125mV, 010: 150mV, 011: 175mV, 100: 200mV, 101: 225mV, 110: 250mV, 111: 275mV
4:0	SEL_1PH_AQR_THB	Select adaptive quick response threshold of rail B 00000: 240mV, 00001: 320mV, 00010: 400mV, 00011: 480mV, 00100: 560mV, 00101: 640mV, 00110: 720mV, 00111: 800mV, 01000: 880mV, 01001: 960mV, 01010: 1040mV, 01011: 1120mV, 01100: 1200mV, 01101: 1280mV, 01110: Disable, 01111: Disable, 10000: 720mV, 10001: 800mV, 10010: 880mV, 10011: 960mV, 10100: 1040mV, 10101: 1120mV, 10110: 1200mV, 10111: 1280mV, 11000: 1360mV, 11001: 1440mV, 11010: 1520mV, 11011: 1600mV, 11100: 1680mV, 11101: 1760mV, 11110: Disable, 11111: Disable

Table 22. SEL_1PH_AR_THC and SEL_1PH_AQR_THC

Address: 0x1D								
Bit	7	6	5	4	3	2	1	0
Field	SEL_1PH_AR_THC			SEL_1PH_AQR_THC				
Default	0	0	0	1	1	1	1	1
Type	RW			RW				

Bit	Name	Description
7:5	SEL_1PH_AR_THC	Select adaptive ramp threshold of rail C 000: Disable, 001: 125mV, 010: 150mV, 011: 175mV, 100: 200mV, 101: 225mV, 110: 250mV, 111: 275mV
4:0	SEL_1PH_AQR_THC	Select adaptive quick response threshold of rail C 00000: 240mV, 00001: 320mV, 00010: 400mV, 00011: 480mV, 00100: 560mV, 00101: 640mV, 00110: 720mV, 00111: 800mV, 01000: 880mV, 01001: 960mV, 01010: 1040mV, 01011: 1120mV, 01100: 1200mV, 01101: 1280mV, 01110: Disable, 01111: Disable, 10000: 720mV, 10001: 800mV, 10010: 880mV, 10011: 960mV, 10100: 1040mV, 10101: 1120mV, 10110: 1200mV, 10111: 1280mV, 11000: 1360mV, 11001: 1440mV, 11010: 1520mV, 11011: 1600mV, 11100: 1680mV, 11101: 1760mV, 11110: Disable, 11111: Disable

Table 23. SEL_ZCD_THA

Address: 0x1E								
Bit	7	6	5	4	3	2	1	0
Field	Reserved		SEL_ZCD_THA					
Default	0	0	1	0	0	1	0	0
Type	RW		RW					

Bit	Name	Description
7:6	Reserved	Unimplemented, default value is 0b00
5:0	SEL_ZCD_THA	Select the ZCD threshold of rail A. [5]: sign bit, 0 is positive [4:0]: 0.208mV/step For example, SEL_ZCD_THA = 0b011111, ZCD_THA = 6.4573mV SEL_ZCD_THA = 0b000000 or 0b100000, ZCD_THA = 0mV SEL_ZCD_THA = 0b111111, ZCD_THA = –6.4573mV

Table 24. EN_MT_TO_X1_RAMPA and SEL_ZCD_THB

Address: 0x1F								
Bit	7	6	5	4	3	2	1	0
Field	EN_MT_TO_X1_RAMPA	Reserved	SEL_ZCD_THB					
Default	0	0	0	1	1	1	0	1
Type	RW	RW	RW					

Bit	Name	Description
7	EN_MT_TO_X1_RAMPA	Enable ramp slop reduction to 1 times ramp slop of rail A. When power state transfer from PS0 to PS1 0: Disable, 1: Enable
6	Reserved	Default value 0, not change
5:0	SEL_ZCD_THB	Select the ZCD threshold of rail B. ZCD_THB = –2mV + [5:0] x 0.0625mV For example, SEL_ZCD_THB = 0b111111, ZCD_THB = 1.9375mV SEL_ZCD_THB = 0b100000, ZCD_THB = 0mV SEL_ZCD_THB = 0b000000, ZCD_THB = –2mV

Table 25. EN_EX_1UA_LPF_INITA and SEL_ZCD_THC

Address: 0x20								
Bit	7	6	5	4	3	2	1	0
Field	Reserved	EN_EX_1UA_LPF_INITA	SEL_ZCD_THC					
Default	0	0	0	1	1	1	0	1
Type	RW	RW	RW					

Bit	Name	Description
7	Reserved	Unimplemented, default value is 0
6	EN_EX_1UA_LPF_INITA	Enable extra +1μA on initial current of LPF of rail A 0: Disable, 1: Enable For example, EN_EX_1UA_LPF_INITA = 1, SEL_LPF_INITA = 00: −0.5μA, 01: 0μA, 10: +0.5μA, 11: +1μA
5:0	SEL_ZCD_THC	Select the ZCD threshold of rail C. ZCD_THC = −4mV + [5:0] x 0.125mV For example, SEL_ZCD_THC = 0b111111, ZCD_THC = 3.875mV SEL_ZCD_THC = 0b100000, ZCD_THC = 0mV SEL_ZCD_THC = 0b000000, ZCD_THC = −4mV

Table 26. SET_SS_OCPA

Address: 0x21								
Bit	7	6	5	4	3	2	1	0
Field	SET_SS_OCPA							
Default	1	1	0	0	1	0	0	0
Type	RW							

Bit	Name	Description
7:0	SET_SS_OCPA	Set soft-start OCP of rail A which can be set from 00h to FFh representing 0A to 1020A. Resolution = 4A/LSB. The maximum ratio value SET_SS_OCPA/ICCMAXA is limited at 6.5. For example, SET_SS_OCPA = 0x64, SS_OCPA = 400A SET_SS_OCPA = 0xFF, SS_OCPA = 1020A

Table 27. SEL_LPF_INITA and SET_SS_OCPB

Address: 0x22								
Bit	7	6	5	4	3	2	1	0
Field	SEL_LPF_INITA		SET_SS_OCPB					
Default	0	0	0	1	1	0	0	1
Type	RW		RW					

Bit	Name	Description
7:6	SEL_LPF_INITA	Set initial current of LPF of rail A 00: –1.5μA, 01: –1μA, 10: –0.5μA, 11: 0μA
5:0	SET_SS_OCPB	Set soft-start OCP of rail B which can be set from 00h to 3Fh representing 0A to 252A. Resolution = 4A/LSB. The maximum ratio value SET_SS_OCPB/ICCMAXB is limited at 6.5. For example, SET_SS_OCPB = 0x14, SS_OCPB = 80A SET_SS_OCPB = 0x3F, SS_OCPB = 252A

Table 28. EN_SPM_DEFAULTB, EN_SPM_DEFAULTC, and SET_SS_OCPC

Address: 0x23								
Bit	7	6	5	4	3	2	1	0
Field	EN_SPM_DEFAULTB	EN_SPM_DEFAULTC	SET_SS_OCPC					
Default	0	0	0	1	1	0	0	1
Type	RW	RW	RW					

Bit	Name	Description
7	EN_SPM_DEFAULTB	Default enable SPM of rail B 0: Disable, 1: Enable
6	EN_SPM_DEFAULTC	Default enable SPM of rail C 0: Disable, 1: Enable
5:0	SET_SS_OCPC	Set the soft-start OCP of rail C which can be set from 00h to 3Fh representing 0A to 252A. Resolution = 4A/LSB. The maximum ratio value SET_SS_OCPC/ICCMAXC is limited at 6.5. For example, SET_SS_OCPC = 0x14, SS_OCPC = 80A SET_SS_OCPC = 0x3F, SS_OCPC = 252A

Table 29. EN_FAST_EX_TOFFBC, SEL_FASTV_TOFFB, and SEL_FASTV_DLYB

Address: 0x24								
Bit	7	6	5	4	3	2	1	0
Field	SEL_FASTV_CLAMPA			EN_FASTV_EX_TOFFBC	SEL_FASTV_TOFFB		SEL_FASTV_DLYB	
Default	0	0	0	1	1	0	1	0
Type	RW			RW	RW		RW	

Bit	Name	Description
7:5	SEL_FASTV_CLAMPA	Select the clamp voltage when Fast V-Mode is triggered of rail A 000: 2.62V, 001: 2.58V, 010: 2.54V, 011: 2.5V, 100: 2.54V, 101: 2.5V, 110: 2.46V, 111: 2.38V
4	EN_FASTV_EX_TOFFBC	Enable extend toff during Fast V-Mode of rail B and rail C 0: Disable, 1: Enable
3:2	SEL_FASTV_TOFFB	Select extend toff during Fast V-Mode of rail B 00: 130ns, 01: 160ns, 10: 200ns, 11: 240ns
1:0	SEL_FASTV_DLYB	Select the clamp delay when Fast V-Mode is triggered of rail B 00: 1μs, 01: 2μs, 10: 4μs, 11: 5μs

Table 30. EN_2X_RIPPLE_COMPA, SEL_RIPPLE_COMPA, SEL_FASTV_TOFFC, and SEL_FASTV_DLYC

Address: 0x25								
Bit	7	6	5	4	3	2	1	0
Field	EN_2X_RIPPLE_COMPA	SEL_RIPPLE_COMPA			SEL_FASTV_TOFFC		SEL_FASTV_DLYC	
Default	0	0	0	0	1	0	1	0
Type	RW	RW			RW		RW	

Bit	Name	Description
7	EN_2X_RIPPLE_COMPA	Enable/Disable ripple compensation current x2 of Rail A corresponding to the register of SET_RIPPLE_COMPA 0: Disable 1: Enable
6:4	SEL_RIPPLE_COMPA	Adding auxiliary compensation current to VEA for compensating frequency difference when VID = 0.3V ~ 0.9V of Rail A, which helps the output voltage to reach the target within the specified time during DVID transition. Icomp = VID/0.886MΩ x SEL_RIPPLE_COMPA As EN_2X_RIPPLE_COMPA = 0, 000: x0 001: x1 010: x2 011: x3 100: x4 101: x5 110: x6 111: x7 As EN_2X_RIPPLE_COMPA = 1, 000: x0 001: x2 010: x4 011: x6 100: x8 101: x10 110: x12 111: x14
3:2	SEL_FASTV_TOFFC	Select extend toff during Fast V-Mode of rail C 00: 130ns, 01: 160ns, 10: 200ns, 11: 240ns
1:0	SEL_FASTV_DLYC	Select the clamp delay when Fast V-Mode is triggered of rail C 00: 1μs, 01: 2μs, 10: 4μs, 11: 5μs

Table 31. SEL_I_DVID_LIFTA and SEL_I_DVID_LIFTB

Address: 0x26								
Bit	7	6	5	4	3	2	1	0
Field	SEL_I_DVID_LIFTA				SEL_I_DVID_LIFTB			
Default	0	1	0	1	0	1	0	0
Type	RW				RW			

Bit	Name	Description
7:4	SEL_I_DVID_LIFTA	Select the compensation current I_{DVID_LIFT} during DVID up period of rail A 0000: 0μA, 0001: 2μA, 0010: 4μA, 0011: 6μA, 0100: 8μA, 0101: 10μA, 0110: 12μA, 0111: 14μA, 1000: 16μA, 1001: 18μA, 1010: 20μA, 1011: 24μA, 1100: 28μA, 1101: 32μA, 1110: 36μA, 1111: 40μA
3:0	SEL_I_DVID_LIFTB	Select the compensation current I_{DVID_LIFT} during DVID up period of rail B 0000: 0μA, 0001: 2μA, 0010: 4μA, 0011: 6μA, 0100: 8μA, 0101: 10μA, 0110: 12μA, 0111: 14μA, 1000: 16μA, 1001: 18μA, 1010: 20μA, 1011: 24μA, 1100: 28μA, 1101: 32μA, 1110: 36μA, 1111: 40μA

Table 32. SEL_I_DVID_LIFTC & EN_SPM_DEFAULTA & SEL_UV_THA & EN_UVA

Address: 0x27								
Bit	7	6	5	4	3	2	1	0
Field	SEL_I_DVID_LIFTC				EN_SPM_DEFAULTA	SEL_UV_THA	EN_UVA	Reserved
Default	0	1	0	1	0	0	1	1
Type	RW				RW	RW	RW	RW

Bit	Name	Description
7:4	SEL_I_DVID_LIFTC	Select the compensation current I_{DVID_LIFT} during DVID up period of rail C 0000: 0μA, 0001: 2μA, 0010: 4μA, 0011: 6μA, 0100: 8μA, 0101: 10μA, 0110: 12μA, 0111: 14μA, 1000: 16μA, 1001: 18μA, 1010: 20μA, 1011: 24μA, 1100: 28μA, 1101: 32μA, 1110: 36μA, 1111: 40μA
3	EN_SPM_DEFAULTA	Default enable SPM of rail A 0: Disable, 1: Enable
2	SEL_UV_THA	Select UV threshold of rail A 0: 650mV, 1: 850mV
1	EN_UVA	Enable UV protection of rail A 0: Disable, 1: Enable
0	Reserved	Default value 1, not change

Table 33. SEL_DELTA_OVPA, SEL_DELTA_OVPB, and SEL_DELTA_OVPC

Address: 0x28								
Bit	7	6	5	4	3	2	1	0
Field	SEL_DELTA_OVPA		SEL_DELTA_OVPB		SEL_DELTA_OVPC		Reserved	
Default	0	0	0	0	0	0	0	0
Type	RW		RW		RW		RW	

Bit	Name	Description
7:6	SEL_DELTA_OVPA	Select delta OVP threshold of rail A 00: 350mV, 01: 400mV, 10: 450mV, 11: 500mV
5:4	SEL_DELTA_OVPB	Select delta OVP threshold of rail B 00: 350mV, 01: 400mV, 10: 450mV, 11: 500mV
3:2	SEL_DELTA_OVPC	Select delta OVP threshold of rail C 00: 350mV, 01: 400mV, 10: 450mV, 11: 500mV
1:0	Reserved	Unimplemented, default value is 0b00

Table 34. Reserved

Address: 0x29								
Bit	7	6	5	4	3	2	1	0
Field	Reserved							
Default	1	0	0	0	0	0	0	0
Type	RW							

Bit	Name	Description
7:0	Reserved	Default value 80h, not change

Table 35. SEL_PSYS_LEVEL, SEL_DRVEN_F, EN_DRVEN_TO_DRVEN_F & EN_RT_SPS, and SEL_FASTV_DLYA

Address: 0x2A								
Bit	7	6	5	4	3	2	1	0
Field	SEL_PSYS_LEVEL	SEL_DRVEN_F	EN_DRVEN_TO_DRVEN_F	EN_RT_SPS	Reserved	SEL_FASTV_DLYA		
Default	0	1	0	0	0	1	0	1
Type	RW	RW	RW	RW	RW	RW		

Bit	Name	Description
7	SEL_PSYS_LEVEL	Select the full scale of PSYS 0: 1.6V, 1: 3.2V
6	SEL_DRVEN_F	Select DRVEN_F behavior for applicated rail 0: For rail A and rail B 1: For all rail
5	EN_DRVEN_TO_DRVEN_F	Enable DRVEN behavior as DRVEN_F behavior for all rail 0: Disable, 1: Enable
4	EN_RT_SPS	Enable DRVEN_F behavior as: This pin will be in low state when VID = 0V 0: Disable, 1: Enable
3	Reserved	Default value 0, not change
2:0	SEL_FASTV_DLYA	Select the clamp delay when Fast V-Mode is triggered of rail A 000: 0.125μs, 001: 0.25μs, 010: 0.375μs, 011: 0.5μs, 100: 1μs, 101: 2μs, 110: 3μs, 111: 4μs

Table 36. SEL_SUM_OCP_DEB_TIMEA, SEL_SUM_OCP_DEB_TIMEB, and SET_SUM_OCPB

Address: 0x2B								
Bit	7	6	5	4	3	2	1	0
Field	SEL_SUM_OCP_DEB_TIMEA	SEL_SUM_OCP_DEB_TIMEB	SET_SUM_OCPB					
Default	1	1	0	1	0	1	0	0
Type	RW	RW	RW					

Bit	Name	Description
7	SEL_SUM_OCP_DEB_TIMEA	Select the debounce time of sum OCP of rail A 0: 20μs, 1: 40μs
6	SEL_SUM_OCP_DEB_TIMEB	Select the debounce time of sum OCP of rail B 0: 20μs, 1: 40μs
5:0	SET_SUM_OCPB	Set sum OCP of rail B which can be set from 00h to 3Fh representing 0A to 252A. Resolution = 4A/LSB. The maximum ratio value SET_SUM_OCPB /ICCMAXB is limited at 6.5. For example, SET_SUM_OCPB = 0x14, SUM_OCPB = 80A SET_SUM_OCPB = 0x3F, SUM_OCPB = 252A

Table 37. SEL_SUM_OCP_DEB_TIMEC & SET_SUM_OCPC

Address: 0x2C								
Bit	7	6	5	4	3	2	1	0
Field	SEL_SUM_OCP_DEB_TIMEC	Reserved	SET_SUM_OCPC					
Default	1	1	0	0	1	1	0	0
Type	RW	RW	RW					

Bit	Name	Description
7	SEL_SUM_OCP_DEB_TIMEC	Select the debounce time of sum OCP of rail C 0: 20μs, 1: 40μs
6	Reserved	Default value 1, not change
5:0	SET_SUM_OCPC	Set sum OCP of rail C which can be set from 00h to 3Fh representing 0A to 252A. Resolution = 4A/LSB. The maximum ratio value SET_SUM_OCPC /ICCMAXC is limited at 6.5. For example, SET_SUM_OCPC = 0x14, SUM_OCPC = 80A SET_SUM_OCPC = 0x3F, SUM_OCPC = 252A

Table 38. EN_2X_KTON, EN_AR_LIFT_VIDB, SEL_SS_OVPA, SEL_SS_OVPB, and SEL_SS_OVPC

Address: 0x2D								
Bit	7	6	5	4	3	2	1	0
Field	EN_2X_KTON	EN_AR_LIFT_VIDB	SEL_SS_OVPA		SEL_SS_OVPB		SEL_SS_OVPC	
Default	0	1	0	0	0	0	0	0
Type	RW	RW	RW		RW		RW	

Bit	Name	Description
7	EN_2X_KTON	Enable 2X K_{TON} 0: Disable, 1: Enable
6	EN_AR_LIFT_VIDB	Enable lifting VID in adaptive ramp of rail B 0: Disable, 1: Enable
5:4	SEL_SS_OVPA	Select soft-start OVP threshold of rail A 00: 2.1V, 01: 2.3V, 10: 2.5V, 11: 2.7V
3:2	SEL_SS_OVPB	Select soft-start OVP threshold of rail B 00: 2.1V, 01: 2.3V, 10: 2.5V, 11: 2.7V
1:0	SEL_SS_OVPC	Select soft-start OVP threshold of rail C 00: 2.1V, 01: 2.3V, 10: 2.5V, 11: 2.7V

Table 39. SEL_ANTI_OVS_THA and SEL_ANTI_OVS_THB

Address: 0x2E								
Bit	7	6	5	4	3	2	1	0
Field	Reserved		SEL_ANTI_OVS_THA			SEL_ANTI_OVS_THB		
Default	1	0	1	1	1	1	1	1
Type	RW		RW			RW		

Bit	Name	Description
7:6	Reserved	Default value 0b10, not change
5:3	SEL_ANTI_OVS_THA	Select anti-overshoot threshold of rail A 000: 180mV, 001: 240mV, 010: 300mV, 011: 360mV, 100: 420mV, 101: 480mV, 110: Disable, 111: Disable
2:0	SEL_ANTI_OVS_THB	Select anti-overshoot threshold of rail B 000: 90mV, 001: 120mV, 010: 150mV, 011: 180mV, 100: 210mV, 101: 240mV, 110: Disable, 111: Disable

Table 40. EN_AR_LIFT_VIDC, SEL_ANTI_OVS_THC, EN_QR_LIFT_VIDB, EN_SS_OCPA, EN_SS_OCPB, and EN_SS_OCPC

Address: 0x2F								
Bit	7	6	5	4	3	2	1	0
Field	EN_AR_LIFT_VIDC	SEL_ANTI_OVS_THC			EN_QR_LIFT_VIDB	EN_SS_OCPA	EN_SS_OCPB	EN_SS_OCPC
Default	1	1	1	1	0	1	1	1
Type	RW	RW			RW	RW	RW	RW

Bit	Name	Description
7	EN_AR_LIFT_VIDC	Enable lifting VID in adaptive ramp of rail C 0: Disable, 1: Enable
6:4	SEL_ANTI_OVS_THC	Select anti-overshoot threshold of rail C 000: 90mV, 001: 120mV, 010: 150mV, 011: 180mV, 100: 210mV, 101: 240mV, 110: Disable, 111: Disable
3	EN_QR_LIFT_VIDB	Enable lifting VID in quick response of rail B 0: Disable, 1: Enable
2	EN_SS_OCPA	Enable soft-start OCP of rail A 0: Disable, 1: Enable
1	EN_SS_OCPB	Enable soft-start OCP of rail B 0: Disable, 1: Enable
0	EN_SS_OCPC	Enable soft-start OCP of rail C 0: Disable, 1: Enable

Table 41. EN_EX_10MV_LIFT_VIDA, SEL_1PH_QR_MODEA, SEL_1PH_QR_WIDTHA, SEL_LIFT_VIDA, SEL_MPH_QR_MODEA, and SEL_MPH_QR_WIDTHA

Address: 0x30								
Bit	7	6	5	4	3	2	1	0
Field	EN_EX_10MV_LIFT_VIDA	SEL_1PH_QR_MODEA	SEL_1PH_QR_WIDTHA		SEL_LIFT_VIDA	SEL_MPH_QR_MODEA	SEL_MPH_QR_WIDTHA	
Default	0	0	0	0	1	1	1	0
Type	RW	RW	RW		RW	RW	RW	

Bit	Name	Description
7	EN_EX_10MV_LIFT_VIDA	Enable extra 10mV lifting VID amount for SEL_LIFT_VIDA 0: Disable, 1: Enable
6	SEL_1PH_QR_MODEA	Select single-phase quick response mode of rail A 0: Fixed PWM width in quick response mode 1: Adaptive PWM width in quick response mode
5:4	SEL_1PH_QR_WIDTHA	Select PWM width in single-phase quick response mode of rail A 00: 0.5 x t_{ON}, 01: 0.75 x t_{ON}, 10: 1.0 x t_{ON}, 11: 1.25 x t_{ON}
3	SEL_LIFT_VIDA	Select lifting VID amount of rail A 0: 5mV, 1: 10mV EN_EX_10mV_LIFT_VIDA = 1, 0: 15mV, 1: 20mV
2	SEL_MPH_QR_MODEA	Select multi-phase quick response mode of rail A 0: Fixed PWM width in quick response mode 1: Adaptive PWM width in quick response mode
1:0	SEL_MPH_QR_WIDTHA	Select PWM width in multi-phase quick response mode of rail A 00: 0.5 x t_{ON}, 01: 0.75 x t_{ON}, 10: 1.0 x t_{ON}, 11: 1.25 x t_{ON}

Table 42. EN_EX_TONA, SEL_EX_TON_WIDTHA, and SEL_EX_TON_THA

Address: 0x31								
Bit	7	6	5	4	3	2	1	0
Field	EN_EX_TONA	Reserved			SEL_EX_TON_WIDTHA		SEL_EX_TON_THA	
Default	1	1	1	0	0	1	1	1
Type	RW	RW			RW		RW	

Bit	Name	Description
7	EN_EX_TONA	Enable the extend t_{ON} of rail A 0: Disable, 1: Enable
6:4	Reserved	Default value is 0b110. All other combinations are not defined.
3:2	SEL_EX_TON_WIDTHA	Select extend t_{ON} width of rail A 00: 4 x t_{ON}, 01: 2.66 x t_{ON}, 10: 2 x t_{ON}, 11: 1.6 x t_{ON}
1:0	SEL_EX_TON_THA	Select extend t_{ON} threshold of rail A 00: 2.4V + 150mV, 01: 2.4V + 200mV, 10: 2.4V + 250mV, 11: 2.4V + 300mV

Table 43. EN_MPH_QR_LIFT_VIDA, EN_1PH_QR_LIFT_VIDA, EN_MPH_AR_LIFT_VIDA, EN_1PH_AR_LIFT_VIDA, SEL_QR_LIFT_VID_RECOVERY_TIMEA, SEL_AR_LIFT_VID_RECOVERY_TIMEA, SEL_QR_LIFT_VIDA, and SEL_AR_LIFT_VIDA

Address: 0x32								
Bit	7	6	5	4	3	2	1	0
Field	EN_MPH_QR_LIFT_VIDA	EN_1PH_QR_LIFT_VIDA	EN_MPH_AR_LIFT_VIDA	EN_1PH_AR_LIFT_VIDA	SEL_QR_LIFT_VID_RECOVERY_TIMEA	SEL_AR_LIFT_VID_RECOVERY_TIMEA	SEL_QR_LIFT_VIDA	SEL_AR_LIFT_VIDA
Default	0	0	0	1	1	0	1	1
Type	RW	RW	RW	RW	RW	RW	RW	RW

Bit	Name	Description
7	EN_MPH_QR_LIFT_VIDA	Enable lifting VID in multi-phase quick response mode of rail A 0: Disable, 1: Enable
6	EN_1PH_QR_LIFT_VIDA	Enable lifting VID in single-phase quick response mode of rail A 0: Disable, 1: Enable
5	EN_MPH_AR_LIFT_VIDA	Enable lifting VID in multi-phase adaptive ramp mode of rail A 0: Disable, 1: Enable
4	EN_1PH_AR_LIFT_VIDA	Enable lifting VID in single-phase adaptive ramp mode of rail A 0: Disable, 1: Enable
3	SEL_QR_LIFT_VID_RECOVERY_TIMEA	Select lifting VID recovery time in quick response mode of rail A 0: 150μs, 1: 40μs
2	SEL_AR_LIFT_VID_RECOVERY_TIMEA	Select lifting VID recovery time in adaptive ramp mode of rail A 0: 150μs, 1: 40μs
1	SEL_QR_LIFT_VIDA	Select lift VID amount in quick response mode of rail A 0: 5mV, 1: 10mV
0	SEL_AR_LIFT_VIDA	Select lift VID amount in adaptive ramp mode of rail A 0: 5mV, 1: 10mV

Table 44. EN_MPH_QR_LIFT_LPFA, EN_1PH_QR_LIFT_LPFA, EN_MPH_AR_LIFT_LPFA, EN_1PH_AR_LIFT_LPFA, EN_MPH_LIFT, EN_MPH_LIFT_LPFA, and EN_1PH_LIFT_LPFA

Address: 0x33								
Bit	7	6	5	4	3	2	1	0
Field	EN_MPH_QR_LIFT_LPFA	EN_1PH_QR_LIFT_LPFA	EN_MPH_AR_LIFT_LPFA	EN_1PH_AR_LIFT_LPFA	Reserved	EN_MPH_LIFT_LPFA	Reserved	EN_1PH_LIFT_LPFA
Default	1	0	0	1	0	0	0	1
Type	RW	RW	RW	RW	RW	RW	RW	RW

Bit	Name	Description
7	EN_MPH_QR_LIFT_LPFA	Enable lifting LPF in quick response mode with multi-phase operation of rail A. To enable this function, EN_MPH_LIFT_LPFA must be enabled also. 0: Disable, 1: Enable
6	EN_1PH_QR_LIFT_LPFA	Enable lifting LPF in quick response mode with single-phase operation of rail A. To enable this function, EN_1PH_LIFT_LPFA must be enabled also. 0: Disable, 1: Enable
5	EN_MPH_AR_LIFT_LPFA	Enable lifting LPF in adaptive ramp mode with multi-phase operation of rail A. To enable this function, EN_MPH_LIFT_LPFA must be enabled also. 0: Disable, 1: Enable
4	EN_1PH_AR_LIFT_LPFA	Enable lifting LPF in adaptive ramp mode with single-phase operation of rail A. To enable this function, EN_1PH_LIFT_LPFA must be enabled also. 0: Disable, 1: Enable
3	Reserved	Unimplemented, default value is 0
2	EN_MPH_LIFT_LPFA	Enable lifting LPF in quick response or adaptive ramp mode with multi-phase operation of rail A 0: Disable, 1: Enable
1	Reserved	Unimplemented, default value is 0
0	EN_1PH_LIFT_LPFA	Enable lifting LPF in quick response or adaptive ramp mode with single-phase operation of rail A 0: Disable, 1: Enable

Table 45. EN_HF_ACLL_QRA, SEL_HF_ACLL_QR_FREQA, EN_HF_ACLL_SQRA, and SEL_HF_ACLL_SQR_FREQA

Address: 0x34								
Bit	7	6	5	4	3	2	1	0
Field	EN_HF_ACLL_QRA	SEL_HF_ACLL_QR_FREQA			EN_HF_ACLL_SQRA	SEL_HF_ACLL_SQR_FREQA		
Default	1	1	0	0	1	0	1	0
Type	RW	RW			RW	RW		

Bit	Name	Description
7	EN_HF_ACLL_QRA	Enable quick response at ACLL frequency is larger than SEL_HF_ACLL_QR_FREQ of rail A 0: Enable 1: Disable
6:4	SEL_HF_ACLL_QR_FREQA	Select the ACLL frequency threshold that will disable quick response of rail A 000: 402kHz, 001: 443kHz, 010: 483kHz, 011: 523kHz, 100: 564kHz, 101: 604kHz, 110: 644kHz, 111: 684kHz
3	EN_HF_ACLL_SQRA	Shrink quick response of rail A when ACLL frequency is larger than SEL_HF_ACLL_SQR_FREQA 0: Disable, 1: Enable
2:0	SEL_HF_ACLL_SQR_FREQA	Select ACLL frequency that will shrink quick response of rail A 000: 161kHz, 001: 201kHz, 010: 241kHz, 011: 282kHz, 100: 322kHz, 101: 362kHz, 110: 402kHz, 111: 443kHz

Table 46. EN_EX_25MV_FLT_RAMPB and SEL_HF_ACLL_QR_FREQB

Address: 0x35								
Bit	7	6	5	4	3	2	1	0
Field	EN_EX_25MV_FLT_RAMPB	SEL_HF_ACLL_QR_FREQB			Reserved			
Default	0	1	1	1	1	0	0	1
Type	RW	RW			RW			

Bit	Name	Description
7	EN_EX_25MV_FLT_RAMPB	Enable extra 25mV on floating ramp of rail B 0: Disable, 1: Enable
6:4	SEL_HF_ACLL_QR_FREQB	Select the ACLL frequency threshold that will disable quick response of rail B 000: Disable, 001: 475kHz, 010: 517kHz, 011: 559kHz, 100: 601kHz, 101: 642kHz, 110: 682kHz, 111: 724kHz
3:0	Reserved	Default value 0b1001, not change

Table 47. SEL_QR_WIDTHB and SEL_FLT_RAMPB

Address: 0x36								
Bit	7	6	5	4	3	2	1	0
Field	Reserved				SEL_QR_WIDTHB		SEL_FLT_RAMPB	
Default	1	1	0	0	0	1	1	1
Type	RW				RW		RW	

Bit	Name	Description
7:4	Reserved	Default value 0b1100, not change
3:2	SEL_QR_WIDTHB	Select PWM width in quick response mode of rail B 00: 0.475 x t_{ON}, 01: 0.533 x t_{ON}, 10: 0.615 x t_{ON}, 11: 0.726 x t_{ON}
1:0	SEL_FLT_RAMPB	Select floating ramp threshold of rail B EN_EX_25MV_FLT_RAMPB = 0, 00: 125mV, 01: 175mV, 10: 225mV, 11: Disable EN_EX_25MV_FLT_RAMPB = 1, 00: 150mV, 01: 200mV, 10: 250mV, 11: Disable

Table 48. EN_QR_LIFT_VIDC, EN_EX_TONB, SEL_EX_TON_WIDTHB, and SEL_EX_TON_THB

Address: 0x37								
Bit	7	6	5	4	3	2	1	0
Field	Reserved		EN_QR_LIFT_VIDC	EN_EX_TONB	SEL_EX_TON_WIDTHB		SEL_EX_TON_THB	
Default	0	0	0	0	0	0	0	1
Type	RW		RW	RW	RW		RW	

Bit	Name	Description
7:6	Reserved	Unimplemented, default value is 0b00
5	EN_QR_LIFT_VIDC	Enable lifting VID in quick response of rail C 0: Enable, 1: Disable
4	EN_EX_TONB	Enable the extend t_{ON} of rail B 0: Disable, 1: Enable
3:2	SEL_EX_TON_WIDTHB	Select extend t_{ON} width of rail B 00: 4 x t_{ON}, 01: 2.66 x t_{ON}, 10: 2 x t_{ON}, 11: 1.6 x t_{ON}
1:0	SEL_EX_TON_THB	Select extend t_{ON} threshold of rail B 00: 2.4V + 150mV, 01: 2.4V + 200mV, 10: 2.4V + 250mV, 11: 2.4V + 300mV

Table 49. EN_EX_25MV_FLT_RAMPC and SEL_HF_ACLL_QR_FREQC

Address: 0x38								
Bit	7	6	5	4	3	2	1	0
Field	EN_EX_25MV_FLT_RAMPC	SEL_HF_ACLL_QR_FREQC			Reserved			
Default	0	1	1	1	1	0	0	1
Type	RW	RW			RW			

Bit	Name	Description
7	EN_EX_25MV_FLT_RAMPC	Enable extra 25mV on floating ramp of rail C 0: Disable, 1: Enable
6:4	SEL_HF_ACLL_QR_FREQC	Select the ACLL frequency threshold that will disable quick response of rail C 000: Disable, 001: 475kHz, 010: 517kHz, 011: 559kHz, 100: 601kHz, 101: 642kHz, 110: 682kHz, 111: 724kHz
3:0	Reserved	Default value 0b1001, not change

Table 50. SEL_QR_WIDTHC and SEL_FLT_RAMPC

Address: 0x39								
Bit	7	6	5	4	3	2	1	0
Field	Reserved				SEL_QR_WIDTHC		SEL_FLT_RAMPC	
Default	1	1	0	0	0	1	1	1
Type	RW				RW		RW	

Bit	Name	Description
7:4	Reserved	Default value 0b1100, not change
3:2	SEL_QR_WIDTHC	Select PWM width in quick response mode of rail C 00: 0.475 x t_{ON}, 01: 0.533 x t_{ON}, 10: 0.615 x t_{ON}, 11: 0.726 x t_{ON}
1:0	SEL_FLT_RAMPC	Select floating ramp threshold of rail C EN_EX_25MV_FLT_RAMPC = 0 00: 125mV, 01: 175mV, 10: 225mV, 11: Disable EN_EX_25MV_FLT_RAMPC = 1 00: 150mV, 01: 200mV, 10: 250mV, 11: Disable

Table 51. EN_EX_TONC, SEL_EX_TON_WIDTHC, and SEL_EX_TON_THC

Address: 0x3A								
Bit	7	6	5	4	3	2	1	0
Field	Reserved			EN_EX_TONC	SEL_EX_TON_WIDTHC		SEL_EX_TON_THC	
Default	0	0	0	0	0	0	0	1
Type	RW			RW	RW		RW	

Bit	Name	Description
7:5	Reserved	Unimplemented, the default value is 0b000
4	EN_EX_TONC	Enable the extend t_{ON} of rail C 0: Disable, 1: Enable
3:2	SEL_EX_TON_WIDTHC	Select extend t_{ON} width of rail C 00: 4 x t_{ON}, 01: 2.66 x t_{ON}, 10: 2 x t_{ON}, 11: 1.6 x t_{ON}
1:0	SEL_EX_TON_THC	Select extend t_{ON} threshold of rail C 00: 2.4V + 150mV, 01: 2.4V + 200mV, 10: 2.4V + 250mV, 11: 2.4V + 300mV

Table 52. SEL_PH_TYPEA, SEL_PH_TYPEB, and SEL_PH_TYPEC

Address: 0x3B								
Bit	7	6	5	4	3	2	1	0
Field	Reserved		SEL_PH_TYPEA		SEL_PH_TYPEB		SEL_PH_TYPEC	
Default	0	0	0	0	0	0	0	0
Type	RW		RW		RW		RW	

Bit	Name	Description
7:6	Reserved	Default value 0b00, not change
5:4	SEL_PH_TYPEA	Select the phase type of rail A 00: Normal 01: One PWM to two phases with phase doubler 10: One PWM to two phases without phase doubler 11: Extend to nine phases with phase doubler
3:2	SEL_PH_TYPEB	Select the phase type of rail B 00: Normal 01: Unimplemented 10: One PWM to two phases without phase doubler 11: Unimplemented
1:0	SEL_PH_TYPEC	Select the phase type of rail C 00: Normal 01: Unimplemented 10: One PWM to two phases without phase doubler 11: Unimplemented

Table 53. SET_SUM_OCPA

Address: 0x3C								
Bit	7	6	5	4	3	2	1	0
Field	SET_SUM_OCPA							
Default	1	0	0	0	0	0	1	0
Type	RW							

Bit	Name	Description
7:0	SET_SUM_OCPA	Set sum OCP of rail A which can be set from 00h to FFh representing 0A to 1020A. Resolution = 4A/LSB. The maximum ratio value SET_SUM_OCPBA /ICCMAXA is limited at 6.5. For example, SET_SUM_OCPA = 0x64, SUM_OCPA = 400A SET_SUM_OCPA = 0xFF, SUM_OCPA = 1020A

Table 54. SET_IMON_RPT_OFSA

Address: 0x3D								
Bit	7	6	5	4	3	2	1	0
Field	Reserved		SET_IMON_RPT_OFSA					
Default	1	0	0	0	0	0	0	0
Type	RW		RW					

Bit	Name	Description
7:6	Reserved	Default value 0b10, not change
5:0	SET_IMON_RPT_OFSA	Set the offset of IMONA in the range from −32 to +31, representing by 2's complement method. For example, SET_IMON_RPT_OFSTA = 0b000101, IMON_RPT_OFSTA = +5 SET_IMON_RPT_OFSTA = 0b111011, IMON_RPT_OFSTA = −5

Table 55. SET_IMON_RPT_OFSB

Address: 0x3E								
Bit	7	6	5	4	3	2	1	0
Field	Reserved		SET_IMON_RPT_OFSB					
Default	0	0	0	0	0	0	0	0
Type	RW	RW	RW	RW	RW	RW	RW	RW

Bit	Name	Description
7:6	Reserved	Default value 0b00, not change
5:0	SET_IMON_RPT_OFSB	Set the offset of IMONB in the range from −32 to +31, representing by 2's complement method. For example, SET_IMON_RPT_OFSTB = 0b000101, IMON_RPT_OFSTB = +5 SET_IMON_RPT_OFSTB = 0b111011, IMON_RPT_OFSTB = −5

Table 56. SET_IMON_RPT_OFSC

Address: 0x3F								
Bit	7	6	5	4	3	2	1	0
Field	Reserved		SET_IMON_RPT_OFSC					
Default	0	0	0	0	0	0	0	0
Type	RW		RW					

Bit	Name	Description
7:6	Reserved	Default value 0b00, not change
5:0	SET_IMON_RPT_OFSC	Set the offset of IMONC in the range from −32 to +31, representing by 2's complement method. For example, SET_IMON_RPT_OFSTC = 0b000101, IMON_RPT_OFSTC = +5 SET_IMON_RPT_OFSTC = 0b111011, IMON_RPT_OFSTC = −5

Table 57. SEL_PSK_LIFT_VID

Address: 0x40								
Bit	7	6	5	4	3	2	1	0
Field	Reserved	SEL_PSK_LIFT_VID			Reserved			
Default	1	1	0	0	1	1	1	1
Type	RW	RW			RW			

Bit	Name	Description
7	Reserved	Default value 1, not change
6:4	SEL_PSK_LIFT_VID	Select lift VID amount in PSK mode 000: 0mV for rail A, B and C 001: 0mV for rail A, 5mV for rail B and C 010: 5mV for rail A, 0mV for rail B and C 011: 0mV for rail A, 10mV for rail B and C 100: 5mV for rail A, B and C 101: 5mV for rail A, 10mV for rail B and C 110: 10mV for rail A, 5mV for rail B and C 111: 10mV for rail A, B and C
3:0	Reserved	Default value 0b1111, not change

Table 58. EN_AUTO_TONA, SEL_AUTO_TON_MAXA, EN_AUTO_TONB, and SEL_AUTO_TON_MAXB

Address: 0x41								
Bit	7	6	5	4	3	2	1	0
Field	EN_AUTO_TONA	SEL_AUTO_TON_MAXA			EN_AUTO_TONB	SEL_AUTO_TON_MAXB		
Default	1	0	1	1	1	0	1	1
Type	RW	RW			RW	RW		

Bit	Name	Description
7	EN_AUTO_TONA	Enable limit the switching frequency in the range from 10 to 20kHz in PSK mode of rail A 0: Enable, 1: Disable
6:4	SEL_AUTO_TON_MAXA	Select the tON derating percentage in PSK mode of rail A 000: 100%, 001: 91.67%, 010: 83.33%, 011: 75%, 100: 66%, 101: 58.33%, 110: 50%, 111: 42%
3	EN_AUTO_TONB	Enable limit the switching frequency in the range from 10 to 20kHz in PSK mode of rail B 0: Enable, 1: Disable
2:0	SEL_AUTO_TON_MAXB	Select the tON derating percentage in PSK mode of rail B 000: 100%, 001: 91.67%, 010: 83.33%, 011: 75%, 100: 66%, 101: 58.33%, 110: 50%, 111: 42%

Table 59. EN_AUTO_TONC and SEL_AUTO_TON_MAXC

Address: 0x42								
Bit	7	6	5	4	3	2	1	0
Field	EN_AUTO_TONC	SEL_AUTO_TON_MAXC			Reserved			
Default	1	0	1	1	1	0	0	0
Type	RW	RW	RW	RW	RW	RW	RW	RW

Bit	Name	Description
7	EN_AUTO_TONC	Enable limit the switching frequency in the range from 10 to 20kHz in PSK mode of rail C 0: Enable, 1: Disable
6:4	SEL_AUTO_TON_MAXC	Select the tON derating percentage in PSK mode of rail C 000: 100%, 001: 91.67%, 010: 83.33%, 011: 75%, 100: 66%, 101: 58.33%, 110: 50%, 111: 42%
3:0	Reserved	Default value 0b1000, not change

Table 60. SEL_HOLD_LPF_THA, SEL_HOLD_LPF_THA and SEL_HOLD_LPF_THA

Address: 0x44								
Bit	7	6	5	4	3	2	1	0
Field	Reserved		SEL_HOLD_LPF_THA		SEL_HOLD_LPF_THB		SEL_HOLD_LPF_THC	
Default	1	1	0	0	1	0	1	1
Type	RW		RW		RW		RW	

Bit	Name	Description
7:6	Reserved	Default value 0b11, not change
5:4	SEL_HOLD_LPF_THA	Select the threshold of difference between VSENA and VFBA to hold LPF in PSK mode of rail A 00: 0mV, 01: 2.5mV, 10: 5mV, 11: 7.5mV
3:2	SEL_HOLD_LPF_THB	Select the threshold of difference between VSENB and VFBB to hold LPF in PSK mode of rail B 00: 0mV, 01: 2.5mV, 10: 5mV, 11: 7.5mV
1:0	SEL_HOLD_LPF_THC	Select the threshold of difference between VSENC and VFBC to hold LPF in PSK mode of rail C 00: 0mV, 01: 2.5mV, 10: 5mV, 11: 7.5mV

Table 61. SEL_RST_LPF_CURRA, SEL_RST_LPF_CURB, and SEL_RST_LPF_CURRC

Address: 0x45								
Bit	7	6	5	4	3	2	1	0
Field	Reserved		SEL_RST_LPF_CURRA		SEL_RST_LPF_CURRB		SEL_RST_LPF_CURRC	
Default	1	0	1	1	0	0	1	1
Type	RW		RW		RW		RW	

Bit	Name	Description
7:6	Reserved	Default value 0b10, not change
5:4	SEL_RST_LPF_CURRA	Select the reset LPF current of rail A 00: 0.5μA, 01: 1μA, 10: 1.5μA, 11: 2μA
3:2	SEL_RST_LPF_CURRB	Select the reset LPF current of rail B 00: 0.5μA, 01: 1μA, 10: 1.5μA, 11: 2μA
1:0	SEL_RST_LPF_CURRC	Select the reset LPF current of rail C 00: 0.5μA, 01: 1μA, 10: 1.5μA, 11: 2μA

Table 62. EN_ANSA, EN_ANSB, and EN_ANSC

Address: 0x46								
Bit	7	6	5	4	3	2	1	0
Field	Reserved					EN_ANSA	EN_ANSB	EN_ANSC
Default	1	1	1	1	1	0	0	0
Type	RW					RW	RW	RW

Bit	Name	Description
7:3	Reserved	Default value 0b11111, not change
2	EN_ANSA	Enable acoustic noise suppression function of rail A 0: Disable, 1: Enable
1	EN_ANSB	Enable acoustic noise suppression function of rail B 0: Disable, 1: Enable
0	EN_ANSC	Enable acoustic noise suppression function of rail C 0: Disable, 1: Enable

Table 63. SEL_I_DVID_DROOPA, SEL_LIFT_VIDB & SEL_I_DVID_DROOPB

Address: 0x47								
Bit	7	6	5	4	3	2	1	0
Field	Reserved	SEL_I_DVID_DROOPA			SEL_LIFT_VIDB	SEL_I_DVID_DROOPB		
Default	1	0	0	0	0	0	1	0
Type	RW	RW	RW	RW	RW	RW	RW	RW

Bit	Name	Description
7	Reserved	Default value 1, not change
6:4	SEL_I_DVID_DROOPA	Select the ratio of compensation current I_{DVID_DROOP} to I_{DVID_LIFT} during DVID down period of rail A 000: 0.6, 001: 0.7, 010: 0.8, 011: 0.9, 100: 1.0, 101: 1.1, 110: 1.2, 111: 1.3
3	SEL_LIFT_VIDB	Select lifting VID amount of rail B 0: 5mV, 1: 10mV
2:0	SEL_I_DVID_DROOPB	Select the ratio of compensation current I_{DVID_DROOP} to I_{DVID_LIFT} during DVID down period of rail B 000: 0.6, 001: 0.7, 010: 0.8, 011: 0.9, 100: 1.0, 101: 1.1, 110: 1.2, 111: 1.3

Table 64. SEL_LIFT_VIDC and SEL_I_DVID_DROOPC

Address: 0x48								
Bit	7	6	5	4	3	2	1	0
Field	SEL_LIFT_VIDC	SEL_I_DVID_DROOPC			Reserved			
Default	0	0	0	1	1	1	1	1
Type	RW	RW			RW			

Bit	Name	Description
7	SEL_LIFT_VIDC	Select lifting VID amount of rail C 0: 5mV, 1: 10mV
6:4	SEL_I_DVID_DROOPC	Select the ratio of compensation current I_{DVID_DROOP} to I_{DVID_LIFT} during DVID down period of rail C 000: 0.6, 001: 0.7, 010: 0.8, 011: 0.9, 100: 1.0, 101: 1.1, 110: 1.2, 111: 1.3
3:0	Reserved	Default value 0b1111, not change

Table 65. SEL_MPH_LPF_LIMITA and SEL_MPH_LPF_LIMIT_HYSA

Address: 0x49								
Bit	7	6	5	4	3	2	1	0
Field	SEL_MPH_LPF_LIMITA				SEL_MPH_LPF_LIMIT_HYSA			
Default	0	1	1	1	0	0	1	0
Type	RW				RW			

Bit	Name	Description
7:4	SEL_MPH_LPF_LIMITA	Select multi-phase LPF limit of rail A 0000: 100mV, 0001: 120mV, 0010: 140mV, 0011: 160mV, 0100: 180mV, 0101: 200mV, 0110: 220mV, 0111: 240mV, 1000: 260mV, 1001: 280mV, 1010: 300mV, 1011: 320mV, 1100: 340mV, 1101: 360mV, 1110: 380mV, 1111: 400mV
3:0	SEL_MPH_LPF_LIMIT_HYSA	Select multi-phase hysteresis of LPF limit of rail A 0000: 0mV, 0001: 20mV, 0010: 40 mV, 0011: 60 mV, 0100: 80mV, 0101: 100mV, 0110: 120mV, 0111: 140mV, 1000: 160mV, 1001: 180mV, 1010: 200mV, 1011: 220mV, 1100: 240mV, 1101: 260mV, 1110: 280mV, 1111: 300mV

Table 66. SEL_1PH_LPF_LIMITA and SEL_1PH_LPF_LIMIT_HYSA

Address: 0x4A								
Bit	7	6	5	4	3	2	1	0
Field	SEL_1PH_LPF_LIMITA				SEL_1PH_LPF_LIMIT_HYSA			
Default	0	0	1	1	0	1	0	0
Type	RW				RW			

Bit	Name	Description
7:4	SEL_1PH_LPF_LIMITA	Select single-phase LPF limit of rail A 0000: 50mV, 0001: 60mV, 0010: 70mV, 0011: 80mV, 0100: 90mV, 0101: 100mV, 0110: 110mV, 0111: 120mV, 1000: 130mV, 1001: 140mV, 1010: 150mV, 1011: 160mV, 1100: 170mV, 1101: 180mV, 1110: 190mV, 1111: 200mV
3:0	SEL_1PH_LPF_LIMIT_HYSA	Select single-phase hysteresis of LPF limit of rail A 0000: 0mV, 0001: 10mV, 0010: 20mV, 0011: 30mV, 0100: 40mV, 0101: 50mV, 0110: 60mV, 0111: 70mV, 1000: 80mV, 1001: 90mV, 1010: 100mV, 1011: 110mV, 1100: 120mV, 1101: 130mV, 1110: 140mV, 1111: 150mV

Table 67. SEL_1PH_LPF_LIMITB and SEL_1PH_LPF_LIMITC

Address: 0x4D								
Bit	7	6	5	4	3	2	1	0
Field	Reserved	SEL_1PH_LPF_LIMITB			Reserved	SEL_1PH_LPF_LIMITC		
Default	0	1	0	0	0	1	1	1
Type	RW	RW			RW	RW		

Bit	Name	Description
7	Reserved	Default value 0, not change
6:4	SEL_1PH_LPF_LIMITB	Select LPF limit of rail B 000: Disable, 001: 150mV, 010: 200mV, 011: 250mV, 100: 300mV, 101: 350mV, 110: 400mV, 111: 450mV
3	Reserved	Default value 0, not change
2:0	SEL_1PH_LPF_LIMITC	Select LPF limit of rail C 000: Disable, 001: 150mV, 010: 200mV, 011: 250mV, 100: 300mV, 101: 350mV, 110: 400mV, 111: 450mV

Table 68. SEL_LPF_INITB and SEL_LPF_INITC

Address: 0x4E								
Bit	7	6	5	4	3	2	1	0
Field	SEL_LPF_INITB				SEL_LPF_INITC			
Default	0	0	1	0	0	0	1	0
Type	RW				RW			

Bit	Name	Description
7:4	SEL_LPF_INITB	Set initial current of LPF of rail B 0000: –1.5μA, 0001: –0.5μA, 0010: –5μA, 0011: –4μA, 0100: –1μA, 0101: 0μA, 0110: –4μA, 0111: –3μA, 1000: –0.5μA, 1001: +0.5μA, 1010: –3.5μA, 1011: –2.5μA, 1100: 0μA, 1101: +1μA, 1110: –3μA, 1111: –2μA
3:0	SEL_LPF_INITC	Set initial current of LPF of rail C 0000: –1.5μA, 0001: –0.5μA, 0010: –5μA, 0011: –4μA, 0100: –1μA, 0101: 0μA, 0110: –4μA, 0111: –3μA, 1000: –0.5μA, 1001: +0.5μA, 1010: –3.5μA, 1011: –2.5μA, 1100: 0μA, 1101: +1μA, 1110: –3μA, 1111: –2μA

Table 69. SET_VBOOTA

Address: 0x50								
Bit	7	6	5	4	3	2	1	0
Field	SET_VBOOTA							
Default	0	0	0	0	0	0	0	0
Type	RW							

Bit	Name	Description
7:0	SET_VBOOTA	Set VBOOT of rail A, when connecting the SD_GOOD pin to GND with a resistor. The VID table is setting by SEL_VID_TABLEA

Table 70. Reserved

Address: 0x51								
Bit	7	6	5	4	3	2	1	0
Field	Reserved							
Default	1	0	1	0	0	0	0	1
Type	RW							

Bit	Name	Description
7:0	Reserved	Default value A1h, not change

Table 71. SET_VBOOTB

Address: 0x52								
Bit	7	6	5	4	3	2	1	0
Field	SET_VBOOTB							
Default	0	0	0	0	0	0	0	0
Type	RW							

Bit	Name	Description
7:0	SET_VBOOTB	Set VBOOT of rail B, when connecting the SD_GOOD pin to GND with a resistor. The VID table is setting by SEL_VID_TABLEB

Table 72. Reserved

Address: 0x53								
Bit	7	6	5	4	3	2	1	0
Field	Reserved							
Default	1	0	1	0	0	0	0	1
Type	RW							

Bit	Name	Description
7:0	Reserved	Default value A1h, not change

Table 73. SET_VBOOTC

Address: 0x54								
Bit	7	6	5	4	3	2	1	0
Field	SET_VBOOTC							
Default	0	0	0	0	0	0	0	0
Type	RW							

Bit	Name	Description
7:0	SET_VBOOTC	Set VBOOT of rail C, when connecting the SD_GOOD pin to GND with a resistor. The VID table is setting by SEL_VID_TABLEC

Table 74. Reserved

Address: 0x55								
Bit	7	6	5	4	3	2	1	0
Field	Reserved							
Default	1	0	1	0	0	0	0	1
Type	RW							

Bit	Name	Description
7:0	Reserved	Default value A1h, not change

Table 75. EN_2X_RIPPLE_COMPB, SEL_RIPPLE_COMPB, EN_2X_RIPPLE_COMPC, and SEL_RIPPLE_COMPC

Address: 0x56								
Bit	7	6	5	4	3	2	1	0
Field	EN_2X_RIPPLE_COMPB	SEL_RIPPLE_COMPB			EN_2X_RIPPLE_COMPC	SEL_RIPPLE_COMPC		
Default	1	0	1	0	0	0	0	1
Type	RW	RW			RW	RW		

Bit	Name	Description
7	EN_2X_RIPPLE_COMPB	Enable/Disable ripple compensation current x2 of Rail B corresponding to the register of SET_RIPPLE_COMPB 0: Disable 1: Enable
6:4	SEL_RIPPLE_COMPB	Adding auxiliary compensation current to VEA for compensating frequency difference when VID = 0.3V ~ 0.9V of Rail B, which helps the output voltage to reach the target within the specified time during DVID transition. Icomp = VID/1.123MΩ x SEL_RIPPLE_COMPB As EN_2X_RIPPLE_COMPB = 0, 000: x0 001: x1 010: x2 011: x3 100: x4 101: x5 110: x6 111: x7 As EN_2X_RIPPLE_COMPB = 1, 000: x0 001: x2 010: x4 011: x6 100: x8 101: x10 110: x12 111: x14
3	EN_2X_RIPPLE_COMPC	Enable/Disable ripple compensation current x2 of Rail C corresponding to the register of SET_RIPPLE_COMPC 0: Disable 1: Enable
2:0	SEL_RIPPLE_COMPC	Adding auxiliary compensation current to VEA for compensating frequency difference when VID = 0.3V ~ 0.9V of Rail C, which helps the output voltage to reach the target within the specified time during DVID transition. Icomp = VID/1.123MΩ x SEL_RIPPLE_COMPC As EN_2X_RIPPLE_COMPC = 0, 000: x0 001: x1 010: x2 011: x3 100: x4 101: x5

Bit	Name	Description
		110: x6 111: x7 As EN_2X_RIPPLE_COMPC = 1, 000: x0 001: x2 010: x4 011: x6 100: x8 101: x10 110: x12 111: x14

Table 76. SEL_SPM_HYSA2 and SEL_SPM_THA2

Address: 0x57								
Bit	7	6	5	4	3	2	1	0
Field	SEL_SPM_HYSA2			SEL_SPM_THA2				
Default	0	1	0	1	1	1	1	0
Type	RW			RW				

Bit	Name	Description
7:5	SEL_SPM_HYSA2	Select smart phase management hysteresis from 2 phases to 1 phase of rail A For example, SEL_SPM_HYSA2 = 0b010, EN_2X_SPM_HYS = 0, hysteresis = 2.5% of ICCMAXA EN_2X_SPM _HYS = 0, 000: 0%, 001: 1.25%, 010: 2.5%, 011: 3.75%, 100: 5%, 101: 6.25%, 110: 7.5%, 111: 8.75% EN_2X_ SPM _HYS = 1, 000: 0%, 001: 2.5%, 010: 5%, 011: 7.5%, 100: 10%, 101: 12.5%, 110: 15%, 111: 17.5%
4:0	SEL_SPM_THA2	Select smart phase management threshold from 1 phase to 2 phases of rail A For example, SEL_SPM_THA2 = 0b00001, threshold = 94% of ICCMAXA 00000: 100%, 00001: 94%, 00010: 88%, 00011: 82%, 00100: 76%, 00101: 70%, 00110: 66%, 00111: 62%, 01000: 58%, 01001: 54%, 01010: 50%, 01011: 48%, 01100: 46%, 01101: 44%, 01110: 42%, 01111: 40%, 10000: 38%, 10001: 36%, 10010: 34%, 10011: 32%, 10100: 30%, 10101: 28%, 10110: 26%, 10111: 24%, 11000: 22%, 11001: 20%, 11010: 18%, 11011: 16%, 11100: 14%, 11101: 12%, 11110: 10%, 11111: 8%

Table 77. SEL_SPM_HYSA3 and SEL_SPM_THA3

Address: 0x58								
Bit	7	6	5	4	3	2	1	0
Field	SEL_SPM_HYSA3			SEL_SPM_THA3				
Default	0	0	1	1	1	1	0	0
Type	RW			RW				

Bit	Name	Description
7:5	SEL_SPM_HYSA3	Select smart phase management hysteresis from 3 phases to 2 phases of rail A. Bit field definition is the same as SEL_SPM_HYSA2
4:0	SEL_SPM_THA3	Select smart phase management threshold from 2 phases to 3 phases of rail A. Bit field definition is the same as SEL_SPM_THA2

Table 78. SEL_SPM_HYSA4 and SEL_SPM_THA4

Address: 0x59								
Bit	7	6	5	4	3	2	1	0
Field	SEL_SPM_HYSA4			SEL_SPM_THA4				
Default	0	0	1	1	1	0	1	0
Type	RW			RW				

Bit	Name	Description
7:5	SEL_SPM_HYSA4	Select smart phase management hysteresis from 4 phases to 3 phases of rail A. Bit field definition is the same as SEL_SPM_HYSA2
4:0	SEL_SPM_THA4	Select smart phase management threshold from 3 phases to 4 phases of rail A. Bit field definition is the same as SEL_SPM_THA2

Table 79. SEL_SPM_HYSA5 and SEL_SPM_THA5

Address: 0x5A								
Bit	7	6	5	4	3	2	1	0
Field	SEL_SPM_HYSA5			SEL_SPM_THA5				
Default	0	0	1	1	1	0	0	1
Type	RW			RW				

Bit	Name	Description
7:5	SEL_SPM_HYSA5	Select smart phase management hysteresis from 5 phases to 4 phases of rail A. Bit field definition is the same as SEL_SPM_HYSA2
4:0	SEL_SPM_THA5	Select smart phase management threshold from 4 phases to 5 phases of rail A. Bit field definition is the same as SEL_SPM_THA2

Table 80. SEL_SPM_HYSA6 and SEL_SPM_THA6

Address: 0x5B								
Bit	7	6	5	4	3	2	1	0
Field	SEL_SPM_HYSA6			SEL_SPM_THA6				
Default	0	0	1	1	1	0	0	0
Type	RW			RW				

Bit	Name	Description
7:5	SEL_SPM_HYSA6	Select smart phase management hysteresis from 6 phases to 5 phases of rail A. Bit field definition is the same as SEL_SPM_HYSA2
4:0	SEL_SPM_THA6	Select smart phase management threshold from 5 phases to 6 phases of rail A. Bit field definition is the same as SEL_SPM_THA2

Table 81. SEL_SPM_HYSA7 and SEL_SPM_THA7

Address: 0x5C								
Bit	7	6	5	4	3	2	1	0
Field	SEL_SPM_HYSA7			SEL_SPM_THA7				
Default	0	0	1	1	0	1	0	1
Type	RW			RW				

Bit	Name	Description
7:5	SEL_SPM_HYSA7	Select smart phase management hysteresis from 7 phases to 6 phases of rail A. Bit field definition is the same as SEL_SPM_HYSA2
4:0	SEL_SPM_THA7	Select smart phase management threshold from 6 phases to 7 phases of rail A. Bit field definition is the same as SEL_SPM_THA2

Table 82. SEL_SPM_HYSA8 and SEL_SPM_THA8

Address: 0x5D								
Bit	7	6	5	4	3	2	1	0
Field	SEL_SPM_HYSA8			SEL_SPM_THA8				
Default	0	0	1	1	0	0	1	1
Type	RW			RW				

Bit	Name	Description
7:5	SEL_SPM_HYSA8	Select smart phase management hysteresis from 8 phases to 7 phases of rail A. Bit field definition is the same as SEL_SPM_HYSA2
4:0	SEL_SPM_THA8	Select smart phase management threshold from 7 phases to 8 phases of rail A. Bit field definition is the same as SEL_SPM_THA2

Table 83. EN_2X_SPM_HYS, SEL_SPM_TH_RATIO, and SEL_SPM_SHED_DLYA

Address: 0x5E								
Bit	7	6	5	4	3	2	1	0
Field	EN_2X_SPM_HYS	SEL_SPM_TH_RATIO		SEL_SPM_SHED_DLYA			Reserved	
Default	1	0	1	0	1	1	0	0
Type	RW	RW		RW			RW	

Bit	Name	Description
7	EN_2X_SPM_HYS	Enable 2X hysteresis of smart phase management 0: Disable, 1: Enable
6:5	SEL_SPM_TH_RATIO	Derating the threshold of smart phase management 00: 100%, 01: 50%, 10: 37.5%, 11: 25%
4:2	SEL_SPM_SHED_DLYA	Select the delay when phase down in smart phase management of rail A 000: 5µs, 001: 3.75µs, 010: 2.5µs, 011: 1.25µs, 100: 20µs, 101: 15µs, 110: 10µs, 111: 5µs
1:0	Reserved	Default value 0b00, not change

Table 84. SEL_ZCD_HYSB and SEL_ZCD_HYSC

Address: 0x5F								
Bit	7	6	5	4	3	2	1	0
Field	Reserved				SEL_ZCD_HYSB		SEL_ZCD_HYSC	
Default	0	0	0	0	0	1	0	1
Type	RW				RW		RW	

Bit	Name	Description
7:4	Reserved	Default value 0b0000, not change
3:2	SEL_ZCD_HYSB	Select the ZCD hysteresis of rail B 00: 0.25mV, 01: 0.5mV, 10: 0.75mV, 11: 1mV
1:0	SEL_ZCD_HYSC	Select the ZCD hysteresis of rail C 00: 0.25mV, 01: 0.5mV, 10: 0.75mV, 11: 1mV

Table 85. SEL_ANS_PS4_BEHAV, EN_DBLR_SPM_1PH_CCM, EN_SPS_TSENA, EN_SPS_TSENB, and EN_SPS_TSENC

Address: 0x60								
Bit	7	6	5	4	3	2	1	0
Field	SEL_ANS_PS4_BEHAV	EN_DBLR_SPM_1PH_CCM	Reserved			EN_SPS_TSENA	EN_SPS_TSENB	EN_SPS_TSENC
Default	0	0	1	1	1	0	0	0
Type	RW	RW	RW			RW	RW	RW

Bit	Name	Description
7	SEL_ANS_PS4_BEHAV	Select the SetPS4 behavior when ANS is enable and no action for DVID down (SEL_ANS_BEHAV = 0) 0: ACK for SetPS4 and enter the PS4 1: ACK for SetPS4 and not enter the PS4
6	EN_DBLR_SPM_1PH_CCM	Enable single-phase CCM detection in smart phase management when using phase doubler 0: Disable, 1: Enable
5:3	Reserved	Default value 0b111, not change
2	EN_SPS_TSENA	Enable SPS TSEN table with positive temperature coefficient of rail A 0: Disable, 1: Enable
1	EN_SPS_TSENB	Enable SPS TSEN table with positive temperature coefficient of rail B 0: Disable, 1: Enable
0	EN_SPS_TSENC	Enable SPS TSEN table with positive temperature coefficient of rail C 0: Disable, 1: Enable

Table 86. SEL_SPM_SHED_DLYB, SEL_SPM_SHED_DLYC, SEL_PIN51_CONFIG, and EN_2X_Ai_GAINA

Address: 0x61								
Bit	7	6	5	4	3	2	1	0
Field	SEL_SPM_SHED_DLYB			SEL_SPM_SHED_DLYC			SEL_PIN51_CONFIG	EN_2X_Ai_GAINA
Default	0	0	0	0	0	0	0	0
Type	RW			RW			RW	RW

Bit	Name	Description
7:5	SEL_SPM_SHED_DLYB	Select the delay from CCM to DCM in smart phase management of rail B 000: 5µs, 001: 3.75µs, 010: 2.5µs, 011: 1.25µs, 100: 20µs, 101: 15µs, 110: 10µs, 111: 5µs
4:2	SEL_SPM_SHED_DLYC	Select the delay from CCM to DCM in smart phase management of rail C 000: 5µs, 001: 3.75µs, 010: 2.5µs, 011: 1.25µs, 100: 20µs, 101: 15µs, 110: 10µs, 111: 5µs
1	SEL_PIN51_CONFIG	Select the configuration of the DRVEN/DBLR_PS pin 0: The DRVEN/DBLR_PS pin is configured as DRVEN 1: The DRVEN/DBLR_PS pin is configured as DBLR_PS
0	EN_2X_Ai_GAINA	Enable double Ai gain of rail A 0: Disable 1: Enable

Table 87. SET_SPS_TSEN_RPT_OFSA

Address: 0x62								
Bit	7	6	5	4	3	2	1	0
Field	Reserved		SET_SPS_TSEN_RPT_OFSA					
Default	0	0	1	0	0	0	0	0
Type	RW		RW					

Bit	Name	Description
7:6	Reserved	Unimplemented, default value is 0b00
5:0	SET_SPS_TSEN_RPT_OFSA	Set the reporting offset of SPS TSEN of rail A in the range from –32 to +31. 000000: –31, 000001: –31, 000010: –30, 000011: –29, 000100: –28, 000101: –27, 000110: –26, 000111: –25, 001000: –24, 001001: –23, 001010: –22, 001011: –21, 001100: –20, 001101: –19, 001110: –18, 001111: –17, 010000: –16, 010001: –15, 010010: –14, 010011: –13, 010100: –12, 010101: –11, 010110: –10, 010111: –9, 011000: –8, 011001: –7, 011010: –6, 011011: –5, 011100: –4, 011101: –3, 011110: –2, 011111: –1 100000: 0, 100001: 1, 100010: 2, 100011: 3, 100100: 4, 100101: 5, 100110: 6, 100111: 7, 101000: 8, 101001: 9, 101010: 10, 101011: 11, 101100: 12, 101101: 13, 101110: 14, 101111: 15, 110000: 16, 110001: 17, 110010: 18, 110011: 19, 110100: 20, 110101: 21, 110110: 22, 110111: 23, 111000: 24, 111001: 25, 111010: 26, 111011: 27, 111100: 28, 111101: 29, 111110: 30, 111111: 31

Table 88. SET_SPS_TSEN_RPT_OFSB

Address: 0x63								
Bit	7	6	5	4	3	2	1	0
Field	Reserved		SET_SPS_TSEN_RPT_OFSB					
Default	0	0	1	0	0	0	0	0
Type	RW	RW	RW	RW	RW	RW	RW	RW

Bit	Name	Description
7:6	Reserved	Unimplemented, default value is 0b00
5:0	SET_SPS_TSEN_RPT_OFSB	Set the reporting offset of SPS TSEN of rail B in the range from –32 to +31. Bit field definition is the same as SET_SPS_TSEN_RPT_OFSA

Table 89. SET_SPS_TSEN_RPT_OFSC

Address: 0x64								
Bit	7	6	5	4	3	2	1	0
Field	Reserved		SET_SPS_TSEN_RPT_OFSC					
Default	0	0	1	0	0	0	0	0
Type	RW		RW					

Bit	Name	Description
7:6	Reserved	Unimplemented, default value is 0b00
5:0	SET_SPS_TSEN_RPT_OFSC	Set the reporting offset of SPS TSEN of rail C in the range from −32 to +31. Bit field definition is the same as SET_SPS_TSEN_RPT_OFSA

Table 90. EN_RAIL

Address: 0x66								
Bit	7	6	5	4	3	2	1	0
Field	EN_RAIL	Reserved						
Default	0	0	0	0	0	0	0	0
Type	RW	RW						

Bit	Name	Description
7	EN_RAIL	Control the ON/OFF status for the output of all rails 0: Disable 1: Enable
6:0	Reserved	Unimplemented, the default value is 0b0000000

Table 91. SET_CODE_VER_LB

Address: 0x70								
Bit	7	6	5	4	3	2	1	0
Field	SET_CODE_VER_LB							
Default	0	0	0	0	0	0	0	0
Type	RW							

Bit	Name	Description
7:0	SET_CODE_VER_LB	Set the low byte of the code version

Table 92. SET_CODE_VER_HB

Address: 0x71								
Bit	7	6	5	4	3	2	1	0
Field	SET_CODE_VER_HB							
Default	0	0	0	0	0	0	0	0
Type	RW							

Bit	Name	Description
7:0	SET_CODE_VER_HB	Set the high byte of the code version

Table 93. SET_PRODUCT_ID

Address: 0x74								
Bit	7	6	5	4	3	2	1	0
Field	SET_PRODUCT_ID							
Default	0	0	1	1	1	0	0	0
Type	RW							

Bit	Name	Description
7:0	SET_PRODUCT_ID	Set the product ID. Default value is 0x38

Table 94. CRC

Address: 0x7F								
Bit	7	6	5	4	3	2	1	0
Field	CRC							
Default	--	--	--	--	--	--	--	--
Type	R							

Bit	Name	Description
7:0	CRC	Cyclic redundancy check

Table 95. CBGA1 and CBGA2

Address: 0x90 **Description:** Adjust current balance gain of phase 1 and 2 of rail A								
Bit	7	6	5	4	3	2	1	0
Field	Reserved	CBGA1			Reserved	CBGA2		
Default	0	1	0	0	0	1	0	0
Type	RW	RW			RW	RW		

Bit	Name	Description
7	Reserved	Unimplemented, the default value is 0
6:4	CBGA1	000: 69.2%, 001: 76.9%, 010: 84.6%, 011: 92.3%, 100: 100% (default), 101: 107.69%, 110: 115.38%, 111: 123.08%
3	Reserved	Unimplemented, the default value is 0
2:0	CBGA2	Bit field definition and the default value is the same as CBGA1

Table 96. CBGA3 and CBGA4

Address: 0x91 **Description:** Adjust current balance gain of phase 3 and 4 of rail A								
Bit	7	6	5	4	3	2	1	0
Field	Reserved	CBGA3			Reserved	CBGA4		
Default	0	1	0	0	0	1	0	0
Type	RW	RW			RW	RW		

Bit	Name	Description
7	Reserved	Unimplemented, the default value is 0
6:4	CBGA3	Bit field definition and the default value is the same as CBGA1
3	Reserved	Unimplemented, the default value is 0
2:0	CBGA4	Bit field definition and the default value is the same as CBGA1

Table 97. CBGA5 and CBGA6

Address: 0x92 **Description:** Adjust current balance gain of phase 5 and 6 of rail A								
Bit	7	6	5	4	3	2	1	0
Field	Reserved	CBGA5			Reserved	CBGA6		
Default	0	1	0	0	0	1	0	0
Type	RW	RW			RW	RW		

Bit	Name	Description
7	Reserved	Unimplemented, the default value is 0
6:4	CBGA5	Bit field definition and the default value is the same as CBGA1
3	Reserved	Unimplemented, the default value is 0
2:0	CBGA6	Bit field definition and the default value is the same as CBGA1

Table 98. CBGA7 and CBGA8

Address: 0x93 **Description:** Adjust current balance gain of phase 7 and 8 of rail A								
Bit	7	6	5	4	3	2	1	0
Field	Reserved	CBGA7			Reserved	CBGA8		
Default	0	1	0	0	0	1	0	0
Type	RW	RW			RW	RW		

Bit	Name	Description
7	Reserved	Unimplemented, the default value is 0
6:4	CBGA7	Bit field definition and the default value is the same as CBGA1
3	Reserved	Unimplemented, the default value is 0
2:0	CBGA8	Bit field definition and the default value is the same as CBGA1

Table 99. VFIXA_LB

Address: 0x94
Description: 9-bit fixed VID (Reg. 0x94 + Reg. 0x95). Set the voltage in fixed VID mode of rail A. In fixed VID mode, VR skips the SetVID/SetPS command. (VR has no actions but still asserts ALERT immediately after receiving the SetVID command, while the VR output voltage stays at the fixed VID.) While fixed VID is enabled, VR does not act for the I2C voltage offset as well. After disabling fixed VID mode, VID returns to the last SetVID target and last power state. When entering/exiting fixed VID mode, VID slew rate is 1/2 of the fast slew rate.

Bit	7	6	5	4	3	2	1	0
Field	VFIXA_LB							
Default (VID1)	1	0	0	0	0	0	1	1
Default (VID2)	1	0	1	0	0	0	0	1
Type	RW							

Bit	Name	Description
7:0	VFIXA_LB	Voltage of fixed VID mode = 0.0V when receiving an off code (VFIXA_HB [0] = 00h + VFIXA_LB[7:0] = 00h) SEL_VID_TABLEA = 0, Voltage of fixed VID mode = 0.245V + (VFIXA_HB [0] + VFIXA_LB[7:0]) x 5mV, (VID1), voltage range from 0.25V to 2.17V. SEL_VID_TABLEA = 1, Voltage of fixed VID mode = 0.19V + (VFIXA_HB [0] + VFIXA_LB[7:0]) x 10mV, (VID2), voltage range from 0.2V to 3.04V. Refer to Figure 35 for Control Logic.

Table 100. VFIXA_HB

Address: 0x95
Description: 9-bit fixed VID (Reg. 0x94 + Reg. 0x95). Set the voltage in fixed VID mode of rail A. In fixed VID mode, VR skips the SetVID/SetPS command. (VR has no actions but still asserts ALERT immediately after receiving the SetVID command, while the VR output voltage stays at the fixed VID.) While fixed VID is enabled, VR does not act for the I2C voltage offset as well. After disabling fixed VID mode, VID returns to the last SetVID target and last power state. When entering/exiting fixed VID mode, VID slew rate is 1/2 of the fast slew rate.

Bit	7	6	5	4	3	2	1	0
Field	VFIXA_HB							
Default	0	0	0	0	0	0	0	0
Type	R							RW

Bit	Name	Description
7:0	VFIXA_HB	Voltage of fixed VID mode = 0.0V when receives an off code (VFIXA_HB [0] = 00h + VFIXA_LB[7:0] = 00h) SEL_VID_TABLEA = 0, Voltage of fixed VID mode = 0.245V + (VFIXA_HB [0]+VFIXA_LB[7:0]) x 5mV, (VID1), voltage range from 0.25V to 2.17V. SEL_VID_TABLEA = 1, Voltage of fixed VID mode = 0.19V + (VFIXA_HB [0] + VFIXA_LB[7:0]) x 10mV, (VID2), voltage range from 0.2V to 3.04V. Refer to Figure 35 for Control Logic.

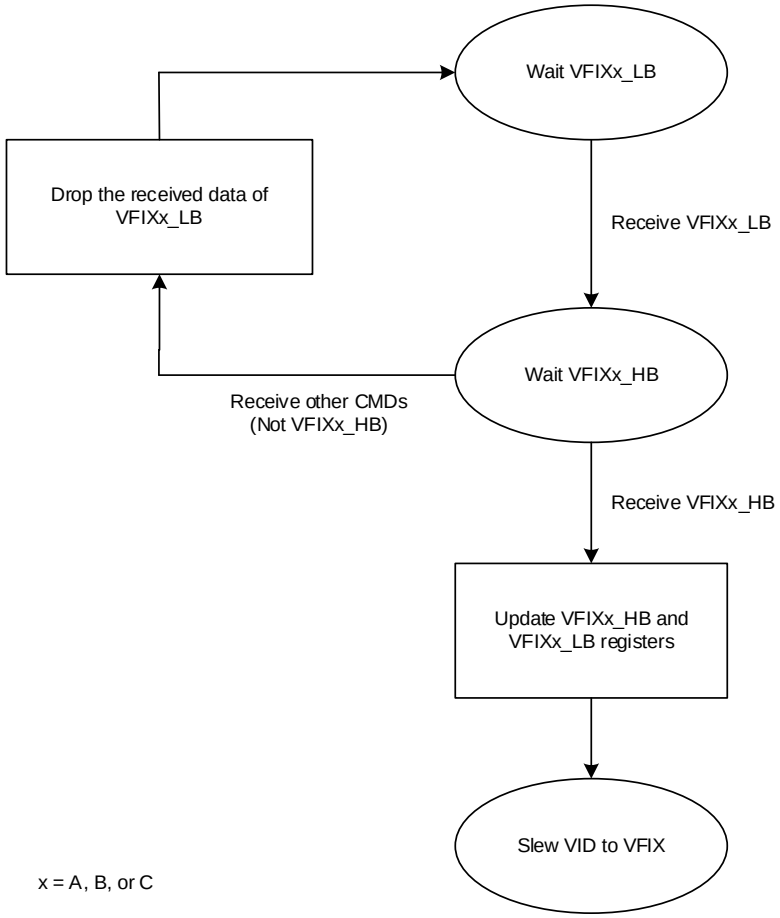


Figure 35. Control Logic of Command VFIX

Table 101. VOFSA

Address: 0x96
Description: Setting the offset voltage of rail A. For VID1 the final voltage limiting range 0.25V to 2.17V. (For example, 0.25V ≤ VID setting ± SVID offset voltage ± I^2C offset voltage ≤ 2.17V.) For VID2, the final voltage limiting range is from 0.2V to 3.04V. The offset slew rate is 1/2 of the fast slew rate. While setting the voltage offset, the VR should return to the power state PS0. After VSEN settles at the target offset voltage, the power state (PS) goes back to the original PS. If CPU sends the SetPS1/2/3 command, the controller follows PS and the voltage offset still exists. If CPU sends SetVID off code command (VID setting ± SVID offset voltage ± I^2C offset voltage), the controller sets output voltage to 0V.

Bit	7	6	5	4	3	2	1	0
Field	VOFSA							
Default	0	0	0	0	0	0	0	0
Type	RW							

Bit	Name	Description
7:0	VOFSA	[7:0] = 00h: No offset [7]: Sign bit (as part of two's complement) [6:0]: 5mV/step (SEL_VID_TABLEA = 0) or 10mV/step (SEL_VID_TABLEA = 1) For example, 0b00000001 = current VID + (1 x VID step) 0b00000011 = current VID + (3 x VID steps) 0b11111111 = current VID - (1 x VID step)

Table 102. TEMP_ALERT and TEMP_VRHOT

Address: 0x97
Description: Setting rail A's ALERT temperature and thermal VRHOT temperature. The VRHOT temperature should be higher than the ALERT temperature. While the VRHOT temperature is lower than the thermal ALERT temperature, the VR will enforce that the ALERT temperature is smaller than the VRHOT temperature (TEMP_VRHOTA[7:4] = TEMP_ALERTA[3:0]).

Bit	7	6	5	4	3	2	1	0
Field	TEMP_ALERTA				TEMP_VRHOTA			
Default	0	1	1	0	0	1	1	0
Type	RW							

Bit	Name	Description
7:4	TEMP_ALERTA	Select thermal ALERT temperature of rail A. Temperature versus $V_{THERMAL}$, refer to Table 105. 0000: 75°C, 0001: 82°C, 0010: 85°C, 0011: 88°C, 0100: 91°C, 0101: 94°C, 0110: 97°C, 0111: 100°C, 1000: 103°C, 1001: 106°C, 1010: 109°C, 1011: 112°C, 1100: 115°C, 1101: 118°C, 1110: 121°C, 1111: 124°C
3:0	TEMP_VRHOTA	Select VRHOT temperature of rail A. Temperature versus $V_{THERMAL}$, refer to Table 105. 0000: 82°C, 0001: 85°C, 0010: 88°C, 0011: 91°C, 0100: 94°C, 0101: 97°C, 0110: 100°C, 0111: 103°C, 1000: 106°C, 1001: 109°C, 1010: 112°C, 1011: 115°C, 1100: 118°C, 1101: 121°C, 1110: 124°C, 1111: 127°C

Table 103. SUM_OCP_DEB_TIMEA, EN_SS_OCPA, EN_SUM_OCPA, EN_NVA, and EN_OVA

Address: 0x98
Description: Enable protection function of rail A

Bit	7	6	5	4	3	2	1	0
Field	Reserved		SUM_OCP_DEB_TIMEA	EN_SS_OCPA	EN_SUM_OCPA	EN_NVA	EN_UVA	EN_OVA
Default	0	0	-	-	1	1	1	1
Type	RW		RW	RW	RW	RW	RW	RW

Bit	Name	Description
7:6	Reserved	Unimplemented, the default value is 0b00
5	SUM_OCP_DEB_TIMEA	0: 20μs, 1: 40μs The default value is from SEL_SUM_OCP_DEB_TIMEA (0x2B[7]) in the setting function table.
4	EN_SS_OCPA	0: Disable soft-start OC protection, 1: Enable soft-start OC protection The default value is from EN_SS_OCPA (0x2F[2]) in the setting function table.
3	EN_SUM_OCPA	0: Disable sum OC protection, 1: Enable sum OC protection (default)
2	EN_NVA	0: Disable NV protection, 1: Enable NV protection (default)
1	EN_UVA	0: Disable UV protection, 1: Enable UV protection (default) The default value is from EN_UVA (0x27[2]) in the setting function table.
0	EN_OVA	0: Disable OV protection, 1: Enable OV protection (default)

Table 104. OCA, NVA, UVA, and OVA

Address: 0x99 **Description**: Protection indicator of rail A								
Bit	7	6	5	4	3	2	1	0
Field	Reserved				OCA	NVA	UVA	OVA
Default	0	0	0	0	0	0	0	0
Type	R				R	R	R	R

Bit	Name	Description
7:4	Reserved	Unimplemented, the default value is 0b0000
3	OCA	0: No occurrence of OCP, 1: Occurrence of OCP
2	NVA	0: No occurrence of negative-voltage protection (NVP), 1: Occurrence of NVP
1	UVA	0: No occurrence UVP, 1: Occurrence UVP
0	OVA	0: No occurrence of OVP, 1: Occurrence of OVP

Table 105. ILOAD_RPTA

Address: 0x9A **Description**: Output current reporting of rail A								
Bit	7	6	5	4	3	2	1	0
Field	ILOAD_RPTA							
Default	-	-	-	-	-	-	-	-
Type	R							

Bit	Name	Description
7:0	ILOAD_RPTA	Output current reporting

Table 106. PSYS_RPT

Address: 0x9B **Description**: PSYS reporting								
Bit	7	6	5	4	3	2	1	0
Field	PSYS_RPT							
Default	-	-	-	-	-	-	-	-
Type	R							

Bit	Name	Description
7:0	PSYS_RPT	PSYS reporting

Table 107. TEMP_RPTA

Address: 0x9C **Description**: Temperature reporting of rail A								
Bit	7	6	5	4	3	2	1	0
Field	TEMP_RPTA							
Default	--	--	--	--	--	--	--	--
Type	R							

Bit	Name	Description
7:0	TEMP_RPTA	$V_{THERMAL}$ = TEMP_RPTA x 6.25mV. Temperature versus $V_{THERMAL}$ refer to Table 108.

Table 108. $V_{THERMAL}$ vs Temperature (based on the R_{NTC} = 100k/Beta = 4250K)

Temperature (°C)	$V_{THERMAL}$ (V)	Temperature (°C)	$V_{THERMAL}$ (V)	Temperature (°C)	$V_{THERMAL}$ (V)	Temperature (°C)	$V_{THERMAL}$ (V)
61	1.133	81	0.814	101	0.591	121	0.453
62	1.116	82	0.800	102	0.582	122	0.447
63	1.098	83	0.787	103	0.574	123	0.442
64	1.080	84	0.774	104	0.566	124	0.437
65	1.063	85	0.761	105	0.558	125	0.432
66	1.046	86	0.749	106	0.550	126	0.428
67	1.029	87	0.737	107	0.542	127	0.423
68	1.012	88	0.725	108	0.534	128	0.419
69	0.995	89	0.713	109	0.527	129	0.414
70	0.979	90	0.702	110	0.520	130	0.410
71	0.963	91	0.690	111	0.513		
72	0.947	92	0.679	112	0.506		
73	0.931	93	0.669	113	0.500		
74	0.916	94	0.658	114	0.493		
75	0.900	95	0.648	115	0.487		
76	0.885	96	0.638	116	0.481		
77	0.871	97	0.628	117	0.475		
78	0.856	98	0.618	118	0.469		
79	0.842	99	0.609	119	0.463		
80	0.828	100	0.600	120	0.458		

Table 109. VOFS_LOAD_HYSA & VOFS_LOAD_THA

Address: 0x9E **Description**: Load condition for VID offset of rail A								
Bit	7	6	5	4	3	2	1	0
Field	VOFS_LOAD_HYSA		VOFS_LOAD_THA					
Default	1	0	0	0	0	0	0	0
Type	RW		RW					

Bit	Name	Description
7:6	VOFS_LOAD_HYSA	Select the current hysteresis 00: 4A, 01: 8A, 10: 12A, 11: 16A
5:0	VOFS_LOAD_THA	Set the current threshold from 0A to 504A with 8A/LSB

Table 110. ILOAD_RPT_RATIOA, FORCE_PS0A, and KTONA

Address: 0x9F **Description**: Adjust output current reporting ratio, enable or disable to force the PS0 function and K_{TON} of rail A								
Bit	7	6	5	4	3	2	1	0
Field	ILOAD_RPT_RATIOA			FORCE_PS0A	Reserved	KTONA		
Default	0	0	0	0	0	--	--	--
Type	RW			RW	RW	RW		

Bit	Name	Description
7:5	ILOAD_RPT_RATIOA	Output current reporting ratio 000: 100%, 001: 95%, 010: 90%, 011: 85%, 100: 80%, 101: 75%, 110: 60%, 111: 50%
4	FORCE_PS0A	Enable this function, VR will stay at PS0 even though the SetPS PS1, PS2, or PS3 command is received 0: Disable, 1: Enable
3	Reserved	Unimplemented, default value is 0
2:0	KTONA	On time factor K_{TON}. Refer to the section Switching Frequency Setting for the details. The default value is from SEL_KTONA (0x15[6:4]) in the setting function table.

Table 111. EN_FVMA, EN_FVMB, and EN_FVMC

Address: 0xA0 **Description**: Enable Fast V-Mode current limit function								
Bit	7	6	5	4	3	2	1	0
Field	Reserved	EN_FVMA	EN_FVMB	EN_FVMC	Reserved			
Default	0	1	1	1	0	0	0	0
Type	RW	RW	RW	RW	RW			

Bit	Name	Description
7	Reserved	Unimplemented, the default value is 0
6	EN_FVMA	Enable Fast V-Mode current limit function of rail A 0: Disable, 1: Enable
5	EN_FVMB	Enable Fast V-Mode current limit function of rail B 0: Disable, 1: Enable
4	EN_FVMC	Enable Fast V-Mode current limit function of rail C 0: Disable, 1: Enable
3:0	Reserved	Unimplemented, the default value is 0b0000

Table 112. EN_SPMA

Address: 0xA3 **Description**: SPM threshold, enable and hysteresis related settings of rail A								
Bit	7	6	5	4	3	2	1	0
Field	Reserved				EN_SPMA	Reserved		
Default	0	0	0	0	--	0	0	0
Type	RW				RW	RW		

Bit	Name	Description
7:4	Reserved	Unimplemented, the default value is 0b0000
3	EN_SPMA	Enable smart phase management function and the default value are from EN_SPM_DEFAULTA (0x27[3]) in the setting function table
2:0	Reserved	Unimplemented, the default value is 0b000

Table 113. PRODUCT_ID

Address: 0xA4								
Bit	7	6	5	4	3	2	1	0
Field	PRODUCT_ID							
Default	0	0	1	1	1	0	0	0
Type	RW							

Bit	Name	Description
7:0	PRODUCT_ID	Set the product ID. The default value is 0x38

Table 114. EN_ANSA and SMALL_LLA

Address: 0xA7 **Description**: Enable the acoustic noise suppression function and select small loadline of rail A								
Bit	7	6	5	4	3	2	1	0
Field	Reserved			EN_ANSA	SMALL_LLA			
Default	0	0	0	--	--	--	--	--
Type	RW			RW	RW			

Bit	Name	Description
7:5	Reserved	Unimplemented, the default value is 0b000
4	EN_ANSA	Enable acoustic noise suppression function. Bit field definition and the default value are from EN_ANSA (0x46[2]) in the setting function table.
3:0	SMALL_LLA	Small loadline. Bit field definition and the default value are from SEL_SMALL_LLA (0x17[3:0]) in the setting function table.

Table 115. VOFS_LOAD_OFSA

Address: 0xA8 **Description**: VID offset for load condition VOFS_LOADA (0x9E) of rail A								
Bit	7	6	5	4	3	2	1	0
Field	VOFS_LOAD_OFSA							
Default	0	0	0	0	0	0	0	0
Type	RW							

Bit	Name	Description
7:0	VOFS_LOAD_OFSA	Set the VID offset for load condition VOFS_LOADA (0x9E) [7:0] = 00h: No offset [7]: Sign bit (as part of two's complement) [6:0]: 5mV/step (SEL_VID_TABLEA = 0) or 10mV/step (SEL_VID_TABLEA = 1) For example, 0b00000001 = current VID + (1 x VID step) 0b00000011 = current VID + (3 x VID steps) 0b11111111 = current VID - (1 x VID step)

Table 116. LLA

Address: 0xA9 **Description**: Select loadline of rail A								
Bit	7	6	5	4	3	2	1	0
Field	Reserved			LLA				
Default	0	0	0	0	1	0	1	0
Type	RW			RW				

Bit	Name	Description
7:5	Reserved	Unimplemented, the default value is 0b000
4:0	LLA	Loadline setting. 1LSB = 10%. Range is from 0% to 200%. When LLA is above 15h, loadline will be 0%. For example, LLA = 0b01010, loadline = 100%, LLA = 0b10100, loadline = 200%, LLA = 0b10101, loadline = 0%

Table 117. EN_VFIXA, EN_VFIXB and EN_VFIXC

Address: 0xAA **Description**: Enable fixed VID mode								
Bit	7	6	5	4	3	2	1	0
Field	Reserved					EN_VFIXA	EN_VFIXB	EN_VFIXC
Default	0	0	0	0	0	0	0	0
Type	RW					RW	RW	RW

Bit	Name	Description
7:3	Reserved	Unimplemented, the default value is 0b00000
2	EN_VFIXA	0: Disable 1: Enable
1	EN_VFIXB	0: Disable 1: Enable
0	EN_VFIXC	0: Disable 1: Enable

Table 118. VFIXB_LB

Address: 0xAB
Description: 9-bit fixed VID (Reg. 0xAB + Reg. 0xAC). Set the voltage in fixed VID mode of rail B. In fixed VID mode, VR skips the SetVID/SetPS command. (VR has no actions but still asserts $\overline{\text{ALERT}}$ immediately after receiving the SetVID command, while the VR output voltage stays at the fixed VID.) While fixed VID is enabled, VR does not act for the I^2C voltage offset as well. After disabling fixed VID mode, VID returns to the last SetVID target and last power state. When entering/exiting fixed VID mode, VID slew rate is 1/2 of the fast slew rate.

Bit	7	6	5	4	3	2	1	0
Field	VFIXB_LB							
Default (VID1)	1	0	0	0	0	0	1	1
Default (VID2)	1	0	1	0	0	0	0	1
Type	RW							

Bit	Name	Description
7:0	VFIXB_LB	Voltage of fixed VID mode = 0.0V when receiving an off code (VFIXB_HB [0] = 00h + VFIXB_LB[7:0] = 00h) SEL_VID_TABLEB = 0, Voltage of fixed VID mode = 0.245V + (VFIXB_HB [0] + VFIXB_LB[7:0]) x 5mV, (VID1), voltage range from 0.25V to 2.17V. SEL_VID_TABLEB = 1, Voltage of fixed VID mode = 0.19V + (VFIXB_HB [0] + VFIXB_LB[7:0]) x 10mV, (VID2), voltage range from 0.2V to 3.04V. Refer to Figure 35 for Control Logic.

Table 119. VFIXB_HB

Address: 0xAC
Description: 9-bit fixed VID (Reg. 0xAB + Reg. 0xAC). Set the voltage in fixed VID mode of rail B. In fixed VID mode, VR skips the SetVID/SetPS command. (VR has no actions but still asserts $\overline{\text{ALERT}}$ immediately after receiving the SetVID command, while the VR output voltage stays at the fixed VID.) While fixed VID is enabled, VR does not act for the I^2C voltage offset as well. After disabling fixed VID mode, VID returns to the last SetVID target and last power state. When entering/exiting fixed VID mode, VID slew rate is 1/2 of the fast slew rate.

Bit	7	6	5	4	3	2	1	0
Field	VFIXB_HB							
Default	0	0	0	0	0	0	0	0
Type	R							RW

Bit	Name	Description
7:0	VFIXB_HB	Voltage of fixed VID mode = 0.0V when receiving an off code (VFIXB_HB [0] = 00h + VFIXB_LB[7:0] = 00h) SEL_VID_TABLEB = 0, Voltage of fixed VID mode = 0.245V + (VFIXB_HB [0] + VFIXB_LB[7:0]) x 5mV, (VID1), voltage range from 0.25V to 2.17V. SEL_VID_TABLEB = 1, Voltage of fixed VID mode = 0.19V + (VFIXB_HB [0] + VFIXB_LB[7:0]) x 10mV, (VID2), voltage range from 0.2V to 3.04V. Refer to Figure 35 for Control Logic.

Table 120. VOFSB

Address: 0xAD
Description: Setting offset voltage of rail B. For VID1, the final voltage limiting range 0.25V to 2.17V. (For example, 0.25V ≤ VID setting ± SVID offset voltage ± I^2C offset voltage ≤ 2.17V) For VID2 the final voltage limiting range 0.2V to 3.04V. The offset slew rate is 1/2 of the fast slew rate. While setting the voltage offset, the VR should return to power state PS0. After VSEN settles at the target offset voltage, the power state (PS) goes back to the original PS. If CPU sends the SetPS1/2/3 command, the controller follows PS and the voltage offset still exists. If CPU sends the SetVID off code command (VID setting ± SVID offset voltage ± I^2C offset voltage), the controller sets output voltage to 0V.

Bit	7	6	5	4	3	2	1	0
Field	VOFSB							
Default	0	0	0	0	0	0	0	0
Type	RW							

Bit	Name	Description
7:0	VOFSB	[7:0] = 00h: No offset [7]: Sign bit (as part of two's complement) [6:0]: 5mV/step (SEL_VID_TABLEB = 1) or 10mV/step (SEL_VID_TABLEB = 1) For example, 0b00000001 = current VID + (1 x VID step) 0b00000011 = current VID + (3 x VID steps) 0b11111111 = current VID - (1 x VID step)

Table 121. TEMP_ALERTB and TEMP_VRHOTB

Address: 0xAE
Description: Setting rail B's ALERT temperature and thermal VRHOT temperature. The VRHOT temperature should be higher than the ALERT temperature. While the VRHOT temperature is smaller than the thermal ALERT temperature, VR will enforce that the ALERT temperature is smaller than the VRHOT temperature (TEMP_VRHOTB[7:4] = TEMP_ALERTB[3:0]).

Bit	7	6	5	4	3	2	1	0
Field	TEMP_ALERTB				TEMP_VRHOTB			
Default	0	1	1	0	0	1	1	0
Type	RW							

Bit	Name	Description
7:4	TEMP_ALERTB	Select thermal ALERT temperature of rail B. Temperature versus $V_{THERMAL}$ refer to Table 105. 0000: 75°C, 0001: 82°C, 0010: 85°C, 0011: 88°C, 0100: 91°C, 0101: 94°C, 0110: 97°C, 0111: 100°C, 1000: 103°C, 1001: 106°C, 1010: 109°C, 1011: 112°C, 1100: 115°C, 1101: 118°C, 1110: 121°C, 1111: 124°C
3:0	TEMP_VRHOTB	Select VRHOT temperature of rail B. Temperature versus $V_{THERMAL}$ refer to Table 105. 0000: 82°C, 0001: 85°C, 0010: 88°C, 0011: 91°C, 0100: 94°C, 0101: 97°C, 0110: 100°C, 0111: 103°C, 1000: 106°C, 1001: 109°C, 1010: 112°C, 1011: 115°C, 1100: 118°C, 1101: 121°C, 1110: 124°C, 1111: 127°C

Table 122. SUM_OCP_DEB_TIME B, EN_SS_OCPB, EN_SUM_OCPB, EN_NVB, EN_UVB, and EN_OVB

Address: 0xAF
Description: Enable protection function of rail B

Bit	7	6	5	4	3	2	1	0
Field	Reserved		SUM_OCP_DEB_TIME B	EN_SS_OCPB	EN_SUM_OCPB	EN_NVB	EN_UVB	EN_OVB
Default	0	0	--	--	1	1	1	1
Type	RW		RW	RW	RW	RW	RW	RW

Bit	Name	Description
7:6	Reserved	Unimplemented, the default value is 0b00
5	SUM_OCP_DEB_TIME B	0: 20μs, 1: 40μs The default value is from SEL_SUM_OCP_DEB_TIMEB (0x2B[6]) in the setting function table
4	EN_SS_OCPB	0: Disable soft-start OC protection 1: Enable soft-start OC protection The default value is from EN_SS_OCPB (0x2F[1]) in the setting function table.
3	EN_SUM_OCPB	0: Disable sum OC protection 1: Enable sum OC protection (default)
2	EN_NVB	0: Disable NV protection 1: Enable NV protection (default)
1	EN_UVB	0: Disable UV protection 1: Enable UV protection (default)
0	EN_OVB	0: Disable OV protection 1: Enable OV protection (default)

Table 123. OCB, NVB, UVB, and OVB

Address: 0xB0 **Description**: Protection indicator of rail B								
Bit	7	6	5	4	3	2	1	0
Field	Reserved				OCB	NVB	UVB	OVB
Default	0	0	0	0	0	0	0	0
Type	R				R	R	R	R

Bit	Name	Description
7:4	Reserved	Unimplemented, the default value is 0b0000
3	OCB	0: No occurrence of OCP 1: Occurrence of OCP
2	NVB	0: No occurrence of NVP 1: Occurrence of NVP
1	UVB	0: No occurrence UVP 1: Occurrence UVP
0	OVB	0: No occurrence of OVP 1: Occurrence of OVP

Table 124. ILOAD_RPTB

Address: 0xB1 **Description**: Output current reporting of rail B								
Bit	7	6	5	4	3	2	1	0
Field	ILOAD_RPTB							
Default	--	--	--	--	--	--	--	--
Type	R							

Bit	Name	Description
7:0	ILOAD_RPTB	Output current reporting

Table 125. TEMP_RPTB

Address: 0xB2 **Description**: Temperature reporting of rail B								
Bit	7	6	5	4	3	2	1	0
Field	TEMP_RPTB							
Default	--	--	--	--	--	--	--	--
Type	R							

Bit	Name	Description
7:0	TEMP_RPTB	$V_{THERMAL}$ = TEMP_RPTB x 6.25mV. Temperature versus $V_{THERMAL}$ refer to Table 108.

Table 126. VOFS_LOAD_HYSB and VOFS_LOAD_THB

Address: 0xB4 **Description**: Load condition for VID offset of rail B								
Bit	7	6	5	4	3	2	1	0
Field	VOFS_LOAD_HYSB		VOFS_LOAD_THB					
Default	0	0	0	0	0	0	0	0
Type	RW		RW					

Bit	Name	Description
7:6	VOFS_LOAD_HYSB	Select the current hysteresis 00: 4A, 01: 8A, 10: 12A, 11: 16A
5:0	VOFS_LOAD_THB	Set the current threshold from 0A to 126A with 2A/LSB

Table 127. ILOAD_RPT_RATIOB, FORCE_PS0B, and KTONB

Address: 0xB5 **Description**: Adjust output current reporting ratio, enable or disable force PS0 function and K_{TON} of rail B								
Bit	7	6	5	4	3	2	1	0
Field	ILOAD_RPT_RATIOB			FORCE_PS0B	Reserved	KTONB		
Default	0	0	0	0	0	--	--	--
Type	RW			RW	RW	RW		

Bit	Name	Description
7:5	ILOAD_RPT_RATIOB	Output current reporting ratio 000: 100%, 001: 95%, 010: 90%, 011: 85%, 100: 80%, 101: 75%, 110: 60%, 111: 50%
4	FORCE_PS0B	Enable this function, VR will stay at PS0 even though the SetPS PS1, PS2 or PS3 command is received. 0: Disable 1: Enable
3	Reserved	Unimplemented, the default value is 0
2:0	KTONB	On-time factor K_{TON}. Refer to the section Switching Frequency Setting for the details. Default value is from SEL_KTONB (0x15[2:0]) in the setting function table.

Table 128. EN_SPMB, EN_ANSB and SMALL_LLB

Address: 0xB6 **Description**: Enable acoustic noise suppression function and select small loadline of rail B								
Bit	7	6	5	4	3	2	1	0
Field	Reserved		EN_SPMB	EN_ANSB	SMALL_LLB			
Default	0	0	--	--	--	--	--	--
Type	RW		RW	RW	RW			

Bit	Name	Description
7:6	Reserved	Unimplemented, the default value is 0b00
5	EN_SPMB	Enable smart phase management function and the default value are from EN_SPM_DEFAULTB (0x23[7]) in the setting function table.
4	EN_ANSB	Enable acoustic noise suppression function. Bit field definition and the default value are from EN_ANSB (0x46[1]) in the setting function table.
3:0	SMALL_LLB	Small loadline. Bit field definition and the default value are from SEL_SMALL_LLB (0x18[7:4]) in the setting function table.

Table 129. VOFS_LOAD_OFSB

Address: 0xB8 **Description**: VID offset for load condition VOFS_LOADB (0xB4) of rail B								
Bit	7	6	5	4	3	2	1	0
Field	VOFS_LOAD_OFSB							
Default	0	0	0	0	0	0	0	0
Type	RW							

Bit	Name	Description
7:0	VOFS_LOAD_OFSB	Set the VID offset for load condition VOFS_LOADB (0xB4) [7:0] = 00h: No offset [7]: Sign bit (as part of two's complement) [6:0]: 5mV/step (SEL_VID_TABLEB = 0) or 10mV/step (SEL_VID_TABLEB = 1) For example, 0b00000001 = current VID + (1 x VID step) 0b00000011 = current VID + (3 x VID steps) 0b11111111 = current VID - (1 x VID step)

Table 130. LLB

Address: 0xB9 **Description**: Select loadline of rail B								
Bit	7	6	5	4	3	2	1	0
Field	Reserved			LLB				
Default	0	0	0	0	1	0	1	0
Type	RW			RW				

Bit	Name	Description
7:5	Reserved	Unimplemented, the default value is 0b000
4:0	LLB	Loadline setting. 1LSB = 10%. Range is from 0% to 200%. When LLB is above 15h, loadline will be 0%. For example, LLB = 0b01010, loadline = 100%, LLB = 0b10100, loadline = 200%, LLB = 0b10101, loadline = 0%

Table 131. LLC

Address: 0xBA **Description**: Select loadline of rail C								
Bit	7	6	5	4	3	2	1	0
Field	Reserved			LLC				
Default	0	0	0	0	1	0	1	0
Type	RW			RW				

Bit	Name	Description
7:5	Reserved	Unimplemented, the default value is 0b000
4:0	LLC	Loadline setting. 1LSB = 10%. Range is from 0% to 200%. When LLC is above 15h, loadline will be 0%. For example, LLC = 0b01010, loadline = 100%, LLC = 0b10100, loadline = 200%, LLC = 0b10101, loadline = 0%

Table 132. VFIXC_LB

Address: 0xBB
Description: 9-bit fixed VID (Reg. 0xBB + Reg. 0xBC). Set voltage in fixed VID mode of rail C. In fixed VID mode, VR skips the SetVID/SetPS command. (VR has no actions but still asserts ALERT immediately after receiving the SetVID command, while the VR output voltage stays at the fixed VID.) While fixed VID is enabled, VR does not act for the I^2C voltage offset as well. After disabling fixed VID mode, VID returns to the last SetVID target and last power state. When entering/exiting fixed VID mode, VID slew rate is 1/2 of the fast slew rate.

Bit	7	6	5	4	3	2	1	0
Field	VFIXC_LB							
Default (VID1)	1	0	0	0	0	0	1	1
Default (VID2)	1	0	1	0	0	0	0	1
Type	RW							

Bit	Name	Description
7:0	VFIXC_LB	Voltage of fixed VID mode = 0.0V when receiving an off code (VFIXC_HB [0] = 00h + VFIXC_LB[7:0] = 00h) SEL_VID_TABLEC = 0, Voltage of fixed VID mode = 0.245V + (VFIXC_HB [0] + VFIXC_LB[7:0]) x 5mV, (VID1), voltage range from 0.25V to 2.17V. SEL_VID_TABLEC = 1, Voltage of fixed VID mode = 0.19V + (VFIXC_HB [0] + VFIXC_LB[7:0]) x 10mV, (VID2), voltage range from 0.2V to 3.04V. Refer to Figure 35 for Control Logic.

Table 133. VFIXC_HB

Address: 0xBC
Description: 9-bit fixed VID (Reg. 0xBB + Reg. 0xBC). Set voltage in fixed VID mode of rail C. In fixed VID mode, VR skips the SetVID/SetPS command. (VR has no actions but still asserts ALERT immediately after receiving the SetVID command, while the VR output voltage stays at the fixed VID.) While fixed VID is enabled, VR does not act for the I^2C voltage offset as well. After disabling fixed VID mode, VID returns to the last SetVID target and last power state. When entering/exiting fixed VID mode, VID slew rate is 1/2 of the fast slew rate.

Bit	7	6	5	4	3	2	1	0
Field	VFIXC_HB							
Default	0	0	0	0	0	0	0	0
Type	RW							

Bit	Name	Description
7:0	VFIXC_HB	Voltage of fixed VID mode = 0.0V when receiving an off code (VFIXC_HB [0] = 00h + VFIXC_LB[7:0] = 00h) SEL_VID_TABLEC = 0, Voltage of fixed VID mode = 0.245V + (VFIXC_HB [0] + VFIXC_LB[7:0]) x 5mV, (VID1), voltage range from 0.25V to 2.17V. SEL_VID_TABLEC = 1, Voltage of fixed VID mode = 0.19V + (VFIXC_HB [0] + VFIXC_LB[7:0]) x 10mV, (VID2), voltage range from 0.2V to 3.04V. Refer to Figure 35 for Control Logic.

Table 134. VOFSC

Address: 0xBD
Description: Setting offset voltage of rail C. For VID1, the final voltage limiting is range from 0.25V to 2.17V. (For example, 0.25V ≤ VID setting ± SVID offset voltage ± I^2C offset voltage ≤ 2.17V) For VID2, the final voltage limiting is range from 0.2V to 3.04V. The offset slew rate is 1/2 of the fast slew rate. While setting voltage offset, the VR should return to the power state PS0. After VSEN settles at the target offset voltage, the power state (PS) goes back to the original PS. If CPU sends the SetPS1/2/3 command, the controller follows PS and the voltage offset still exists. If CPU sends the SetVID off code command (VID setting ± SVID offset voltage ± I^2C offset voltage), the controller sets the output voltage to 0V.

Bit	7	6	5	4	3	2	1	0
Field	VOFSC							
Default	0	0	0	0	0	0	0	0
Type	RW							

Bit	Name	Description
7:0	VOFSC	[7:0] = 00h: No offset [7]: Sign bit (as part of two's complement) [6:0]: 5mV/step (SEL_VID_TABLEC = 0) or 10mV/step (SEL_VID_TABLEC = 1) For example, 0b00000001 = current VID + (1 x VID step) 0b00000011 = current VID + (3 x VID steps) 0b11111111 = current VID - (1 x VID step)

Table 135. TEMP_ALERTC and TEMP_VRHOTC

Address: 0xBE
Description: Setting rail C's ALERT temperature and thermal VRHOT temperature. The VRHOT temperature should be higher than the ALERT temperature. While the VRHOT temperature is smaller than the thermal ALERT temperature, VR will enforce that the ALERT temperature is smaller than VRHOT temperature (TEMP_VRHOTC[7:4] = TEMP_ALERTC[3:0]).

Bit	7	6	5	4	3	2	1	0
Field	TEMP_ALERTC				TEMP_VRHOTC			
Default	0	1	1	0	0	1	1	0
Type	RW							

Bit	Name	Description
7:4	TEMP_ALERTC	Select thermal ALERT temperature of rail C. Temperature versus $V_{THERMAL}$ refer to Table 105. 0000: 75°C, 0001: 82°C, 0010: 85°C, 0011: 88°C, 0100: 91°C, 0101: 94°C, 0110: 97°C, 0111: 100°C, 1000: 103°C, 1001: 106°C, 1010: 109°C, 1011: 112°C, 1100: 115°C, 1101: 118°C, 1110: 121°C, 1111: 124°C
3:0	TEMP_VRHOTC	Select VRHOT temperature of rail C. Temperature versus $V_{THERMAL}$ refer to Table 105. 0000: 82°C, 0001: 85°C, 0010: 88°C, 0011: 91°C, 0100: 94°C, 0101: 97°C, 0110: 100°C, 0111: 103°C, 1000: 106°C, 1001: 109°C, 1010: 112°C, 1011: 115°C, 1100: 118°C, 1101: 121°C, 1110: 124°C, 1111: 127°C

Table 136. SUM_OCP_DEB_TIMEC, EN_SS_OCPC, EN_SUM_OCPC, EN_NVC, EN_UVC, and EN_OVC

Address: 0xBF
Description: Enable protection function of rail C

Bit	7	6	5	4	3	2	1	0
Field	Reserved		SUM_OCP_DEB_TIMEC	EN_SS_OCPC	EN_SUM_OCPC	EN_NVC	Reserved	EN_OVC
Default	0	0	--	--	1	1	1	1
Type	RW		RW	RW	RW	RW	RW	RW

Bit	Name	Description
7:6	Reserved	Unimplemented, the default value is 0b00
5	SUM_OCP_DEB_TIMEC	0: 20μs 1: 40μs The default value is from SEL_SUM_OCP_DEB_TIMEC (0x2C[7]) in the setting function table.
4	EN_SS_OCPC	0: Disable soft-start OC protection, 1: Enable soft-start OC protection The default value is from EN_SS_OCPC (0x2F[0]) in the setting function table.
3	EN_SUM_OCPC	0: Disable sum OC protection 1: Enable sum OC protection (default)
2	EN_NVC	0: Disable NV protection 1: Enable NV protection (default)
1	EN_UVC	0: Disable UV protection 1: Enable UV protection (default)
0	EN_OVC	0: Disable OV protection 1: Enable OV protection (default)

Table 137. OCC, NVC, UVC, and OVC

Address: 0xC0
Description: Protection indicator of rail C

Bit	7	6	5	4	3	2	1	0
Field	Reserved				OCC	NVC	UVC	OVC
Default	0	0	0	0	0	0	0	0
Type	R				R	R	R	R

Bit	Name	Description
7:4	Reserved	Unimplemented, the default value is 0b0000
3	OCC	0: No occurrence of OCP 1: Occurrence of OCP
2	NVC	0: No occurrence of NVP 1: Occurrence of NVP
1	UVC	0: No occurrence UVP 1: Occurrence UVP
0	OVC	0: No occurrence of OVP 1: Occurrence of OVP

Table 138. ILOAD_RPTC

Address: 0xC1 **Description**: Output current reporting of rail C								
Bit	7	6	5	4	3	2	1	0
Field	ILOAD_RPTC							
Default	--	--	--	--	--	--	---	--
Type	R							

Bit	Name	Description
7:0	ILOAD_RPTC	Output current reporting

Table 139. TEMP_RPTC

Address: 0xC2 **Description**: Temperature reporting of rail C								
Bit	7	6	5	4	3	2	1	0
Field	TEMP_RPTC							
Default	--	--	--	--	--	--	--	--
Type	RW							

Bit	Name	Description
7:0	TEMP_RPTC	$V_{THERMAL}$ = TEMP_RPTC x 6.25mV. For temperature versus $V_{THERMAL}$, refer to Table 108.

Table 140. VOFS_LOAD_HYSC and VOFS_LOAD_THC

Address: 0xC4 **Description**: Load condition for VID offset of rail C								
Bit	7	6	5	4	3	2	1	0
Field	VOFS_LOAD_HYSC		VOFS_LOAD_THC					
Default	1	0	0	0	0	0	0	0
Type	RW		RW					

Bit	Name	Description
7:6	VOFS_LOAD_HYSC	Select the current hysteresis 00: 4A, 01: 8A, 10: 12A, 11: 16A
5:0	VOFS_LOAD_THC	Set the current threshold from 0A to 126A with 2A/LSB

Table 141. ILOAD_RPT_RATIOC, FORCE_PS0C, and KTONC

Address: 0xC5
Description: Adjust output current reporting ratio, enable or disable to force the PS0 function and K_{TON} of rail C

Bit	7	6	5	4	3	2	1	0
Field	ILOAD_RPT_RATIOC			FORCE_PS0C	Reserved	KTONC		
Default	0	0	0	0	0	--	--	--
Type	RW			RW	RW	RW		

Bit	Name	Description
7:5	ILOAD_RPT_RATIOC	Output current reporting ratio 000: 100%, 001: 95%, 010: 90%, 011: 85%, 100: 80%, 101: 75%, 110: 60%, 111: 50%
4	FORCE_PS0C	Enable this function, VR will stay at PS0 even though the SetPS PS1, PS2 or PS3 command is received. 0: Disable, 1: Enable
3	Reserved	Unimplemented, the default value is 0
2:0	KTONC	On-time factor K_{TON}. Refer to the section Switching Frequency Setting for the details. Default value is from SEL_KTONC (0x16[6:4]) in setting function table

Table 142. EN_SPMC, EN_ANSC, and SMALL_LLC

Address: 0xC6
Description: Enable acoustic noise suppression function and select small loadline of rail C

Bit	7	6	5	4	3	2	1	0
Field	Reserved		EN_SPMC	EN_ANSC	SMALL_LLC			
Default	0	0	0	--	--	--	--	--
Type	RW		RW	RW	RW			

Bit	Name	Description
7:6	Reserved	Unimplemented, the default value is 0b00
5	EN_SPMC	Enable smart phase management and the default value are from EN_SPM_DEFAULTC (0x23[6]) in the setting function table.
4	EN_ANSC	Enable acoustic noise suppression function. Bit field definition and the default value are from EN_ANSC (0x46[0]) in the setting function table.
3:0	SMALL_LLC	Small loadline. Bit field definition and default value are from SEL_SMALL_LLC (0x18[3:0]) in setting function table

Table 143. ILOAD_RPT_RATIOD

Address: 0xC7 **Description**: Adjust the output current reporting ratio of rail D								
Bit	7	6	5	4	3	2	1	0
Field	ILOAD_RPT_RATIOD			Reserved				
Default	0	0	0	0	0	0	0	0
Type	RW			RW				

Bit	Name	Description
7:5	ILOAD_RPT_RATIOD	Output current reporting ratio 000: 100%, 001: 95%, 010: 90%, 011: 85%, 100: 80%, 101: 75%, 110: 60%, 111: 50%
4:0	Reserved	Unimplemented, the default value is 0b00000

Table 144. VOFS_LOAD_OFSC

Address: 0xC8 **Description**: VID offset for the load condition VOFS_LOADC (0xC4) of rail C								
Bit	7	6	5	4	3	2	1	0
Field	VOFS_LOAD_OFSC							
Default	0	0	0	0	0	0	0	0
Type	RW							

Bit	Name	Description
7:0	VOFS_LOAD_OFSC	Set the VID offset for the load condition VOFS_LOADC (0xC4) [7:0] = 00h: No offset [7]: Sign bit (as part of two's complement) [6:0]: 5mV/step (SEL_VID_TABLEC = 0) or 10mV/step (SEL_VID_TABLEC = 1) For example, 0b00000001 = current VID + (1 x VID step) 0b00000011 = current VID + (3 x VID steps) 0b11111111 = current VID - (1 x VID step)

Table 145. SEL_ANS, WD_STAT, EN_WD, and WDT

Address: 0xCC **Description**: Acoustic noise suppression behavior and the I²C watchdog related function								
Bit	7	6	5	4	3	2	1	0
Field	Reserved				SEL_ANS	WD_STAT	EN_WD	WDT
Default	0	0	0	0	--	--	--	--
Type	R				RW	R	RW	RW

Bit	Name	Description
7:4	Reserved	The default value is 0b0000
3	SEL_ANS	Acoustic noise suppression behavior. Bit definition and the default value are from SEL_ANS_BEHAV (0x1B[7]) in the setting function table
2	WD_STAT	I²C watchdog status 0: I²C transmission normal 1: I²C transmission abnormal, watch dog is triggered
1	EN_WD	Enable I²C watchdog 0: Disable watchdog. If the I²C bus hangs over 30ms, VR will reset the I²C state machine but keep the latest value of all registers. 1: Enable watchdog. If the I²C bus hangs over watchdog time (WDT, 0xCC[0]), VR will reset all the registers to the default value except the protection flag PROT_FLAGA, PROT_FLAGB, and PROT_FLAGC.
0	WDT	Watchdog time 0: 800ms, 1: 1600ms

Table 146. ILOAD_RPTD

Address: 0xCD **Description**: Output current reporting of rail D								
Bit	7	6	5	4	3	2	1	0
Field	ILOAD_RPTD							
Default	--	--	--	--	--	--	--	--
Type	R							

Bit	Name	Description
7:0	ILOAD_RPTD	Output current reporting

Table 147. RESTORE_FLAG, STORE_FLAG, STORE_ALLOW, RESTORE_BUSY, STORE_BUSY, CRC_NVM, and CRC_NVM_TOTAL

Address: 0xEC
Description: The NVM_PROGRAM_STATUS command returns one byte of information regarding the NVM program status

Bit	7	6	5	4	3	2	1	0
Field	RESTORE_FLAG	STORE_FLAG	STORE_ALLOW	RESTORE_BUSY	STORE_BUSY	CRC_NVM	Reserved	CRC_NVM_TOTAL
Default	--	--	--	--	--	--	--	--
Type	RW	RW	RW	RW	RW	RW	RW	RW

Bit	Name	Description
7	RESTORE_FLAG	Restore process done
6	STORE_FLAG	Store process done
5	STORE_ALLOW	Store process allowed
4	RESTORE_BUSY	NVM restore busy
3	STORE_BUSY	NVM store busy
2	CRC_NVM	NVM check fail
1	Reserved	Default value is 0
0	CRC_NVM_TOTAL	Total NVM check fail

Table 148. PAGE

Address: 0xEF
Description: The PAGE command provides the ability to configure, control, and monitor multiple PWM channels through setting registers and general registers.

Bit	7	6	5	4	3	2	1	0
Field	PAGE							
Default	1	0	0	0	0	0	0	0
Type	RW							

Bit	Name	Description
7:0	PAGE	[7:0] = 80h: Page X. General registers (default) [7:0] = 82h: Page 02. Setting registers All the other combinations are not defined.

Table 149. ENTER_CONFIG_MODE

Address: 0xF1 **Description:** Command to enter the user configuration mode.								
Bit	7	6	5	4	3	2	1	0
Field	ENTER_CONF_MODE							
Default	N/A							
Type	W							

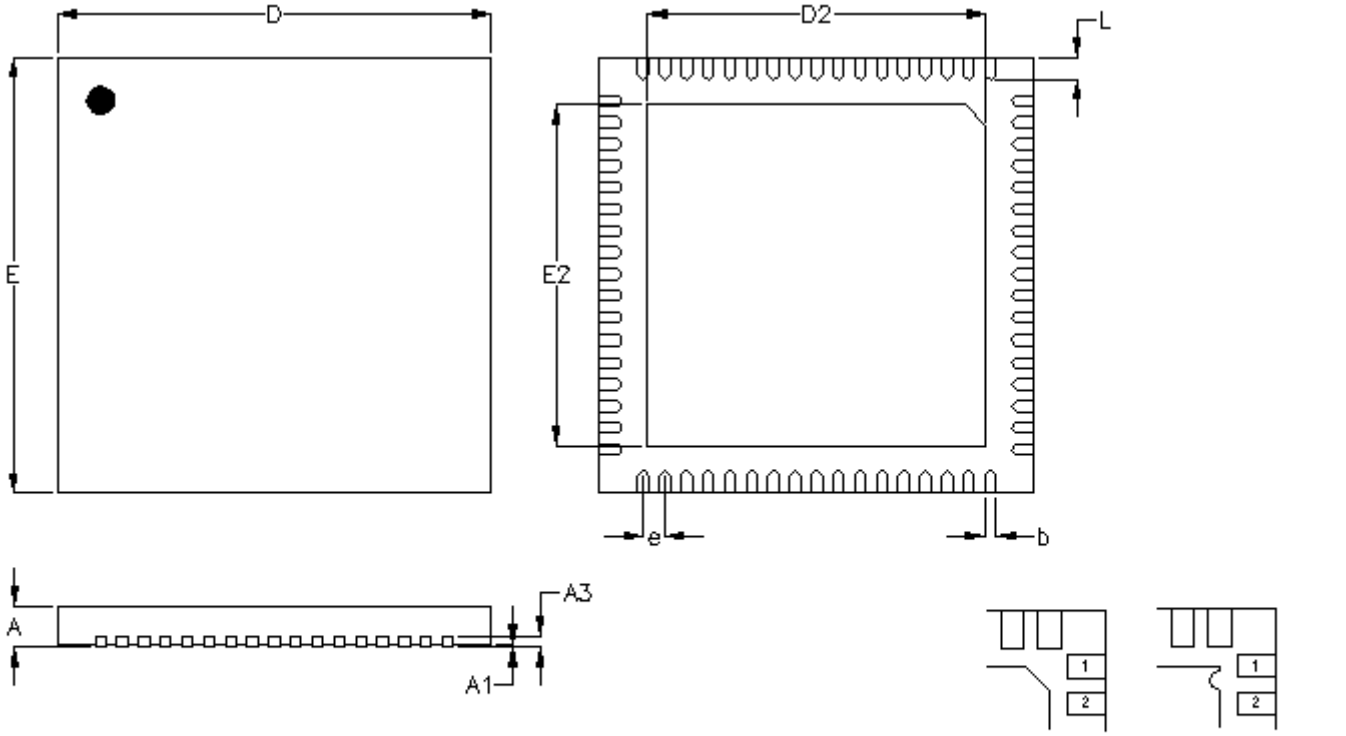
Bit	Name	Description
7:0	ENTER_CONF_MODE	0x62 is not available. Contact Richtek to receive the password required to access the user configuration mode.

Table 150. UNLOCK_NVM

Address: 0xFC **Description:** Unlock command for the NVM configuration settings.								
Bit	7	6	5	4	3	2	1	0
Field	UNLOCK_NVM							
Default	N/A							
Type	W							

Bit	Name	Description
7:0	UNLOCK_NVM	Unlock the NVM configuration settings. Contact Richtek to receive the unlock command for the NVM configuration setting.

20 Outline Dimension



DETAIL A

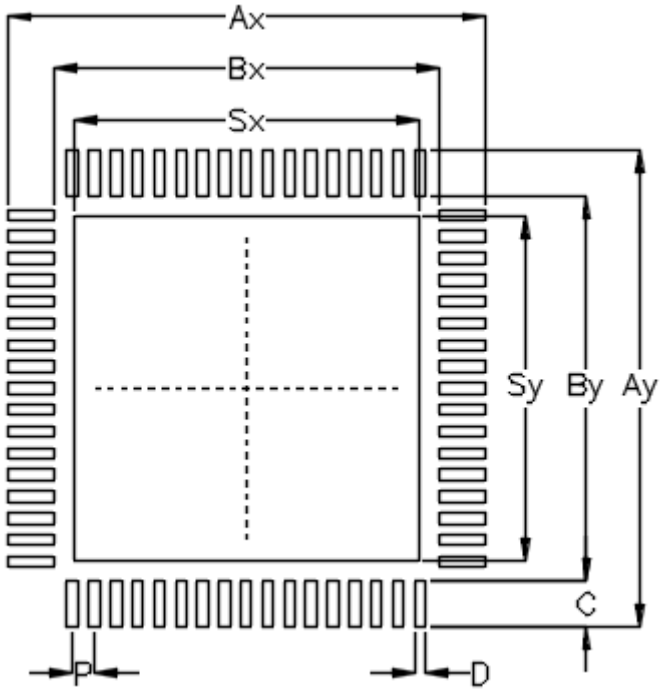
Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.150	0.250	0.006	0.010
D	7.900	8.100	0.311	0.319
D2	6.200	6.300	0.244	0.248
E	7.900	8.100	0.311	0.319
E2	6.200	6.300	0.244	0.248
e	0.400		0.016	
L	0.350	0.450	0.014	0.018

W-Type 68L QFN 8x8 Package

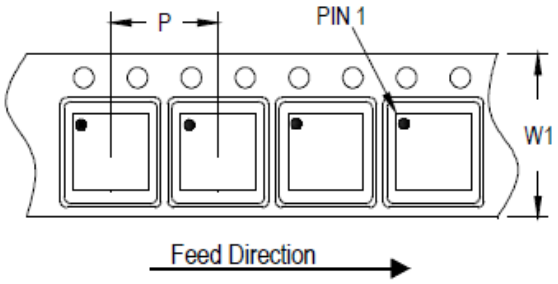
21 Footprint Information

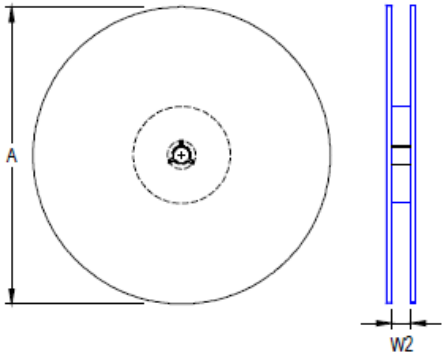


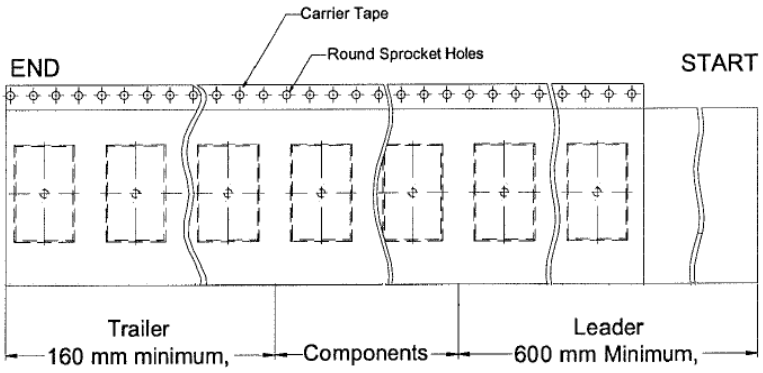
Package	Number of Pin	Footprint Dimension (mm)									Tolerance
		P	Ax	Ay	Bx	By	C	D	Sx	Sy	
V/W/U/XQFN8*8-68	68	0.40	8.80	8.80	7.10	7.10	0.85	0.20	6.35	6.35	±0.05

22 Packing Information

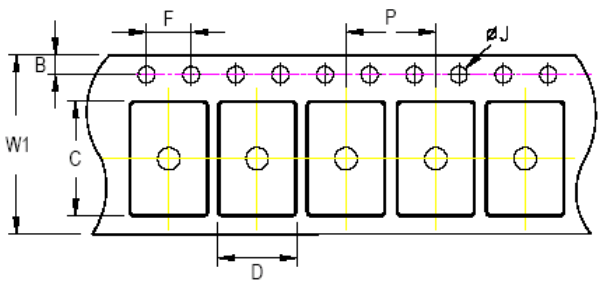
22.1 Tape and Reel Data







Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min./Max. (mm)
			(mm)	(in)				
QFN/DFN 8x8	16	12	330	13	2,500	160	600	16.4/18.4



C, D, and K are determined by component size. The clearance between the components and the cavity is as follows:

- For 16mm carrier tape: 1.0mm max.

Tape Size	W1	P		B		F		ØJ		H
	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Max.
16mm	16.3mm	11.9mm	12.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	0.6mm

22.2 Tape and Reel Packing

Step	Photo/Description	Step	Photo/Description
1	 Reel 13”	4	 1 reel per inner box **Box G**
2	 HIC & Desiccant (2 Unit) inside	5	 6 inner boxes per outer box
3	 Caution label is on backside of Al bag	6	 Outer box **Carton A**

Container / Package	Reel		Box			Carton		
	Size	Units	Item	Reels	Units	Item	Boxes	Units
QFN and DFN 8x8	13”	2,500	Box G	1	2,500	Carton A	6	15,000

22.3 Packing Material Anti-ESD Property

Surface Resistance	Aluminum Bag	Reel	Cover tape	Carrier tape	Tube	Protection Band
Ω/cm^2	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**

Richtek Technology Corporation
14F, No. 8, Tai Yuen 1st Street, Chupei City
Hsinchu, Taiwan, R.O.C.
Tel: (8863)5526789

23 Datasheet Revision History

Version	Date	Description	Item
00	2024/5/24	Final	Application Information on P26, P28, P29, P35, P36, P40, P49