RICHTEK®

RT2872

3A, 36V, Synchronous Step-Down Converter

1 General Description

The RT2872 is a high-efficiency, current-mode synchronous step-down converter that can deliver up to 3A output current over a wide input voltage range from 4.5 V to 36 V. The device integrates 105mΩ high-side and 80mΩ low-side MOSFETs to achieve high conversion efficiency. The current-mode control architecture supports fast transient response and simple external compensation. The cycle-by-cycle current limit provides protection against shorted outputs, and soft-start eliminates input current surges during start-up.

The RT2872 provides comprehensive protection functions such as input undervoltage-lockout, output undervoltage protection, overcurrent protection, and over-temperature protection.

The RT2872 is available in a thermal enhanced SOP-8 (Exposed Pad) package. The recommended junction temperature range is –40°C to 125°C, and the ambient temperature range is –40°C to 85°C.

2 Ordering Information

RT2872 □□

Package Type(1)
SP: SOP-8 (Exposed Pad)
(Exposed Pad-Option 2)

Lead Plating System
G: Richtek Green Policy Compliant(2)

Note 1.

- Marked with (1) indicated: Compatible with the current requirements of IPC/JEDEC J-STD-020.
- Marked with (2) indicated: Richtek products are Richtek Green Policy compliant.

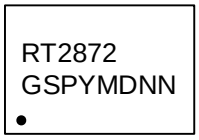
3 Features

- **4.5V to 36V Input Voltage Range**
- **3A Output Current**
- **Internal N-MOSFETs**
- **Current Mode Control**
- **Frequency Operation: 300kHz to 1MHz**
- **Adjustable Output Voltage from 0.8V to 30V**
- **High Efficiency Up to 95%**
- **Stable with Low ESR Ceramic Output Capacitors**
- **Cycle-by-Cycle Current-Limit Protection**
- **Input Undervoltage-Lockout**
- **Output Undervoltage Protection**
- **Over-Temperature Protection**
- **AEC-Q100 Grade 3 Certification**

4 Applications

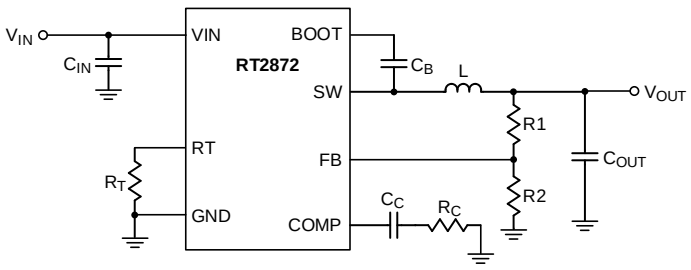
- Point of Load Regulator in Distributed Power Systems
- Digital Set Top Boxes
- Broadband Communications
- Vehicle Electronics
- Automotive Audio, Navigation, and Information Systems
- Enterprise Datacom Platforms Point of Load (POL)
- Industrial Grade General Purpose Point of Load

5 Marking Information



RT2872: Product Code
YMDNN: Date Code

6 Simplified Application Circuit



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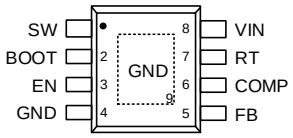
7 Pin Configuration

(TOP VIEW)



SOP-8 (Exposed Pad)

8 Functional Pin Description

Pin No.	Pin Name	Pin Function
1	SW	Switch node. Connect to the power inductor. Return path for the internal high-side MOSFET gate driver bootstrap capacitor. Connect a capacitor from BOOT to this pin.
2	BOOT	Bootstrap supply for the high-side gate driver. Connect a 10nF ceramic capacitor between the BOOT and SW pins.
3	EN	Enable Input. A logic high enables the converter, while a logic low forces the converter into shutdown mode.
4, 9 (Exposed Pad)	GND	Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.
5	FB	Feedback input. The pin is used to set the output voltage of the converter via a resistor divider. Suggest to place the FB resistor divider as close to the FB pin and GND as possible.
6	COMP	Compensation Node. This pin is used for compensating the regulation control loop. A series RC network is required to be connected from COMP to GND. If needed, an additional capacitor should be connected from COMP to GND.
7	RT	Switching Frequency Setting. Connect an external resistor to set the switching frequency from 300kHz to 1MHz.
8	VIN	Input voltage. Support 4.5V to 36V input voltage. Suggest to place equal-value input capacitors on each side of the IC and as close to the VIN and GND pins as possible.

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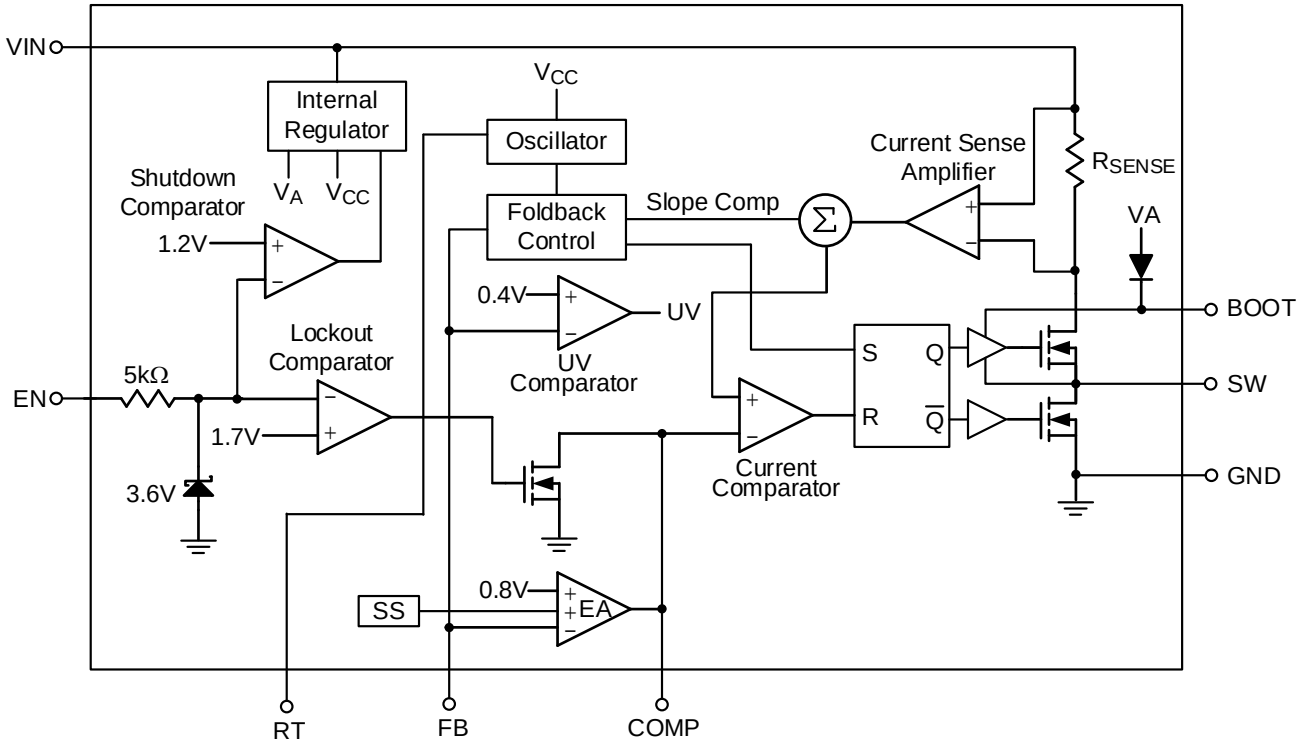
9 Functional Block Diagram



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10 Absolute Maximum Ratings

(Note 2)

- Supply Voltage, VIN ---------- –0.3V to 40V
- Switch Voltage, SW ---------- –0.3V to (V_{IN} + 0.3V)
- BOOT Pin ---------- –0.3V to 46.3V
- EN Pin (with REN (150kΩ to 600kΩ) to VIN) ---------- –0.3V to 40V
- SW Voltage (t < 10ns) ---------- –5V to 46.3V
- EN Pin ---------- –0.3V to 3.6V
- Other Pins ---------- –0.3 to 6V
- Power Dissipation, P_D @ T_A = 25°C

  SOP-8 (Exposed Pad) ---------- 2.041W
- Package Thermal Resistance (Note 3)

  SOP-8 (Exposed Pad), θ_{JA} ---------- 49°C/W

  SOP-8 (Exposed Pad), θ_{JC} ---------- 8°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 4)

  HBM ---------- 2kV

Note 2. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 3. θ_{JA} is simulated at T_A = 25°C on a high effective thermal conductivity four-layer test board per JEDEC 51-7. θ_{JC} is measured at the exposed pad of the package. The PCB copper area with exposed pad is 70mm^2.

Note 4. Devices are ESD sensitive. Handling precautions are recommended.

11 Recommended Operating Conditions

(Note 5)

- Supply Input Voltage, VIN ---------- 4.5V to 36V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Note 5. The device is not guaranteed to function outside its operating conditions.

12 Electrical Characteristics

(V_{IN} = 12V, C_{IN} = 20μF, T_A = –40°C to 85°C, unless otherwise specified.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Shutdown Current	I_{SHDN}	V_{EN} = 0V	--	--	10	μA
Quiescent Current	I_Q	V_{EN} = 3V, V_{FB} = 0.9V	--	1	1.3	mA
Feedback Voltage	V_{FB}	4.5V ≤ V_{IN} ≤ 36V	0.784	0.8	0.816	V
On-Resistance of High-Side MOSFET	R_{DSON_H}		--	105	190	mΩ

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Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
On-Resistance of Low-Side MOSFET	R_{DSON_L}		--	80	145	mΩ
High-Side Switch Current Limit	I_{LIM_H}		4.25	5	5.75	A
Low-Side Switch Current Limit	I_{LIM_L}	From Drain to Source	--	1.7	--	A
Oscillation Frequency	f_{OSC1}	R_T = 191kΩ	264	300	336	kHz
		R_T = 113kΩ	440	500	560	
		R_T = 51kΩ	880	1000	1120	
Short-Circuit Oscillation Frequency	f_{OSC2}	V_{FB} = 0V, R_T = 113kΩ	--	50	--	kHz
Maximum Duty Cycle	D_{MAX}	V_{FB} = 0.7V	--	95	--	%
Minimum On-Time	t_{ON}		--	100	120	ns
EN Input Voltage Rising Threshold	V_{EN_R}		2	--	3.3	V
EN Input Voltage Falling Threshold	V_{EN_F}		--	--	0.4	V
Undervoltage-Lockout Rising Threshold	V_{UVLO_R}	V_{IN} Rising	3.7	4.2	4.5	V
Undervoltage-Lockout Hysteresis	V_{UVLO_HYS}		--	250	--	mV
Over-Temperature Protection Threshold	T_{OTP}		--	150	--	°C
Over-Temperature Protection Hysteresis	T_{OTP_HYS}		--	25	--	°C
COMP to Current Sense Trans-conductance	G_{CS}	ΔI_{COMP} = ±10μA	--	4.1	--	A/V
Error Amplifier Trans-conductance	G_{EA}		--	950	--	μA/V

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14 Typical Application Circuit

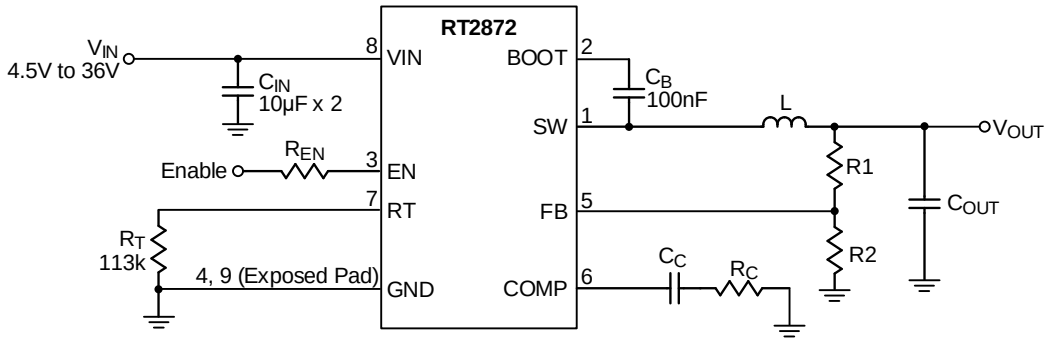

Table 1. Suggested Component Values

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	R_C (kΩ)	L (µH)	C_C (nF)	C_{OUT} (µF)
12	47	3.35	47	10	2.7	22 x 2
8	27	3	36	8.2	2.7	22 x 2
5	62	11.8	24	6.8	2.7	22 x 2
3.3	75	24	16	4.7	2.7	22 x 2
2.5	25.5	12	12	3.6	2.7	22 x 2
1.2	30	60	6.8	2.2	2.7	22 x 2

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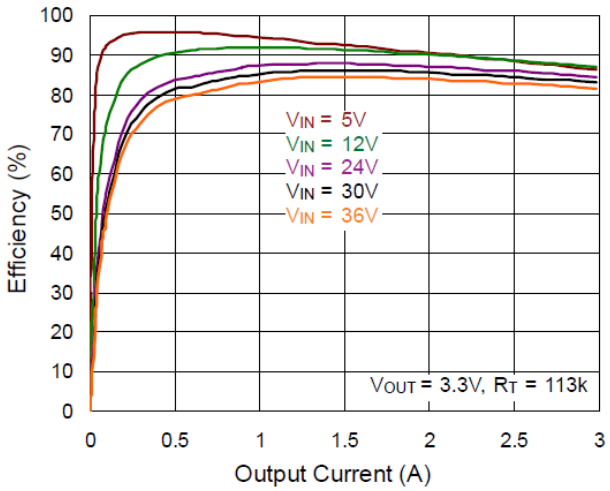
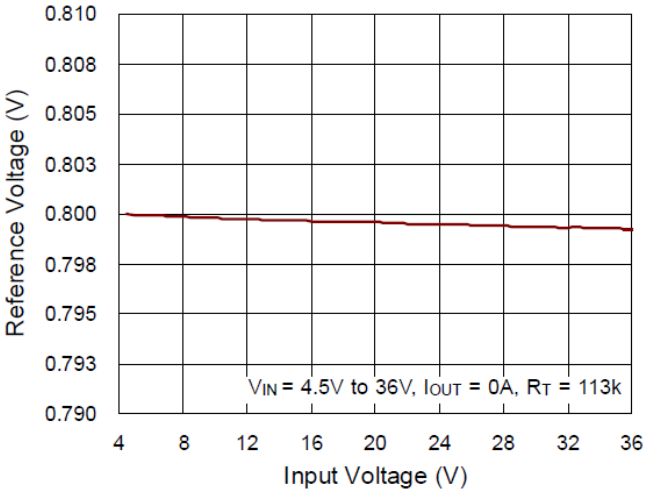
15 Typical Operating Characteristics

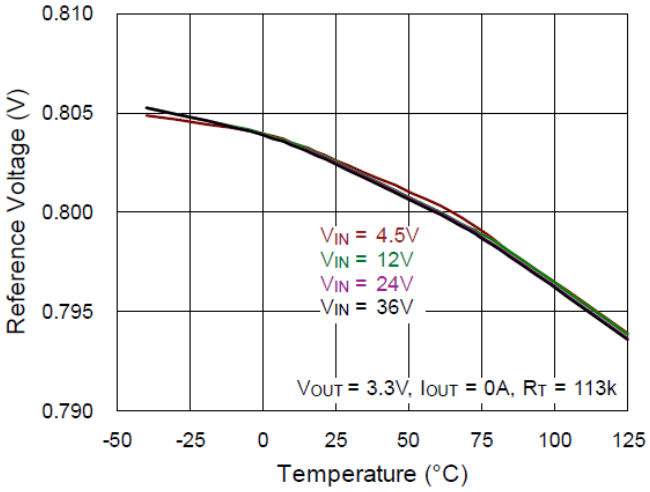
Efficiency vs. Output Current



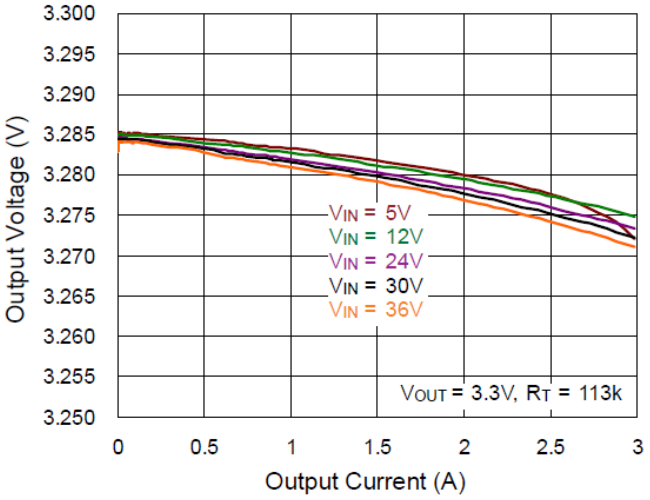
Reference Voltage vs. Input Voltage



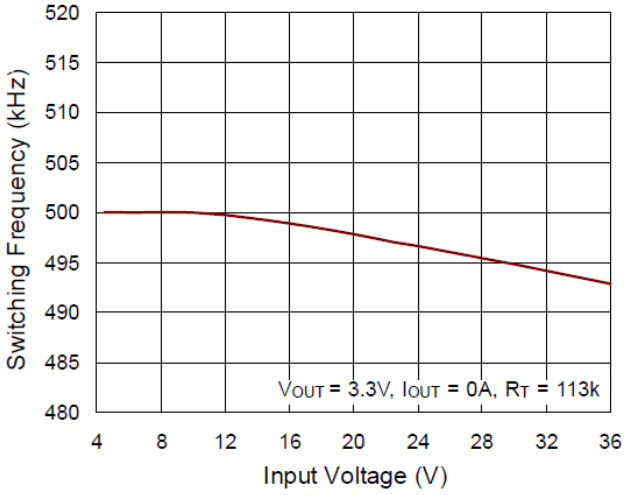
Reference vs. Temperature



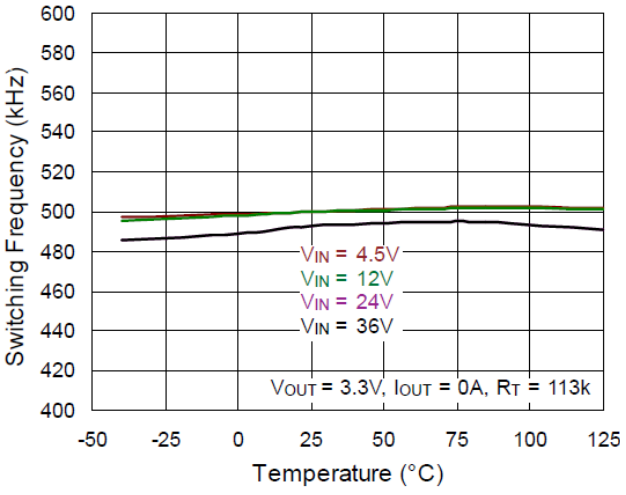
Output Voltage vs. Output Current



Switching Frequency vs. Input Voltage



Switching Frequency vs. Temperature



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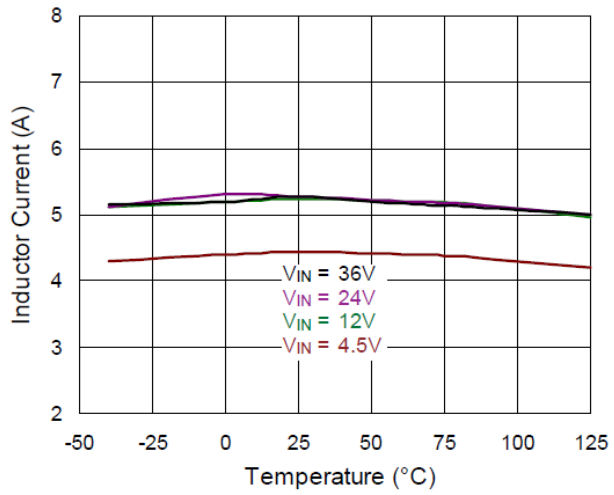
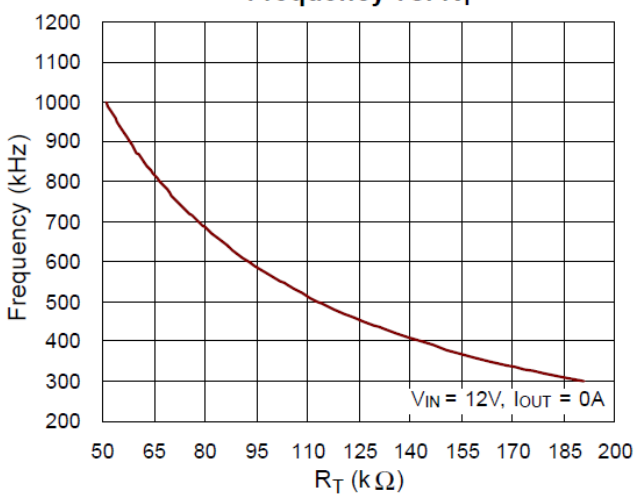
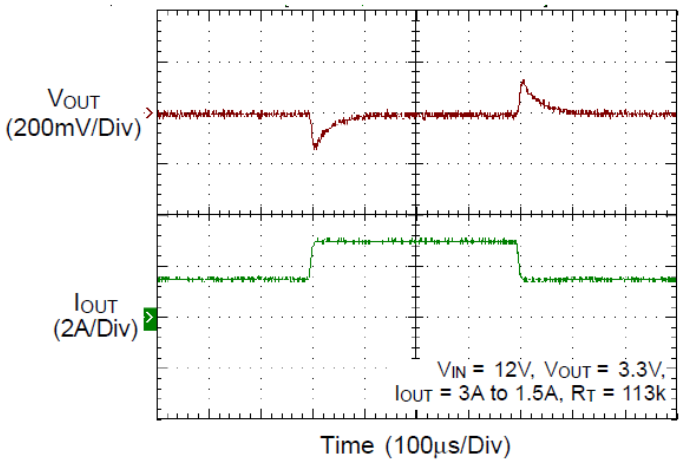
Current Limit vs. Temperature



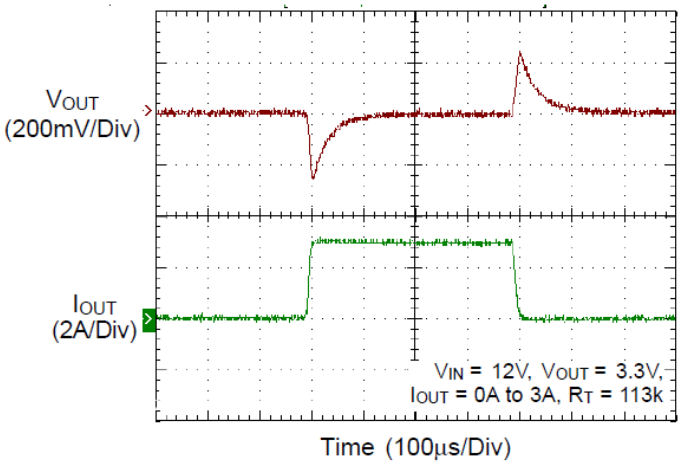
Frequency vs. R_T



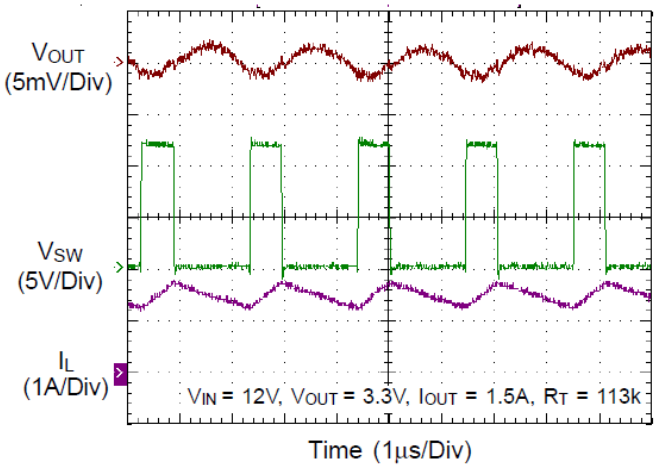
Load Transient Response



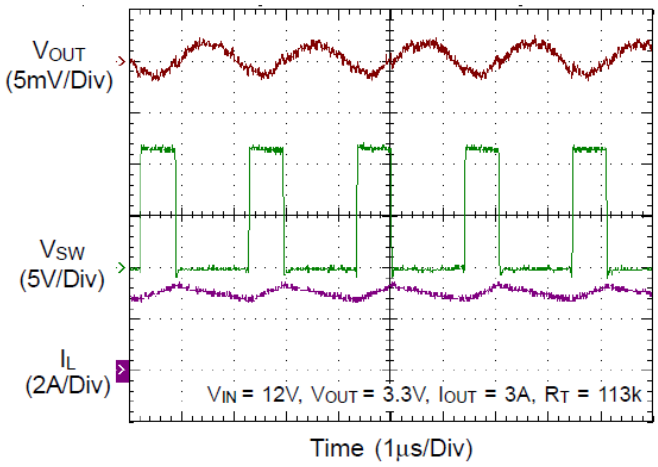
Load Transient Response



Switching



Switching



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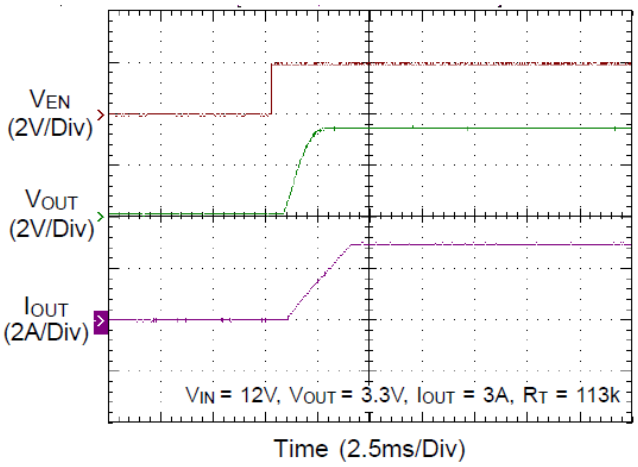
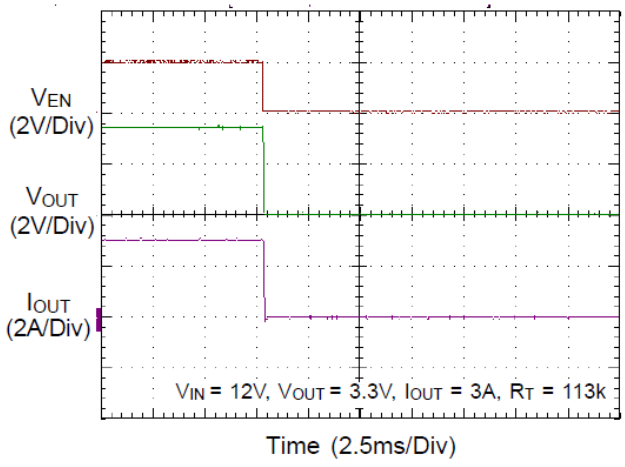
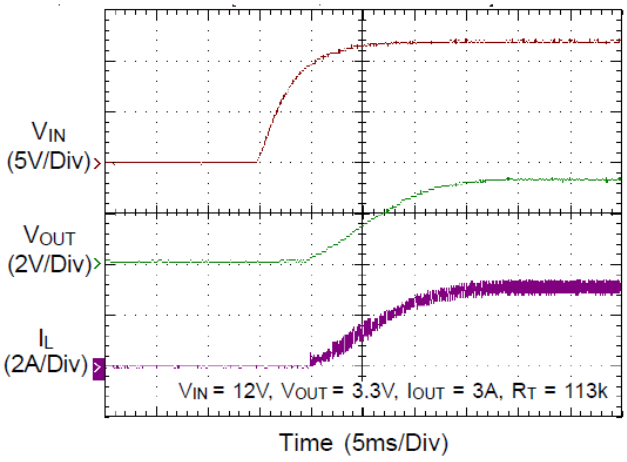
Power On from EN



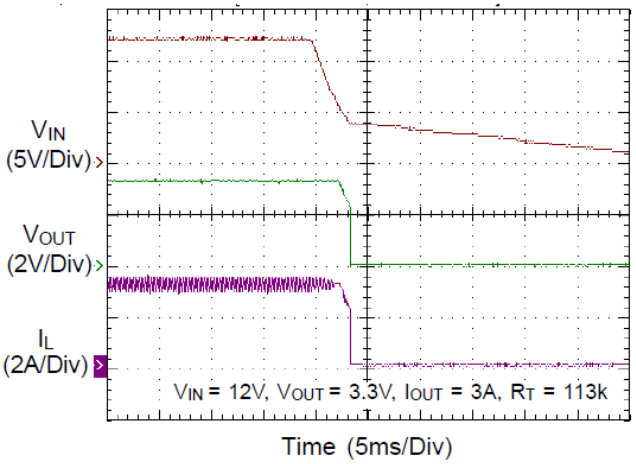
Power Off from EN



Power On from VIN



Power Off from VIN



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16 Operations

The RT2872 is a constant frequency, current-mode synchronous step-down converter. In normal operation, the high-side N-MOSFET is turned on when the S-R latch is set by the oscillator and is turned off when the current comparator resets the S-R latch. While the high-side N-MOSFET is turned off, the low-side N-MOSFET is turned on to conduct the inductor current until the next cycle begins.

16.1 Error Amplifier

The error amplifier adjusts its output voltage by comparing the feedback signal (V_{FB}) with the internal 0.8V reference. When the load current increases, it causes a drop in the feedback voltage relative to the reference, and then the error amplifier's output voltage rises to allow higher inductor current to match the load current.

16.2 Oscillator

The oscillator frequency can be set by using an external resistor R_T. The oscillator frequency range is from 300kHz to 1MHz.

$$\frac{1000}{\frac{1000}{f_S(kHz)} - 0.22} = \frac{66876}{R_T(kW)} - 29.405$$

16.3 Internal Regulator

The regulator provides low voltage power to supply the internal control circuits and the bootstrap power for the high-side gate driver.

16.4 Enable

The converter is turned on when the EN pin is higher than 2V. When the EN pin is lower than 0.4V, the converter will enter shutdown mode and reduce the supply current to 0.5μA.

16.5 Soft-Start Function

An internal current source charges an internal capacitor to build a soft-start (SS) ramp voltage. The FB voltage will track the internal ramp voltage during the soft-start interval. The typical soft-start time is 2ms.

16.6 UV Comparator

If the feedback voltage is lower than 0.4V, the UV Comparator will go high to turn off the high-side MOSFET. The output undervoltage protection is designed to operate in hiccup mode. When the UV condition is removed, the converter will resume switching.

16.7 Over-Temperature Protection

The over-temperature protection function will shut down the switching operation when the junction temperature exceeds 150°C. Once the junction temperature cools down by approximately 20°C, the converter will automatically resume switching.

16.8 Undervoltage-Lockout (UVLO)

The RT2872 implements Undervoltage-Lockout (UVLO) protection to prevent operation without sufficient supply voltage.

When the input voltage of the RT2872 ramps up over 4.5V (V_{UVLO_R} max) during power-up, the RT2872 will begin switching properly and provide V_{OUT}.

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After the device is powered up, if the input voltage V_{IN} goes below the UVLO falling threshold voltage of 4.25V ($V_{UVLO\_R} - V_{UVLO\_HYS}$), switching will be inhibited. If V_{IN} rises above the UVLO rising threshold (V_{UVLO_R}), the device will resume normal operation with a complete soft-start.

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17 Application Information

(Note 6)

17.1 Output Voltage Setting

The resistive divider allows the FB pin to sense the output voltage, as shown in Figure 1.

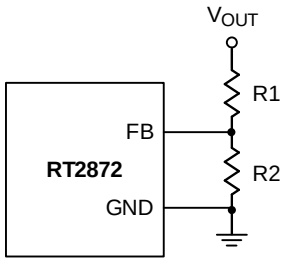

Figure 1. Output Voltage Setting

The output voltage is set by an external resistive divider according to the following equation:

$$V_{OUT} = V_{FB}(1+\frac{R1}{R2})$$

where V_{FB} is the feedback voltage (typically 0.8V).

17.2 External Bootstrap Diode

Connect a 0.1μF low ESR ceramic capacitor between the BOOT pin and the SW pin. This capacitor provides the gate driver voltage for the high-side MOSFET. It is recommended to add an external bootstrap diode between an external 5V supply and the BOOT pin for efficiency improvement when the input voltage is lower than 5.5V, or the duty ratio is higher than 65%. The bootstrap diode can be a low-cost option such as 1N4148 or BAT54. The external 5V can be a 5V fixed input from the system or a 5V output of the RT2872. Note that the external boot voltage must be lower than 5.5 V.

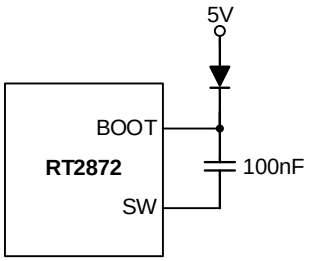

Figure 2. External Bootstrap Diode

17.3 Chip Enable Operation

The EN pin is the chip enable input. Pulling the EN pin low (<0.4V) will shut down the device. During shutdown mode, the RT2872 quiescent current drops to lower than 3μA. Driving the EN pin high (>2.5V, <3.3V) will turn on the device again. For external timing control, the EN pin can also be externally pulled high by adding a R_{EN} resistor and a C_{EN} capacitor from the V_{IN} pin (see Figure 3).

R_{EN} must be chosen between 150kΩ and 600kΩ to avoid a large leak current into the chip.

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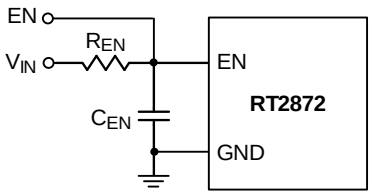

Figure 3. Enable Timing Control

An external MOSFET can be added to implement digital control on the EN pin when no system voltage above 2.5V is available, as shown in Figure 4. In this case, a 300kΩ pull-up resistor, R_{EN}, is connected between V_{IN} and the EN pin. MOSFET Q1 will be under logic control to pull down the EN pin.

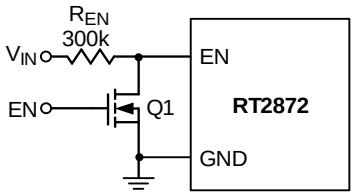

Figure 4. Digital Enable Control Circuit

17.4 Undervoltage Protection

The RT2872 provides Hiccup Mode Undervoltage Protection (UVP). When the V_{FB} voltage drops below 0.4V, the UVP function will be triggered to shut down the switching operation. If the UVP condition remains for a period, the RT2872 will retry automatically. When the UVP condition is removed, the converter will resume operation. The UVP is disabled during the soft-start period.

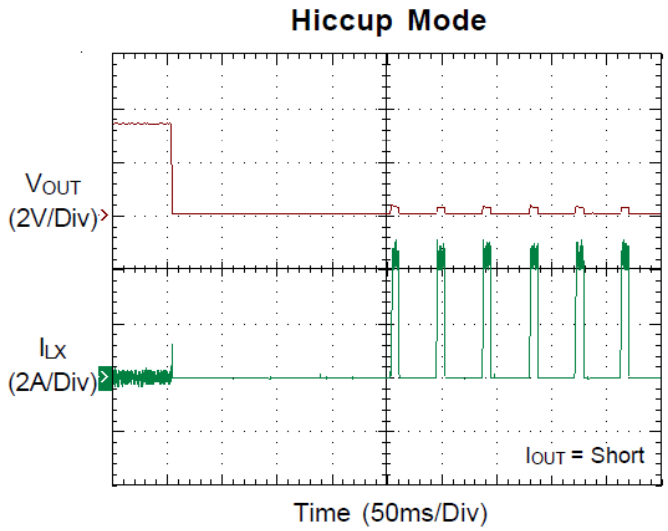

Figure 5. Hiccup Mode Undervoltage Protection

17.5 Over-Temperature Protection

The RT2872 features an Over-Temperature Protection (OTP) circuitry to prevent overheating due to excessive power dissipation. The OTP will shut down the switching operation when the junction temperature exceeds 150°C. Once the junction temperature cools down by approximately 20°C, the converter will resume operation. To maintain continuous operation, the maximum junction temperature should be lower than 125°C.

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17.6 Inductor Selection

The inductor value and operating frequency determine the ripple current according to specific input and output voltages. The ripple current (ΔI_L) increases with higher VIN and decreases with higher inductance.

$$\Delta I_L = [\frac{V_{OUT}}{f \times L}] \times [1-\frac{V_{OUT}}{V_{IN}}]$$

Having a lower ripple current reduces not only the ESR losses in the output capacitors but also the output voltage ripple. High frequency with small ripple current can achieve the highest efficiency operation. However, it requires a large inductor to achieve this goal. For ripple current selection, a value of ΔI_L = 0.24 × I_{MAX} is a reasonable starting point. The largest ripple current occurs at the highest VIN. To guarantee that the ripple current stays below the specified maximum, the inductor value should be chosen according to the following equation:

$$L = [\frac{V_{OUT}}{f \times \Delta I_{L(MAX)}}] \times [1-\frac{V_{OUT}}{V_{IN(MAX)}}]$$

The inductor's current rating (causing a 40°C temperature rise from a 25°C ambient) should be greater than the maximum load current, and its saturation current should be greater than the short circuit peak current limit. See Table 2 for the suggested inductors selection.

Table 2. Suggested Inductors for Typical Application Circuit

Component Supplier	Series	Dimensions (mm)
TDK	VLF10045	10 x 9.7 x 4.5
TDK	SLF12565	12.5 x 12.5 x 6.5
TAIYO YUDEN	NR8040	8 x 8 x 4

17.7 C_{IN} and C_{OUT} Selection

The input capacitance, C_{IN}, is needed to filter the trapezoidal current at the source of the high-side MOSFET. To prevent large ripple current, a low ESR input capacitor sized for the maximum RMS current should be used. The RMS current is given by:

$$I_{RMS} = I_{OUT(MAX)} \times \frac{V_{OUT}}{V_{IN}} \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Choose a capacitor with a higher temperature rating than required. Several capacitors may also be paralleled to meet size or height requirements in the design. For the input capacitor, a 10µF x 2 low ESR ceramic capacitor is recommended. For the recommended capacitor, refer to Table 3 for more details. The selection of C_{OUT} is determined by the required ESR to minimize voltage ripple. Moreover, the amount of bulk capacitance is also key for C_{OUT} selection to ensure that the control loop is stable. Loop stability can be checked by viewing the load transient response, as described in a later section. The output ripple, ΔV_{OUT}, is determined by:

$$\Delta V_{OUT} \leq \Delta I_L \times [ESR + \frac{1}{8 \times f \times C_{OUT}}]$$

The output ripple will be highest at the maximum input voltage since ΔI_L increases with input voltage. Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirements. Dry

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tantalum, special polymer, aluminum electrolytic, and ceramic capacitors are all available in surface mount packages. Special polymer capacitors offer very low ESR values. However, they provide lower capacitance density than other types. Although tantalum capacitors have the highest capacitance density, it is important to only use types that pass the surge test for use in switching power supplies. Aluminum electrolytic capacitors have significantly higher ESR. However, they can be used in cost-sensitive applications for ripple current rating and long-term reliability considerations. Ceramic capacitors have excellent low ESR characteristics but can have a high voltage coefficient and audible piezoelectric effects. The high Q of ceramic capacitors, combined with trace inductance, can also lead to significant ringing.

Higher value, lower cost ceramic capacitors are now becoming available in smaller case sizes. Their high ripple current, high voltage rating, and low ESR make them ideal for switching regulator applications. However, care must be taken when these capacitors are used at the input and output. When a ceramic capacitor is used at the input and the power is supplied by a wall adapter through long wires, a load step at the output can induce ringing at the input, V_{IN}. At best, this ringing can couple to the output and be mistaken for loop instability. At worst, a sudden inrush of current through the long wires can potentially cause a voltage spike at V_{IN} large enough to damage the part.

Table 3. Suggested Capacitors for C_{IN} and C_{OUT}

Location	Component Supplier	Part No.	Capacitance (μF)	Case Size
C_{IN}	MURATA	GRM32ER71H475K	4.7	1206
C_{IN}	TAIYO YUDEN	UMK325BJ475MM-T	4.7	1206
C_{IN}	MURATA	GRM31CR61E106K	10	1206
C_{IN}	TDK	C3225X5R1E106K	10	1206
C_{IN}	TAIYO YUDEN	TMK316BJ106ML	10	1206
C_{OUT}	MURATA	GRM31CR60J476M	47	1206
C_{OUT}	TDK	C3225X5R0J476M	47	1210
C_{OUT}	MURATA	GRM32ER71C226M	22	1210
C_{OUT}	TDK	C3225X5R1C22M	22	1210

17.8 Switching Frequency Setting

The switching frequency can be set by using an external resistor R_T. The switching frequency range is from 300 kHz to 1 MHz. By connecting the external resistor R_T to the RT pin, the switching frequency f_S can be set. The approximate formula is provided below:

$$\frac{1000}{\frac{1000}{f_S(kHz)} - 0.22} = \frac{66876}{R_T(k\Omega)} - 29.405$$

17.9 Thermal Considerations

For continuous operation, do not exceed the absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and the difference between junction and ambient temperature. The maximum power dissipation can be calculated using the following formula:

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For recommended operating condition specifications, the maximum junction temperature is 125°C. The junction-

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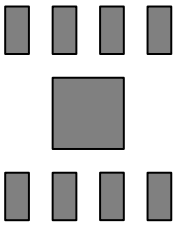
to-ambient thermal resistance, θ_{JA}, is layout dependent. For the SOP-8 (Exposed Pad), the thermal resistance, θ_{JA}, is 75°C/W on a standard JEDEC 51-7 four-layer thermal test board. The maximum power dissipation at T_A = 25°C can be calculated using the following formula:

$P_{D(MAX)}$ = (125°C − 25°C)/(75°C/W) = 1.333W (minimum copper area PCB layout)

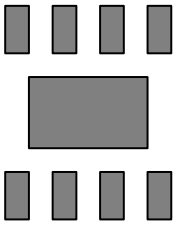
$P_{D(MAX)}$ = (125°C − 25°C)/(49°C/W) = 2.04W (70mm^2 copper area PCB layout)

The thermal resistance θ_{JA} of the SOP-8 (Exposed Pad) package is determined by the package architecture design and the PCB layout design. While the package architecture design is fixed, thermal performance can be enhanced through PCB layout copper design. The thermal resistance θ_{JA} can be decreased by adding copper area under the exposed pad of the SOP-8 (Exposed Pad) package.

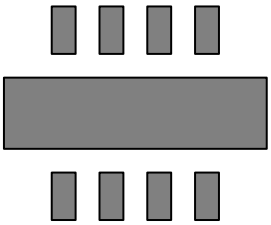
As shown in Figure 6, the amount of copper area to which the SOP-8 (Exposed Pad) is mounted affects thermal performance. When mounted to the standard SOP-8 (Exposed Pad) pad (Figure 6 (a)), θ_{JA} is 75°C/W. Adding copper area under the SOP-8 (Exposed Pad) (Figure 6 (b)) reduces θ_{JA} to 64°C/W. Further increasing the copper area of the pad to 70 mm^2 (Figure 6 (e)) reduces θ_{JA} to 49°C/W.



(a) Copper Area = (2.3 x 2.3) mm^2, θ_{JA} = 75°C/W



(b) Copper Area = 10mm^2, θ_{JA} = 64°C/W



(c) Copper Area = 30mm^2, θ_{JA} = 54°C/W

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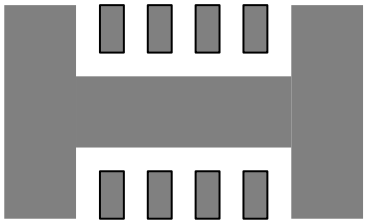
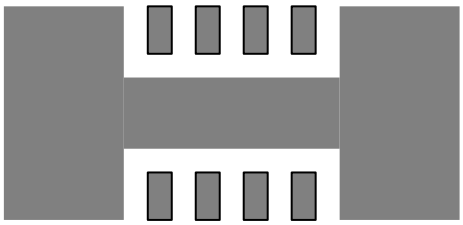


(d) Copper Area = 50mm^2, θ_{JA} = 51°C/W



(e) Copper Area = 70mm^2, θ_{JA} = 49°C/W

Figure 6. Thermal Resistance vs. Copper Area Layout Design

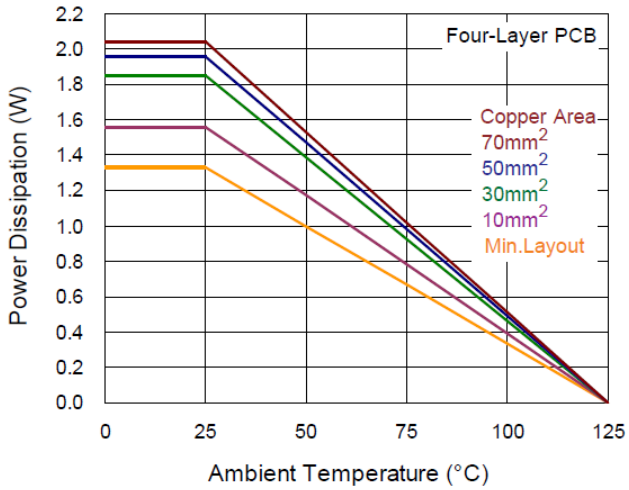


Figure 7. Derating Curves of Maximum Power Dissipation

17.10 Layout Considerations

Follow the PCB layout guidelines for optimal performance of the RT2872.

- Put the input capacitor as close as possible to the device pins (VIN and GND).
- The SW node has a high-frequency voltage swing and should be kept to a small area. Keep sensitive components away from the SW node to prevent stray capacitive noise pickup.
- The RT resistor, compensator, and feedback components must be connected as close to the device as possible. The GND and Exposed Pad should be connected to a strong ground plane for heat sinking and noise protection.

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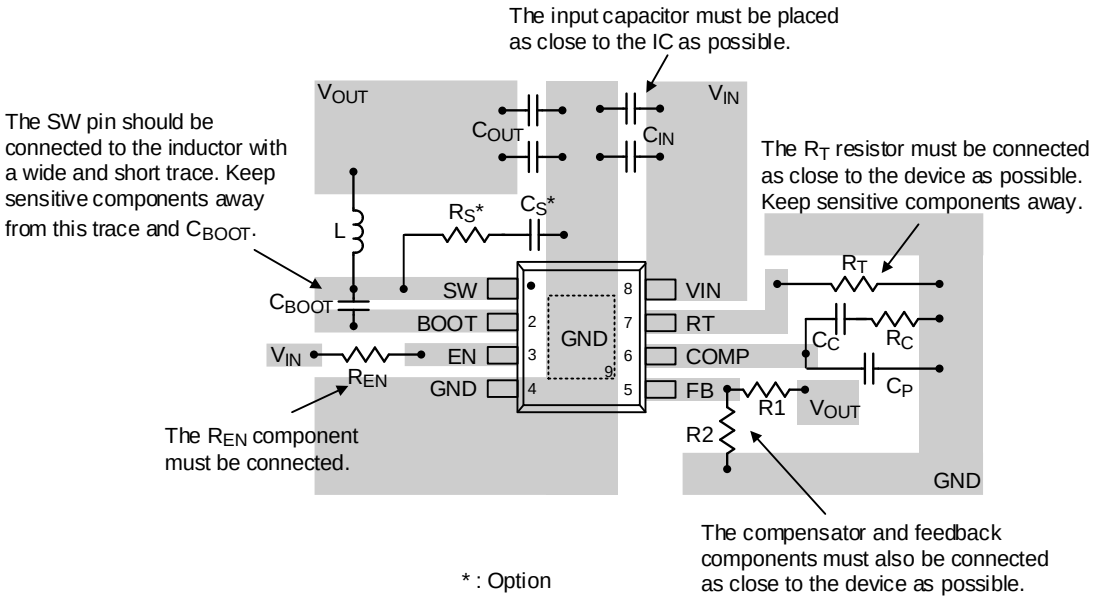

Figure 8. PCB Layout Guide

Note 6. The information provided in this section is for reference only. The customer is solely responsible for the designing, validating, and testing your product incorporating Richtek's product and ensure such product meets applicable standards and any safety, security, or other requirements.

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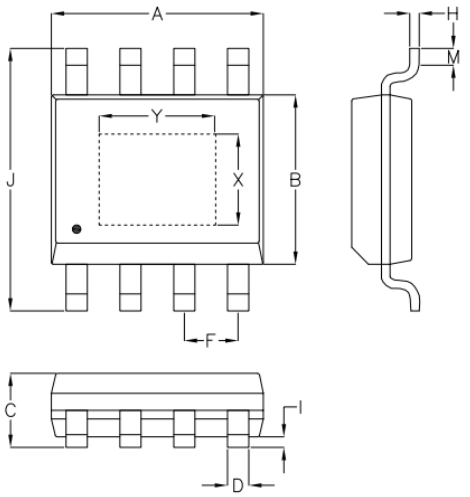
18 Outline Dimension



Symbol		Dimensions In Millimeters		Dimensions In Inches	
		Min	Max	Min	Max
A		4.801	5.004	0.189	0.197
B		3.810	4.000	0.150	0.157
C		1.346	1.753	0.053	0.069
D		0.330	0.510	0.013	0.020
F		1.194	1.346	0.047	0.053
H		0.170	0.254	0.007	0.010
I		0.000	0.152	0.000	0.006
J		5.791	6.200	0.228	0.244
M		0.406	1.270	0.016	0.050
Option 1	X	2.000	2.300	0.079	0.091
	Y	2.000	2.300	0.079	0.091
Option 2	X	2.100	2.500	0.083	0.098
	Y	3.000	3.500	0.118	0.138

8-Lead SOP (Exposed Pad) Plastic Package

Note 7. The package of the RT2872 uses Option 2.

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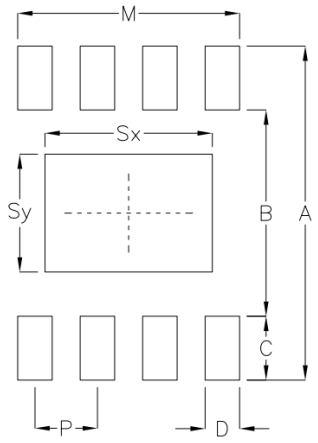
19 Footprint Information



Package		Number of Pin	Footprint Dimension (mm)								Tolerance
			P	A	B	C	D	Sx	Sy	M	
PSOP-8	Option1	8	1.27	6.80	4.20	1.30	0.70	2.30	2.30	4.51	±0.10
	Option2							3.40	2.40		

Note 8. The package of the RT2872 uses Option 2.

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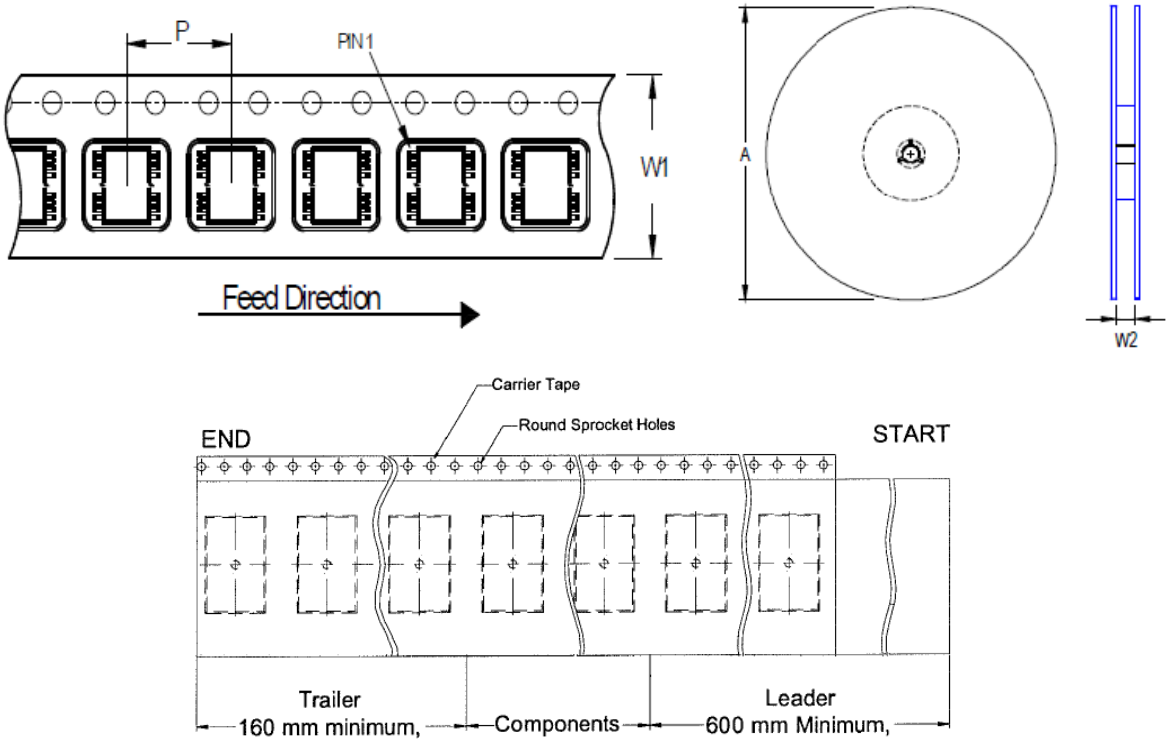
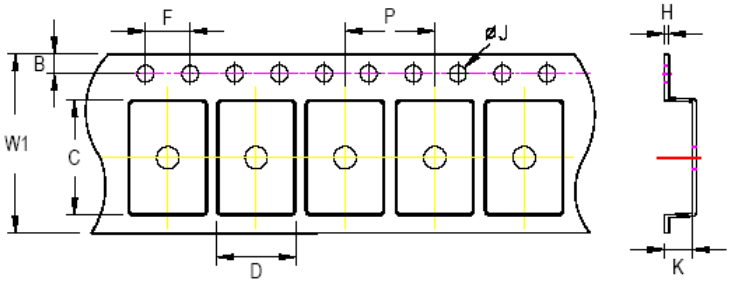
20 Packing Information

20.1 Tape and Reel Data



Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min/Max (mm)
			(mm)	(in)				
PSOP-8	12	8	330	13	2,500	160	600	12.4/14.4



C, D and K are determined by component size. The clearance between the components and the cavity is as follows:

- For 12mm carrier tape: 0.5mm max.

Tape Size	W1	P		B		F		ØJ		K		H
	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Max
12mm	12.3mm	7.9mm	8.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	1.9mm	2.2mm	0.6mm

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20.2 Tape and Reel Packing

Step	Photo/Description	Step	Photo/Description
1	 Reel 13”	4	 1 reel per inner box **Box G**
2	 HIC & Desiccant (2 Unit) inside	5	 6 inner boxes per outer box
3	 Caution label is on backside of Al bag	6	 Outer box **Carton A**

Container / Package	Reel		Box			Carton		
	Size	Units	Item	Reels	Units	Item	Boxes	Units
PSOP-8	13”	2,500	Box G	1	2,500	Carton A	6	15,000

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20.3 Packing Material Anti-ESD Property

Surface Resistance	Aluminum Bag	Reel	Cover tape	Carrier tape	Tube	Protection Band
Ω/cm^2	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**

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21 Datasheet Revision History

Version	Date	Description	Item
07	2023/2/6	Modify	*Operation on page 4* *Application Information on page 10*
08	2024/12/19	Modify	*General Description on page 1* *Features on page 1* *Ordering Information on page 1* *Functional Pin Description on page 3* *Electrical Characteristics on page 5, 6* *Operation on page 11, 12* *Application Information on page 13 to 19* *Footprint Information on page 21* *- Added Footprint Information* *Packing Information on page 22 to 24* *- Added packing information*

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