RICHTEK®

RT1718S

Type-C Port Controller (TCPC) with IEC-ESD Protection on SBU/CC/DP/DM, USB2.0 Switch, Charging Port Controller, and Power-Path Control

1 General Description

The RT1718S is a highly integrated TCPC controller that incorporates IEC-61000-4-2 ESD protection cell for CC/SBU/DP/DM. The RT1718S integrates several high voltage protection switches for SBU1/SBU2/DP/DM to prevent high voltage VBUS from touching the adjacent pins. The AMR of the SBU OVP switch is 24V. HV DCP and fast charging protocols are integrated into the high voltage USB 2.0 switches.

The RT1718S can control the VBUS sink and source path by an internal charge pump for NMOSFETs and GPIO for PMOSFETs. The GPIOs of the RT1718S can also be configured to control system blocks such as USB 3.0 to DP Mux for alternate mode usage.

A VCONN switch with OVP/OCP/RVP/UVP protection is also integrated. The RPD_CC1/CC2 are the dead battery mode Rd pins, which are independent from CC1/CC2 for each customer's system flexibility.

The RT1718S is available in a WQFN-32L 4x4 package. The recommended junction temperature range is –40°C to 125°C, and the ambient temperature range is –40°C to 85°C.

2 Ordering Information

RT1718S□□

Package Type(1)
QW: WQFN-32L 4x4 (W-Type)

Lead Plating System
G: Richtek Green Policy Compliant(2)

Note 1.

- Marked with (1) indicated: Compatible with the current requirements of IPC/JEDEC J-STD-020.
- Marked with (2) indicated: Richtek products are Richtek Green Policy compliant.

3 Features

- **Support TCPC Interface Revision1.0 Version1.2**
- **Low Voltage DRP (2V)**
- **CC AMR = 24V, Meet IEC-61000-4-2 ESD Protection**
- **SBU AMR = 24V, Meet IEC-61000-4-2 ESD Protection with OVP Switch Function**
- **DP/DM USB2.0 Switch with 3dB BW of 800MHz, High Voltage of 21V Protection, and Meet IEC-61000-4-2 ESD Protection**
- **DP/DM Supports Charging Port Controller for SINK and SRC Port (BC1.2, and Other Proprietary Protocols)**
- **Control External NMOSFET and PMOSFET for Power Path**
- **Power Path with VBUS OCP of SRC Mode**
- **3-GPIO are Configurable**
- **4-State ADDR Pin for Multiport Application**
- **Dead Battery Mode Rd is on RPD_CC1/CC2**
- **Powered by VBUS and VCC**

4 Applications

- Desktops, Notebooks, PCs
- USB Hubs/Dongles
- TVs/Monitors
- Servers/Data Centers

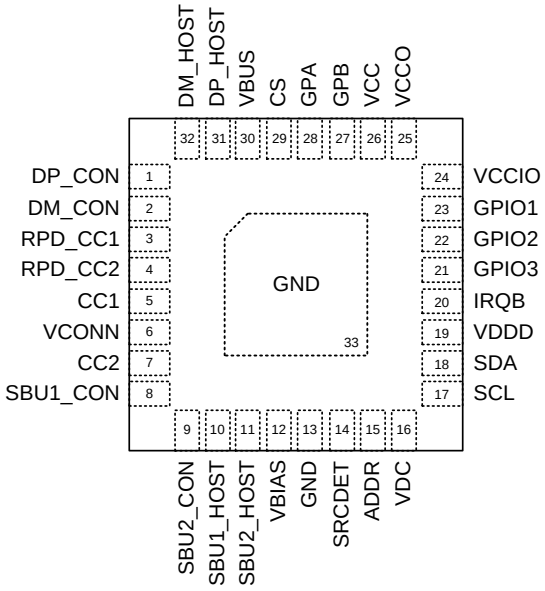
5 Marking Information

GH= : Product Code
YMDNN : Date Code

Table of Contents

6 Pin Configuration

(TOP VIEW)



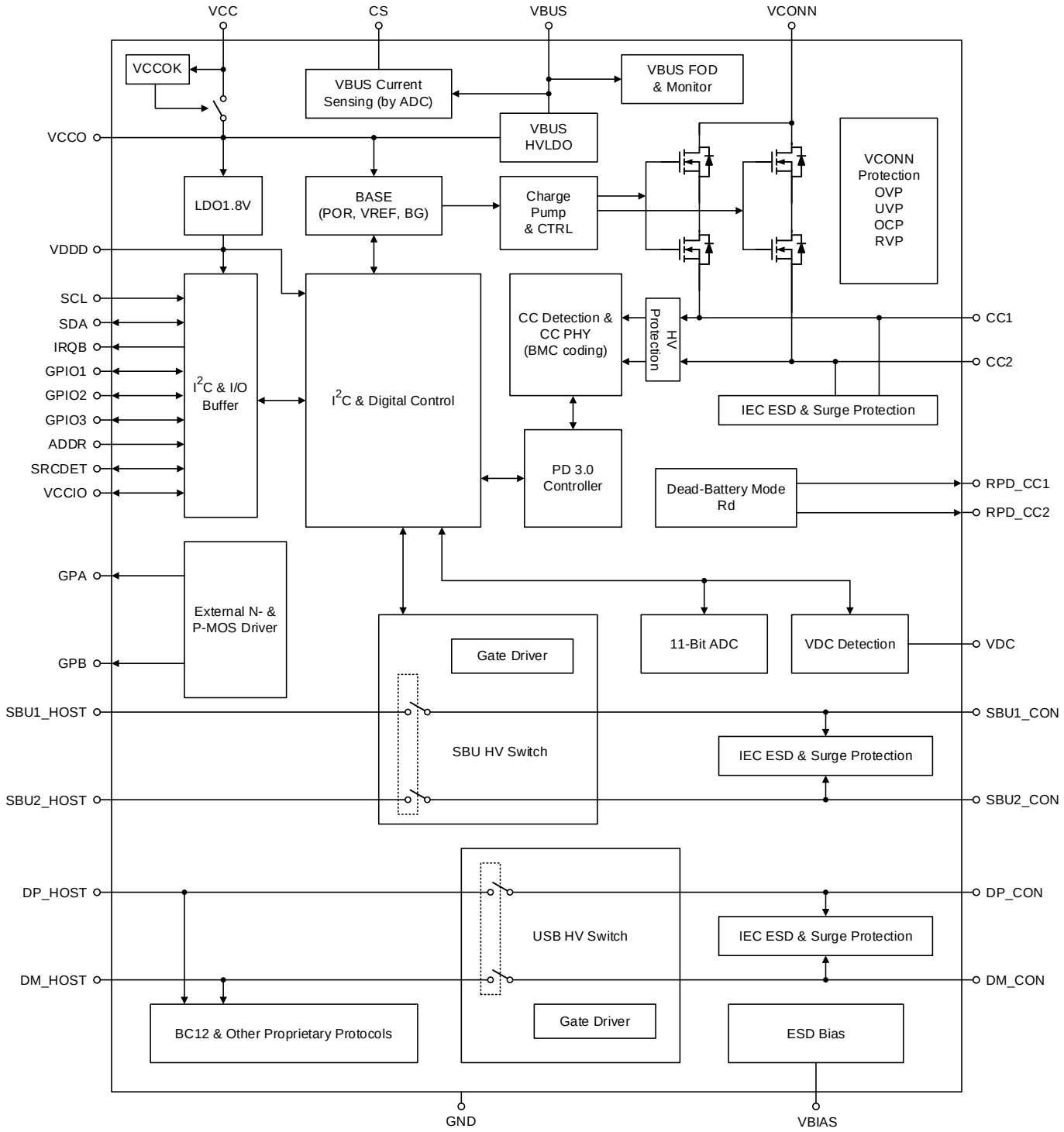
WQFN-32L 4x4

7 Functional Pin Description

Pin No.	Pin Name	Pin Function
1	DP_CON	Type-C connector side DP. Connect to DP of Type-C USB connector.
2	DM_CON	Type-C connector side DM. Connect to DM of Type-C USB connector.
3	RPD_CC1	Short to CC1 with a 200Ω resister if dead battery resistors are needed.
4	RPD_CC2	Short to CC2 with a 200Ω resister if dead battery resistors are needed.
5	CC1	Type-C connector configuration channel pin. Initially used to determine when an attachment has occurred and what the orientation detected. Place a 560pF (0603/50V) capacitor to the pin.
6	VCONN	Regulated power input pin to output VCONN through CC pin for Type-C full-featured cables and other accessories. If the type c port does not support V_{CONN} power, connect this pin to GND with 10kΩ resister.
7	CC2	Type-C connector configuration channel pin. Initially used to determine when an attachment has occurred and what the orientation detected. Place a 560pF (0603/50V) capacitor to the pin.
8	SBU1_CON	Type-C connector side SBU1. Connect to SBU1 of Type-C USB connector.
9	SBU2_CON	Type-C connector side SBU2. Connect to SBU2 of Type-C USB connector.
10	SBU1_HOST	System side SBU1. Connect to SBU1 of System controller.
11	SBU2_HOST	System side SBU2. Connect to SBU2 of System controller.
12	VBIAS	Place a 0.1μF (0402/50V/X7R) capacitor to the pin. This pin cannot drive external load.
13, 33 (Exposed Pad)	GND (Exposed Pad)	Ground. The exposed pad must be connected to GND and be well soldered to a large copper PCB for maximum power dissipation.

Pin No.	Pin Name	Pin Function
14	SRCDET	Setting pin for detecting the RP level without VCC power. Detect the RP level to control the power path by GPIO3.
15	ADDR	Address selection node when used with multiple Type-C ports.
16	VDC	Barrel jack DC power input detection pin.
17	SCL	I^2C interface serial clock input, open-drain. An external pull-up resistor is required.
18	SDA	I^2C interface serial data input/output, open-drain. An external pull-up resistor is required.
19	VDDD	Place a 1μF capacitor to the pin. This pin cannot drive external load.
20	IRQB	Interrupt output, active-low open-drain, to prompt the processor to read the registers.
21	GPIO3	Configurable GPIO3 with open-drain or push-pull type, used for switch control, DC-DC enable, audio enable, and accessory unit control.
22	GPIO2	Configurable GPIO2 with open-drain or push-pull type, used for switch control, DC-DC enable, audio enable, and accessory unit control.
23	GPIO1	Configurable GPIO1 with open-drain or push-pull type, used for switch control, DC-DC enable, audio enable, and accessory unit control.
24	VCCIO	Power input for GPIO1/2/3 application.
25	VCCO	Place a 1μF capacitor to the pin. This pin cannot drive external load.
26	VCC	Main power input for the RT1718S.
27	GPB	High voltage gate driver B, which can be used to drive an NMOSFET/PMOSFET power switch. This pin is connected to the gate of the power switch. (Related to VBUS).
28	GPA	High voltage gate driver A, which can be used to drive an NMOSFET/PMOSFET power switch. This pin is connected to the gate of the power switch. (Related to VBUS).
29	CS	VBUS current sense input. Place a 3.3Ω resistor in series between the current sensing resistor and the CS pin. Place a 0.1μF capacitor between the CS pin and the VBUS pin.
30	VBUS	VBUS input for OCP/OVP/RCP detection and power input for VBUS to 3.3V regulator.
31	DP_HOST	System side DP_HOST. Connect to DP of system controller.
32	DM_HOST	System side DM_HOST. Connect to DM of system controller.

8 Functional Block Diagram



9 Absolute Maximum Ratings

(Note 2)

- VBUS, CS, GPA, GPB ---------- –0.3V to 28V
- CC1, CC2, RPD_CC1, RPD_CC2, VBIAS
  SBU1_CON, SBU2_CON, DP_CON, DM_CON ---------- –0.3V to 24V
- SBU1_HOST, SBU2_HOST, DP_HOST,
  DM_HOST, VCC, VCCO, VCONN, VCCIO ---------- –0.3V to 6V
- SDA, SCL, IRQB, ADDR, GPIO1, GPIO2, GPIO3, VDC, SRCDET ---------- –0.3V to 6V
- VDDD ---------- –0.3V to 2V
- IGPIO1, IGPIO2, IGPIO3 ---------- –20mA to 20mA
- Output Current (DP_CON/DM_CON/DP_HOST/DM_HOST) ---------- –100mA to 100mA
- Output Current (SBU1_CON/SBU2_CON/SBU1_HOST/SBU2_HOST) ---------- –100mA to 100mA
- Power Dissipation, P_D @ T_A = 25°C
- WQFN-32L 4x4 ---------- 3.59W
- Package Thermal Resistance (Note 3)
- WQFN-32L 4x4, θ_{JA} ---------- 27.8°C/W
- WQFN-32L 4x4, θ_{JC} ---------- 7°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 4)
  HBM (Human Body Model) ---------- ±2kV
  DP_CON, DM_CON, CC1, CC2, SBU1_CON, SBU2_CON, VBUS
  (IEC 61000-4-2 Contact Discharge) ---------- ±8kV
  DP_CON, DM_CON, CC1, CC2, SBU1_CON, SBU2_CON, VBUS
  (IEC 61000-4-2 Air Discharge) ---------- ±5kV
  DP_CON, DM_CON, CC1, CC2, SBU1_CON, SBU2_CON, VBUS
  (IEC 61000-4-5 Surge) ---------- ±28V

Note 2. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 3. θ_{JA} is simulated under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. θ_{JC} is simulated at the bottom of the package.

Note 4. Devices are ESD sensitive. Handling precautions are recommended.

10 Recommended Operating Conditions

(Note 5)

- Supply Input Voltage, VCC ---------- 2.7V to 5.5V
- VBUS ---------- 4V to 22V
- VDC ---------- 0V to 5.5V
- VCONN Supply Voltage ---------- 2.8V to 5.5V
- VCONN Supply Current ---------- 100mA to 800mA
- VCCIO ---------- 1.5V to 5.5V
- DP_CON/DM_CON/DP_HOST/DM_HOST ---------- 0V to 4V
- SBU1_CON/SBU2_CON/SBU1_HOST/SBU2_HOST ---------- 0V to 3.4V
- Ambient Temperature Range ---------- –40°C to 85°C
- Junction Temperature Range ---------- –40°C to 125°C

Note 5. The device is not guaranteed to function outside its operating conditions.

11 Electrical Characteristics

(V_{CC} = 2.7V to 5.5V, V_{CC} (Typical) = 3.3V, T_A = –40°C to 85°C and T_A (Typical) = 25°C, unless otherwise specified.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Operation Current						
Shutdown Current	I_{SHDN}	Power-on state (DPDM, SBU switched off)	--	15	70	μA
Low Power DRP Mode Current	$I_{LOWPOWER}$	CC toggle at DRP mode when port is unconnected and waiting for connection	--	20	75	μA
Idle Mode Current when Attached as Sink	I_{IDLE}	VCONN off SBUx switch is off DP/DM switch is off (0xF23A = 00h) GPA/B charge pump is off (0xEC[1:0] = 00b)	--	185	230	μA
Normal Mode Current when Attached as Sink	I_{NORMAL}	VCONN off SBUx switch is off DP/DM switch is off (0xF23A = 00h) GPA/B charge pump is off (0xEC[1:0] = 00b)	--	640	800	μA
More VCC Consumption when DPDM, SBU1/2 Switches On	I_{SWITH_ON}	SBUx switch is on DP/DM switch is on (0xF23A = CFh)	--	70	120	μA
More VCC Consumption when Charge Pumps of GPA and GPB Are On	I_{CP_GATE}	GPA/B charge pump is on (0xEC[1:0] = 11b)	--	350	380	μA

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
More VCC Consumption when VBUS Measurement of ADC Is On	I_{ADC}	VBUS measurement of ADC is on (0x1C[6] = 0b)	--	160	230	μA
More VCC Consumption when VBUS OCP1 Is On	I_{ADC_OCP}	VBUS OCP1 is on (0x1B[2] = 0b)	--	230	300	μA
More VCC Consumption when TX Mode with CC Communication	I_{CC_TX}		--	2.2	3.1	mA
VBUS Related Parameters						
VBUS_PRESENT Voltage Threshold Rising	$V_{BUS\_PRESENT\_R}$	V_{CC}: 2.7V to 5.5V	3.7	3.8	3.9	V
VBUS_PRESENT Voltage Threshold Falling	$V_{BUS\_PRESENT\_F}$	V_{CC}: 2.7V to 5.5V	3.4	3.5	3.6	V
VBUS Vsafe0V Falling	$V_{BUS\_Vsafe0V\_F}$	V_{CC}: 2.7V to 5.5V	--	0.42	0.8	V
VBUS Vsafe0V Rising	$V_{BUS\_Vsafe0V\_R}$	V_{CC}: 2.7V to 5.5V	0.55	0.62	1	V
VBUS OVP Variation (at VBUS OVP Setting *1.2, i.e. 0xF213[5:4] = 11b)	$V_{BUS\_OVP\_VAR}$	V_{CC}: 2.7V to 5.5V	–10	--	10	%
OVP Response Time on The CC Pins	$t_{VBUS\_OVP\_tResponse}$	Time from OVP asserted until OVP MOSFETs turn off. V_{CC}: 2.7V to 5.5V	--	--	12	μs
VBUS OCP1/2	$I_{VBUS\_OCP1/2}$	V_{CC}: 2.7V to 5.5V	0.2	--	12.9	A
VBUS OCP1/2 STEP	$I_{VBUS\_OCP1/2\_STEP}$	V_{CC}: 2.7V to 5.5V	--	100	--	mA
VBUS OCP1/2 Accuracy	$I_{VBUS\ \_OCP1/2\_ACC}$	V_{CC}: 2.7V to 5.5V Tested with a 10mΩ current sensing resistor. It is not considered the variation from current sensing resistor. LSB is 33.33mA.	–5	--	5	LSB
VBUS OCP3	I_{VBUS_OCP3}		7.25	--	15	A
VBUS OCP3 Accuracy	$V_{BUS\_OCP3\_ACC}$	V_{CC}: 2.7V to 5.5V Tested with a 10mΩ current sensing resistor. It is not considered the variation from current sensing resistor.	–6	--	6	%
VBUS OCP3 Time	t_{VBUS_OCP3}		--	--	12	μs
VBUS RCP1/2	$I_{VBUS\_RCP1/2}$	V_{CC}: 2.7V to 5.5V	0.2	--	12.9	A
VBUS RCP1/2 STEP	$I_{VBUS\_RCP1/2\_STEP}$	V_{CC}: 2.7V to 5.5V	--	100	--	mA

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VBUS RCP1/2 Accuracy	$I_{VBUS\_RCP1/2\_ACC}$	V_{CC}: 2.7V to 5.5V Tested with a 10mΩ current sensing resistor. It is not considered the variation from current sensing resistor. LSB is 33.33mA.	−5	--	5	LSB
VBUS RCP3	I_{VBUS_RCP3}		7.25	--	15	A
VBUS RCP3 Accuracy	$I_{VBUS\_RCP3\_Accuracy}$		−20	--	20	%
VBUS RCP3 Time	t_{VBUS_RCP3}		--	--	12	μs
VBUS Foreign Object Detection						
FOD Pull-Up Open Voltage	V_{FOD_LDO}		1.9	2	2.1	V
FOD OV Level	V_{FOD_OV}		2.16	2.4	2.64	V
FOD Pre-Charge Current	I_{FOD_PRE}		18	20	22	mA
FOD Sense Current1	I_{FOD_SENSE1}		9.5	10	10.5	mA
FOD Sense Current2	I_{FOD_SENSE2}		4.5	5	5.5	mA
Sense Resistor Level	R_{FOD_SENSE}		−10	--	10	%
Type-C Port Control						
DFP 80μA CC Current	$I_{NOR\_RP80\mu A}$		64	80	96	μA
DFP 180μA CC Current	$I_{NOR\_RP180\mu A}$		166	180	194	μA
DFP 330μA CC Current	$I_{NOR\_RP330\mu A}$		304	330	356	μA
UFP Rd	R_d		4.59	5.1	5.61	kΩ
UFP Pull-Down Voltage in Dead Battery under DFP 80μA	$V_{DB\_80\mu A}$		0.25	--	1.5	V
UFP Pull-Down Voltage in Dead Battery under DFP 180μA	$V_{DB\_180\mu A}$		0.45	--	1.5	V
UFP Pull-Down Voltage in Dead Battery under DFP 330μA	$V_{DB\_330\mu A}$		0.85	--	2.45	V
CC Communication						
Bit Rate	$f_{BITRATE\_PD}$		270	300	330	kbps
Maximum Difference between The Bit-Rate during The Part of The Packet Following The Preamble and The Reference Bit-Rate	$p_{BITRATE}$		--	--	0.25	%

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Time from The End of Last Bit of A Frame until The Start of The First Bit of The Next Preamble	$t_{INTERFRAMEGAP}$		25	--	--	μs
Time Before The Start of The First Bit of The Preamble when The Transmitter Shall Start Driving The Line	$t_{STARTDRIVE}$		–1	--	1	μs
Time To Cease Driving The Line after The End of The Last Bit of The Frame	$t_{ENDDRIVEBMC}$		--	--	23	μs
Fall Time	t_F		300	--	--	ns
Time To Cease Driving The Line after The Final High-To-Low Transition	$t_{HOLDLOWBMC}$		1	--	--	μs
Rise Time	t_R		300	--	--	ns
Voltage Swing	V_{SWING}		1.05	1.125	1.2	V
Transmitter Output Impedance	Z_{DRIVER}		33	50	75	Ω
BMC Receiver Input Impedance	Z_{BMCRX}		1	--	--	MΩ
VCONN Switch						
VCONN OVP	V_{CONN_OVP}	The rising voltage threshold at the CC pin outputs V_{CONN}.	5.55	--	6	V
Released VCONN OVP	$V_{CONN\_OVP\_RELEASED}$	The falling voltage threshold at the CC pin outputs V_{CONN}.	5.5	--	5.95	V
VCONN Undervoltage Protection Threshold	V_{CONN_UVP}		2.4	2.7	3	V
VCONN Undervoltage Protection Hysteresis	$V_{CONN\_UVP\_HYS}$		50	100	150	mV
VCONN RVP1	V_{CONN_RVP1}		0.1	0.3	0.55	V
VCONN RVP2	V_{CONN_RVP2}		0.3	0.5	0.85	V
VCONN OCP Range (Shutdown)	$I_{VCONN\_OCP\_RANGE}$		100	--	800	mA
VCONN OCP Variation (Shutdown)	$I_{VCONN\_OCP\_VARIATION}$		–10	--	10	%
On-Resistance of VCONN Switch	R_{DSON_VCONN}		--	0.7	1	Ω

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
SBU Switch						
On Leakage Current of SBU Switch	$I_{ONLK\_SBU\_CON\_3.6V}$	V_{CC} = 3.3V, SBU_CON = 0V to 3.6V, the SBU_HOST is floating, the SBU switch is on, measure the current of the SBU_CON	–3	--	3	μA
Off Leakage Current of SBU_CON	$I_{OFFLK\_SBU\_CON\_3.6V}$	V_{CC} = 3.3V, SBU_CON = 0V to 3.6V, the SBU_HOST is floating, the SBU switch is off, measure the current of the SBU_CON	–3	--	3	μA
Off Leakage Current of SBU_CON	$I_{OFFLK\_SBU\_CON\_24V}$	V_{CC} = 3.3V, SBU_CON = 24V, the SBU_HOST is 0V, the SBU switch is under OVP, measure the current of the SBU_CON	--	--	800	μA
Power−Off Leakage Current of SBU_CON	$I_{OFFLK\_SBU\_CON\_3.6V}$	V_{CC} = 0V, SBU_CON = 0V to 3.6V, the SBU_HOST is floating, measure the current of the SBU_CON	–3	--	3	μA
On Leakage Current of SBU_HSOT	$I_{ONLK\_SBU\_HOST\_3.6V}$	V_{CC} = 3.3V, SBU_HOST = 0V to 3.6V, the SBU_CON is floating, the SBU switch is on, measure the current of the SBU_HOST	–3	--	3	μA
Off Leakage Current of SBU_HOST	$I_{OFFLK\_SBU\_HOST\_3.6V}$	V_{CC} = 3.3V, SBU_HOST = 0V to 3.6V, the SBU_CON is floating, the SBU switch is off, measure the current of the SBU_HOST	–3	--	3	μA
Off Leakage Current of SBU_CON to SBU_HSOT	$I_{OFFLK\_SBU\_CON\_24V}$ to SBU_HOST	V_{CC} = 0V or 3.3V SBU_CON = 24 V The SBU_HOST pins are set to 0V, SBU switch is under OVP, measure the leakage out of the SBU_HOST pins	–1	--	1	μA
SBU Input OVP Lockout 4.5V	$V_{SBU\_OVP\_TRIP\_4.5V}$	V_{CC} = 3.3V, the SBU_CON rises from 4V until the SBU_HOST goes from H to L	4.4	4.5	4.6	V
SBU Input OVP Lockout 3.8V	$V_{SBU\_OVP\_TRIP\_3.8V}$	V_{CC} = 3.3V, the SBU_CON rises from 3.3V until the SBU_HOST goes from H to L	3.7	3.8	3.9	V
SBU Input OVP Lockout 3.7V	$V_{SBU\_OVP\_TRIP\_3.7V}$	V_{CC} = 3.3V, the SBU_CON rises from 3.3V until the SBU_HOST goes from H to L	3.6	3.7	3.8	V
SBU Input OVP Lockout 3.6V	$V_{SBU\_OVP\_TRIP\_3.6V}$	V_{CC} = 3.3V, the SBU_CON rises from 3.3V until SBU_HOST goes from H to L	3.5	3.6	3.7	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
SBU Input OVP Hysteresis	$V_{SBU\_OVP\_HYS}$	V_{CC} = 3.3V, the SBU_CON falls from 5V until SBU_HOST goes from L to H	35	60	85	mV
SBU Pins OVP Response Time	t_{SBU_OVP}	V_{CC} = 3.3V, hot-plug with 1m cable voltage SBU_CON = 0 to 24V, 40V/μs. Place a 100nF capacitor and 40 Ω resistor in series to GND on SBU_HOST. Time from OVP trip voltage predicated to switches to turn OFF	--	60	120	ns
On-Resistance of SBU_HOST Switch	R_{DSON_SBU}	V_{CC} = 3.3V, VSBU_CON = 0V to 3.6 V, I_{SW} = 30mA	--	6	9	Ω
SBU On-Resistance Flatness	$R_{DSON\_FLAT\_SBU}$	V_{CC} = 3.3V, Sweep SBU_CON voltage between 0 V and 3.6V. –40°C ≤ T_J ≤ 85°C	--	--	0.15	Ω
SBU_HOST Switch Turn-On Time	t_{ON_SBU}	V_{CC} = 3.3V, SBU_CON = 2.5V, place a 50Ω resistor in series to GND on SBU_HOST. The time from the I^2C turn-on command to when the SBU_HOST voltage reaches 90% of SBU_CON	150	250	400	μs
SBU_HOST Switch Turn-Off Time	t_{OFF_SBU}	V_{CC} = 3.3V, SBU_CON = 2.5 V, place a 50Ω resistor in series to GND on SBU_HOST. The time from the I^2C turn-off command to when the SBU_HOST voltage reaches 10% of SBU_CON	--	15	20	μs
–3dB Bandwidth	BW_{SBU}	Single ended, 50Ω terminal, VSBU_CON = 0.1V to 1.2V	200	--	--	MHz
Crosstalk for SBU	X_{talk_SBU}	Swing 1VPP at 1MHz, measure the SBU_HOST1 to SBU_CON2 or SBU_HOST2 to SBU_CON1 with 50W terminal	–51	–80	--	dB
Short-to-VBUS System-Side Clamping Voltage on the SBU_HOST Pins	$V_{STBUS\_SBUHOST\_CLAMP}$	V_{CC} = 3.3V, hot-plug with 1m cable voltage SBU_CON = 0 to 24 V, 40V/us. Place a 100nF capacitor and a 40Ω resistor in series to GND on SBU_HOST.	--	7	8.5	V
DP/DM HV Switch						
On Leakage Current of USB Switch	$I_{ONLK\_CON\_USB\_3.6V}$	V_{CC} = 3.3V DP_CON, DM_CON =0V to 3.6V, DP_HOST and DM_HOST are floating, DP and DM switch on, measure the current of DP_CON, DM_CON	–3	--	3	μA

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Off Leakage Current of DP_CON and DM_CON	$I_{OFFLK\_CON\_USB\_3.6V}$	V_{CC} = 3.3V DP_CON, DM_CON = 0V to 3.6V, DP_HOST and DM_HOST are floating, DP and DM switch off, measure the current of DP_CON, DM_CON	–3	--	3	μA
Off Leakage Current of DP_CON and DM_CON	$I_{OFFLK\_CON\_USB\_24V}$	V_{CC} = 3.3V DP_CON, DM_CON = 24V, DP_HOST, and DM_HOS are 0V, DP and DM switch OVP, measure the current of DP_CON, DM_CON	--	--	800	μA
Power-Off Leakage Current of DP_CON and DM_CON	$I_{OFFLK\_CON\_USB\_3.6V}$	V_{CC} = 0V DP_CON, DM_CON = 0V to 3.6V, DP_HOST and DM_HOST are floating, measure the current of SBU_CON	–3	--	3	μA
On Leakage Current of DP_HOST and DM_HOST	$I_{ONLK\_USB\_HOST\_3.6V}$	V_{CC} = 3.3V DP_HOST, DM_HOST =0V to 3.6V, DP_CON and DM_CON are floating, SBU switch on, measure the current of DP_HOST, DM_HOST	–3	--	3	μA
Off Leakage Current of DP_HOST and DM_HOST	$I_{OFFLK\_USB\_HOST\_3.6V}$	V_{CC} = 3.3V DP_HOST, DM_HOST = 0V to 3.6V, DP_CON and DM_CON are floating, SBU switch off, measure the current of DP_HOST, DM_HOST	–3	--	3	μA
Off Leakage Current of CON_USB to USB_HSOT	$I_{OFFLK\_CON\_USB\_24V}$ to USB_HOST	V_{CC} = 0V or 3.3V DP_CON, DM_CON = 24V DP_HOST and DM_HOST pins are set to 0 V, SBU switch OVP, measure leakage out of DP_HOST, DM_HOST pins	–1	--	1	μA
USB Input OVP Lockout	$V_{OVP\_USB\_TRIP}$	V_{CC} = 3.3V, DP_CON, DM_CON rises from 4V until DP_HOST and DM_HOST go from H to L	4.35	4.5	4.7	V
USB Input OVP Hysteresis	$V_{OVP\_USB\_HYS}$	V_{CC} = 3.3V, DP_CON, DM_CON falls from 5V until DP_HOST and DM_HOST go from L to H	35	60	85	mV
DP and DM Pins OVP Response Time	t_{OVP_USB}	V_{CC} = 3.3V, Hot-Plug with 1m cable voltage DP_CON, DM_CON = 0 to 24V, 40V/μs. Put a 100nF capacitor and 40Ω in series to GND on DP_HOST and DM_HOST. Time from OVP trip voltage predicated to switches to turn OFF	--	60	120	ns

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
On-Resistance of USB Switch	R_{DSON_USB}	V_{CC} = 3.3V, VDP_CON, VDM_CON = 0V to 3.6V, I_{SW} = 8mA	--	6	9	Ω
USB On-Resistance Flatness	$R_{DSON\_FLAT\_USB}$	V_{CC} = 3.3V, Sweep VDP_CON, VDM_CON voltage between 0V and 3.6V. –40°C ≤ T_J ≤ 85°C	--	--	0.15	Ω
USB Switch Turn-On Time	t_{ON_USB}	V_{CC} = 3.3V, DP_CON, DM_CON = 2.5V, Put a 50Ω in series to GND on DP_HOST and DM_HOST. Time from I2C turn on command trip DP_HOST and DM_HOST voltage to 90% of SBU_CON	150	250	400	μs
USB Switch Turn-Off Time	t_{OFF_USB}	V_{CC} = 3.3V, DP_CON, DM_CON = 2.5V, Put a 50Ω in series to GND on DP_HOST, DM_HOST. Time from I2C turn off command trip DP_HOST and DM_HOST voltage to 10% of DP_CON and DM_CON	--	15	20	μs
–3dB Bandwidth for USB	BW_{USB}	Single ended, 50Ω terminal, VDP_CON, VDM_CON = 0.1V to 1.2V	700	800	--	MHz
Crosstalk for USB	X_{talk_USB}	Swing 1VPP at 1MHz, measure the DP_HOST to DM_CON or DM_HOST to DP_CON with 50Ω terminal	–51	–80	--	dB
Off Isolation between The DP_HSOT, DM_HOST, and Common Node Pins	OIRR_USB	Test power 0dB at 1kHz, measure the DP_CON to DP_HOST or DM_CON to DM_HOST with 50Ω terminal	–90	–100	--	dB
Short-to-VBUS System-Side Clamping VSB_HOST Pins	$V_{STBUS\_USB\_HOST\_CLAMP}$	V_{CC} = 3.3V, Hot-Plug with 1m cable voltage DP_CON, DM_CON = 0 to 24V, 40V/μs. Put a 100nF capacitor and 40Ω in series to GND on DP_HOST and DM_HOST.	--	7	8.5	V
DP/DM Detection						
DP Source Voltage	V_{DP_SRC}		0.5	0.6	0.7	V
DM Source Voltage	V_{DM_SRC}		0.5	0.6	0.7	V
Data Detect Voltage	V_{DAT_REF}		0.25	0.325	0.4	V
Logic Threshold Voltage	V_{LGC_CHG}		0.8	--	2	V
DP Sink Current	I_{DP_SINK}		50	100	150	μA
DM Sink Current	I_{DM_SINK}		50	100	150	μA
Data Contract Detect Current Source	I_{DP_SRC}		7	10	13	μA

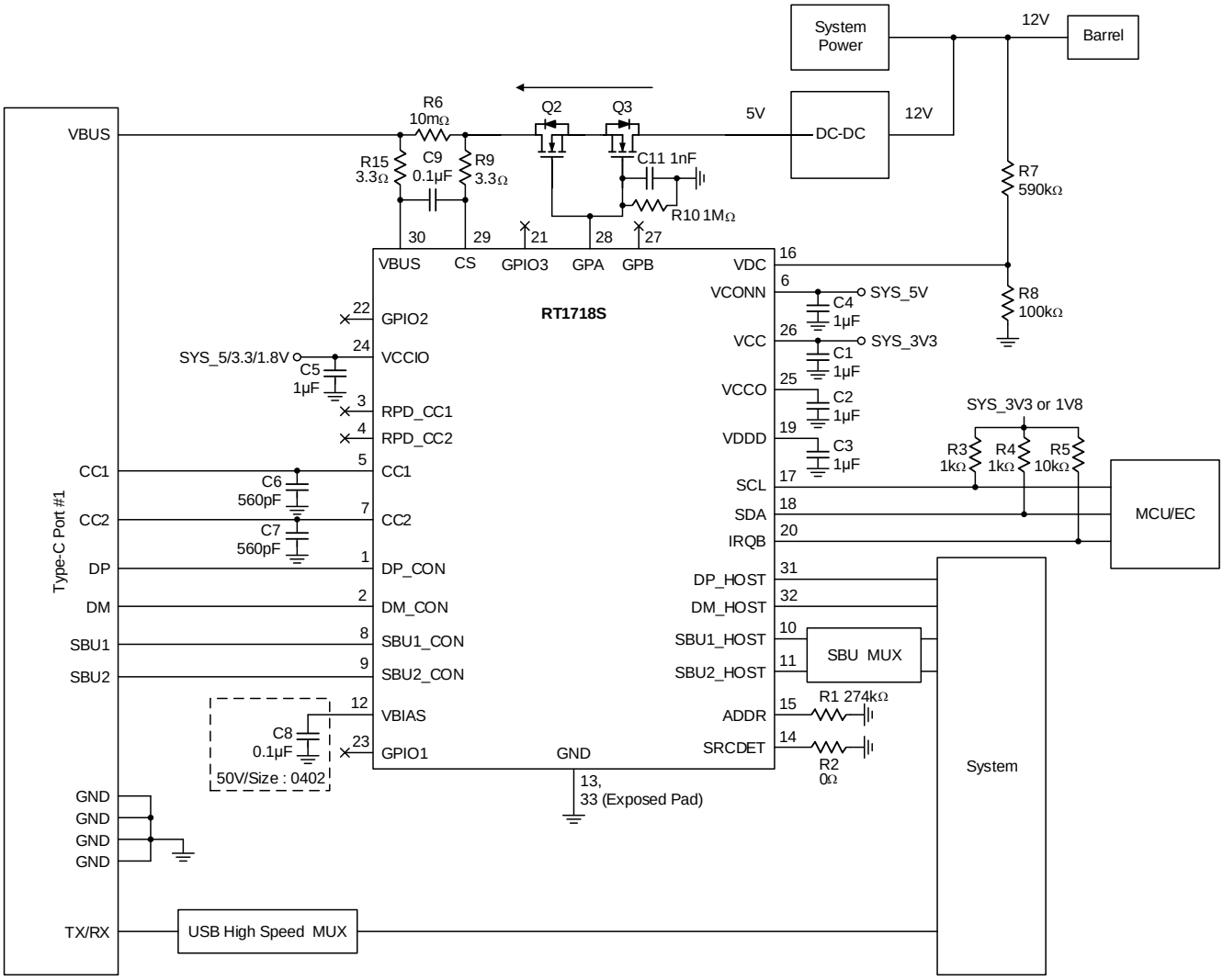
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Dedicated Charging Port Resistance Across DP/DM	R_{DCP_DAT}		--	--	200	Ω
DP Pull-Down Resistance	R_{DP_DWN}		14.25	20	24.8	kΩ
DM Pull-Down Resistance	R_{DM_DWN}		14.25	20	24.8	kΩ
DP Source On-Time	$t_{DP\_SRC\_ON}$		40	64	80	ms
DM Source On-Time	$t_{DM\_SRC\_ON}$		40	64	80	ms
DCD Timeout	$t_{DCD\_TIMEOUT}$		300	600	900	ms
IRQB Electrical Characteristics						
IRQB Low-Level Output Voltage	V_{IRQB_OL}	I_{IRQB_OL} = 4mA	--	--	0.4	V
GPIO						
GPIO Input Voltage HIGH Level	V_{GPIO_IH}		VCCIO x 0.7	--	--	V
GPIO Input Voltage LOW Level	V_{GPIO_IL}		--	--	VCCIO x 0.3	V
GPIO Output Voltage HIGH Level	V_{GPIO_OH}	IOH = -2mA at V_{CC} = 3.3V	VCCIO – 0.7V	--	--	V
GPIO Output Voltage LOW Level	V_{GPIO_OL}	IOL = 4mA at V_{CC} = 3.3V	--	--	0.4	V
GPIO Input Hysteresis	$V_{GPIO\_IN\_HYS}$		400	800	1200	mV
Pull-Up Resistor when Enabled	R_{UP}		36	--	120	kΩ
Pull-Down Resistor when Enabled	R_{DOWN}		36	--	120	kΩ
Input Leakage Current	I_{LK_GPIO}		–1	--	1	μA
ADC						
ADC Resolution	R_{ES_ADC}		--	11	--	Bit
VBUS_DIV Measurement Range	$V_{VBUS\_RANGE\_ADC0}$		0	--	25	V
VBUS_DIV Resolution	$V_{VBUS\_RES\_ADC0}$		--	12.5	--	mV
VBUS_DIV Accuracy	$V_{VBUS\_ACC\_ADC0}$		–50	--	50	mV
VBUS_DIV Measurement Range	$V_{VBUS\_RANGE\_ADC1}$		0	--	5	V
VBUS_DIV Resolution	$V_{VBUS\_RES\_ADC1}$		--	4	--	mV
VBUS_DIV Accuracy	$V_{VBUS\_ACC\_ADC1}$		–20	--	20	mV
CCx Measurement Range	$V_{CCx\_RANGE\_ADC}$		0	--	5	V
CCx Resolution	$V_{CCx\_RES\_ADC}$		--	4	--	mV
CCx Accuracy	$V_{CCx\_ACC\_ADC}$		–20	--	20	mV

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
SBUx Measurement Range	$V_{SBUx\_RANGE\_ADC}$		0	--	5	V
SBUx Resolution	$V_{SBUx\_RES\_ADC}$		--	4	--	mV
SBUx Accuracy	$V_{SBUx\_ACC\_ADC}$		–20	--	20	mV
DP/DM Measurement Range	$V_{DPDM\_RANGE\_ADC}$		0	--	5	V
DP/DM Resolution	$V_{DPDM\_RES\_ADC}$		--	4	--	mV
DP/DM Accuracy	$V_{DPDM\_ACC\_ADC}$		–20	--	20	mV
GPA and GPB						
GPA/B Output High	$V_{OH\_GPA/B}$	Gate driver voltage at Vbus = 0V	4.4	4.7	5	V
GPA/B Pull-Up 1	$I_{PU1\_GPA/B}$		40	55	80	μA
GPA/B Pull-Up 2	$I_{PU2\_GPA/B}$	Time of GPA/B rising from 0V to 8V with VBUS = 5V and capacitance = 1nF at GPA/B.	30	60	90	μs
GPA/B Pull-Down 1	$I_{PD1\_GPA/B}$		40	55	70	μA
GPA/B Pull-Down 2	$I_{PD2\_GPA/B}$		200	250	300	μA
GPA/B Pull-Down 3	$R_{PD3\_GPA/B}$	GPA/B ≤ 2V	2	5	8	kΩ
GPA/B Pull-Down 4	$I_{PD4\_GPA/B}$		150	200	250	μA
VDC						
VDC Detect Threshold Rising 2V	$V_{VDC\_2V\_rising}$		1.93	2.15	2.37	V
VDC Detect Threshold Falling 2V	$V_{VDC\_2V\_falling}$		1.8	2	2.2	V
VDC Detect Threshold Rising 1.5V	$V_{VDC\_1.5V\_rising}$		1.485	1.65	1.815	V
VDC Detect Threshold Falling 1.5V	$V_{VDC\_1.5V\_falling}$		1.35	1.5	1.65	V
VDC Detect Threshold Rising 0.9V	$V_{VDC\_0.9V\_rising}$		0.945	1.05	1.155	V
VDC Detect Threshold Falling 0.9V	$V_{VDC\_0.9V\_falling}$		0.8	0.9	1.0	V
VDC Detect Threshold Rising 0.55V	$V_{VDC\_0.55V\_rising}$		0.6	0.7	0.8	V
VDC Detect Threshold Falling 0.55V	$V_{VDC\_0.55V\_falling}$		0.5	0.55	0.6	V
I^2C						
I^2C Bus Supply Voltage	V_{I2C}	V_{CC} = 3V to 5.5V	1.8	--	3.6	V
Low-Level Input Voltage	V_{IL_I2C}	V_{CC} = 3V to 5.5V	--	--	0.4	V
High-Level Input Voltage	V_{IH_I2C}	V_{CC} = 3V to 5.5V	1.26	--	--	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Low-Level Output Voltage	V_{OL_SDA}	V_{CC} = 3V to 5.5V, open-drain	--	--	0.4	V
Input Current each IO Pin	I_{OL_I2C}	V_{CC} = 3V to 5.5V 0.1VCC < VI < 0.9VCCMAX	−10	--	10	μA
SCL Clock Frequency	f_{SCL}	V_{CC} = 3V to 5.5V	100	--	3000	kHz
Pulse width of spikes that must be suppressed by the input filter	t_{SP}	V_{CC} = 3V to 5.5V	--	--	50	ns
Data Hold Time	$t_{HD;DAT}$	V_{CC} = 3V to 5.5V	30	--	--	ns
Data Set-Up Time	$t_{SU;DAT}$	V_{CC} = 3V to 5.5V	50	--	--	ns

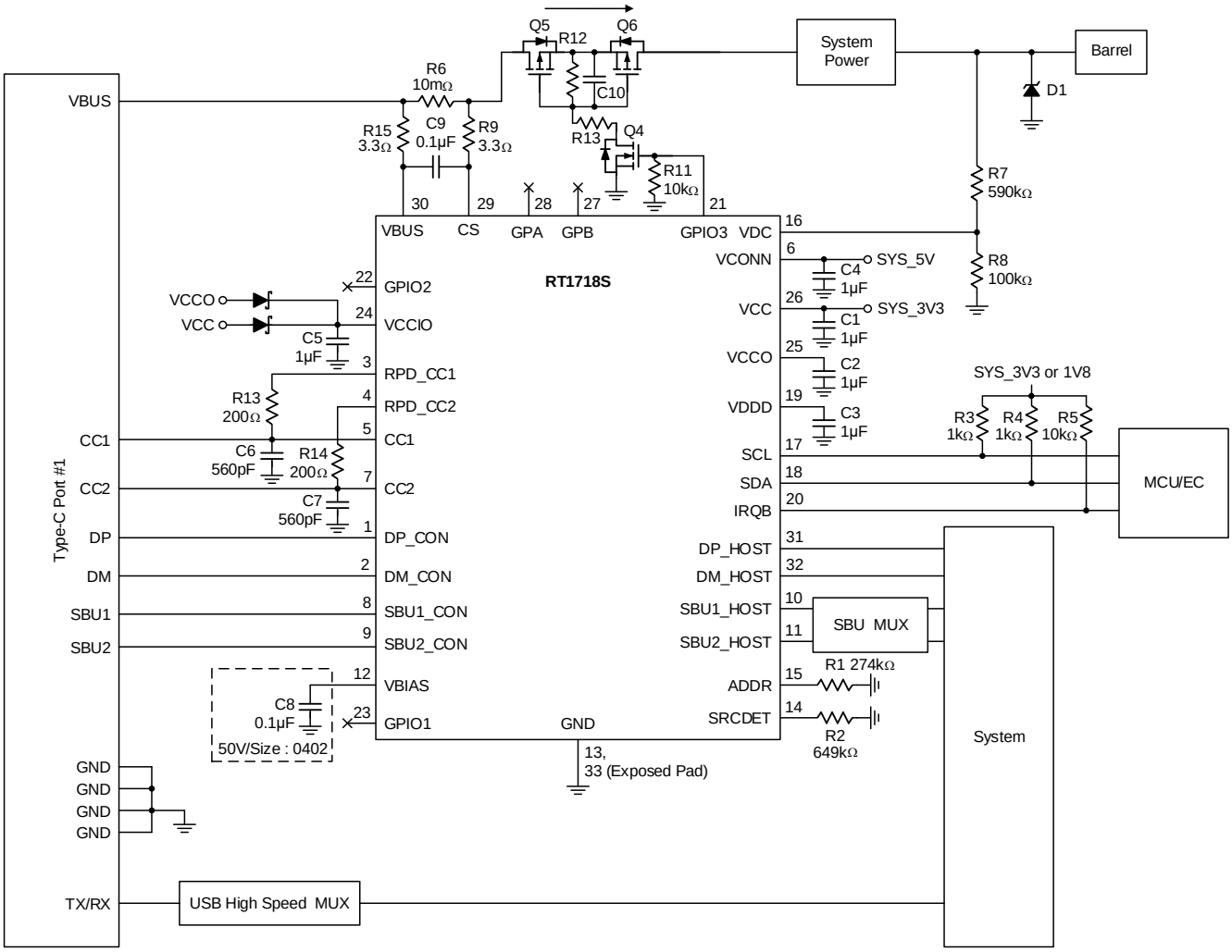
12 Typical Application Circuit

12.1 The RT1718S in Source Application (Source Only Port)



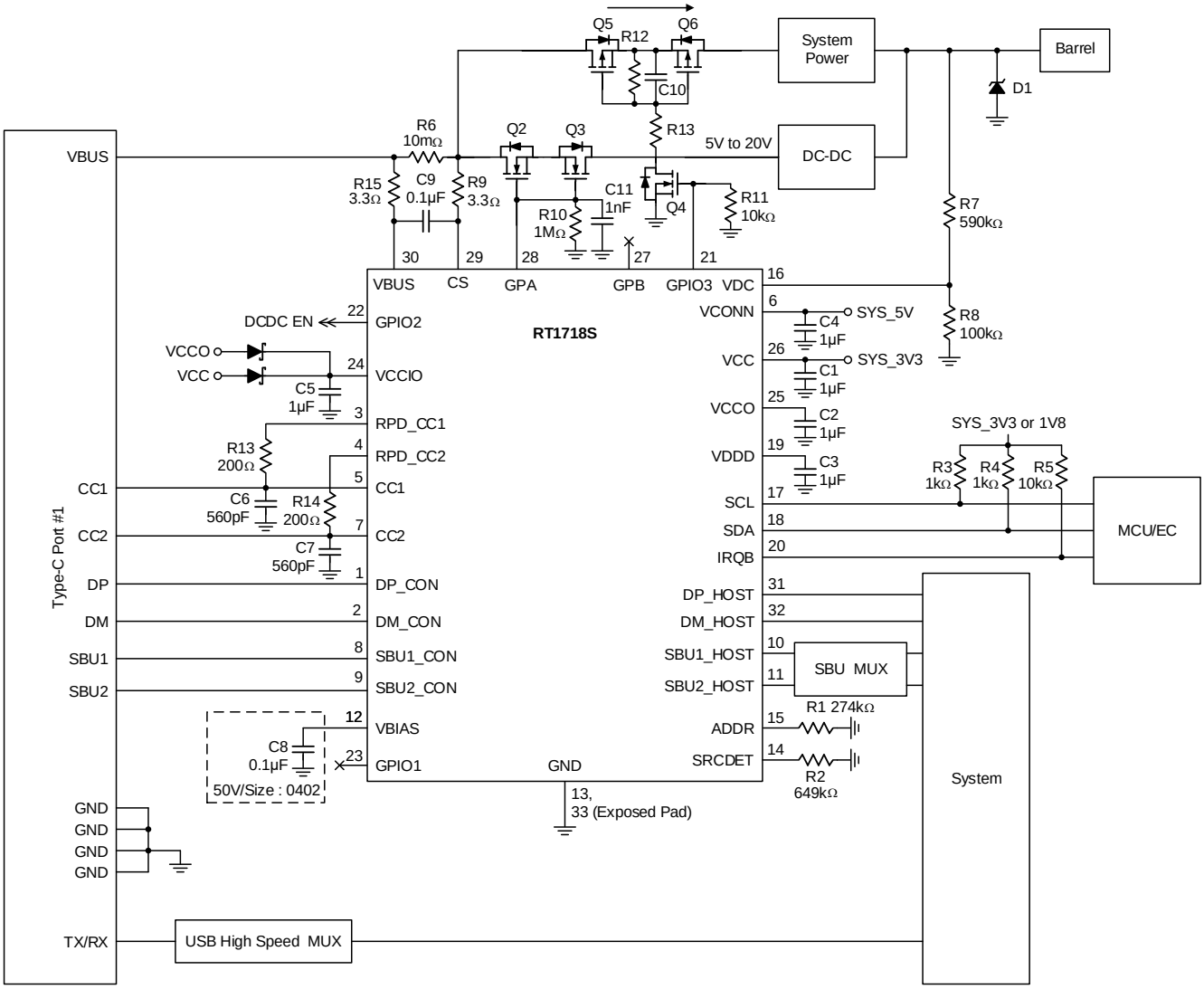
12.2 The RT1718S in Sink Application (Sink Only Port)

R12, R13, and C10 are for soft-on of Q5 and Q6. The values depend on the sink path for system.



12.3 The RT1718S in DRP Application (DRP Port, Source 5V to 20V Output)

R12, R13, C10 are for soft-on of Q5 and Q6. The values depend on the sink path for system.



The followings are the recommended components information.

Pin	Part Number	Description	Package	Manufacturer
VBIAS	0402B104K500CT	0.1µF/50V/X7R	0402	Walsin
Between VBUS and CS (R6)	RTT25R010FTE	RES SMD 0.01Ω 1% 1W 2512	2512	RALEC

13 Application Information

(Note 6)

13.1 USB_PD

The PD function of the RT1718S complies with USB Power Delivery spec 3.0 and Type-C Port Controller Interface spec Revision 1.0, Version 1.2. Some “Not support” functions are listed in the register table.

The RT1718S is also certified for PD 3.1 with TID = 10072.

13.2 Type-C Detection

The USB_PD implements multiple comparators which can be used by software to determine the state of the CC1 and CC2 pins. This status information provides the host processor with all of the information required to determine the attach and detach status of the cable. The USB_PD has three threshold comparators, which match the USB Type-C specification for the three charge current levels, which can be detected by a Type-C device. These comparators can automatically trigger interrupts when there is a state change.

13.3 Type-C Role

The RT1718S supports being a DRP (dual role port), SRC (source) only, or SNK (sink) only port. In DRP mode, the CC pins of the RT1718S will toggle between Rp and Rd periodically.

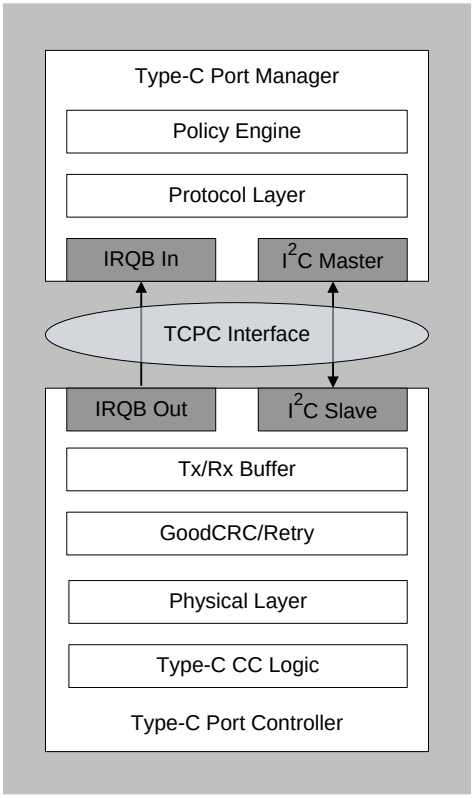
13.4 Dead Battery Mode

The RT1718S supports dead battery Rd by adding 200Ω resisters between CC1 (pin 5) and RPD_CC1 (pin 3) as well as CC2 (pin 7) and RPD_CC2 (pin 4). The CC pins of the RT1718S will present dead battery Rd, allowing a Source to recognize the Sink and provide VBUS. The dead battery system or UFP powered system with the RT1718S inside can be powered on from VBUS. The CC pins of the RT1718S will present real Rd (5.1kΩ) when the RT1718S exits shipping mode (0x8F[5] = 1b). Therefore, the RT1718S cannot recognize the source ability until it exits shipping mode.

13.5 Abbreviations

Term	Description
BMC	Biphase Mark Coding
TCPC	Type-C Port Controller
TCPCI	Type-C Port Controller Interface
TCPM	Type-C Port Manager

13.6 Type-C Port Controller (TCPC) Interface



The Type-C Port Controller Interface (TCPCI) is the interface between a Type-C Port Manager and a Type-C Port Controller.

13.7 The Controller Interface uses the I²C Protocol

- The TCPM is the only master on this I²C bus.
- The TCPC is a slave device on this I²C bus.
- Each Type-C port has its own unique I²C slave address. The TCPC shall have equal numbers of unique I²C slave addresses and supported Type-C ports.
- The TCPC supports Fast-mode bus speed.
- The TCPC has an open-drain output, active-low IRQB pin. This pin is used to indicate a change of state, where the IRQB pin is asserted when any Alert Bits are set.
- The TCPCI supports an I/O nominal voltage range of 1.8V and 3.3V.
- The TCPC can auto-increment the I²C internal register address of the last byte transferred during a read, independent of an ACK/NACK from the master.

13.8 I²C Interface

13.8.1 Slave Address

The RT1718S can be configured to four slave addresses by setting the resistance between ADDR (pin 15) and GND.

I²C Address in 7bit	Resistance between ADDR and GND (Unit: kΩ)
0x40	0
0x41	274
0x42	649
0x43	open

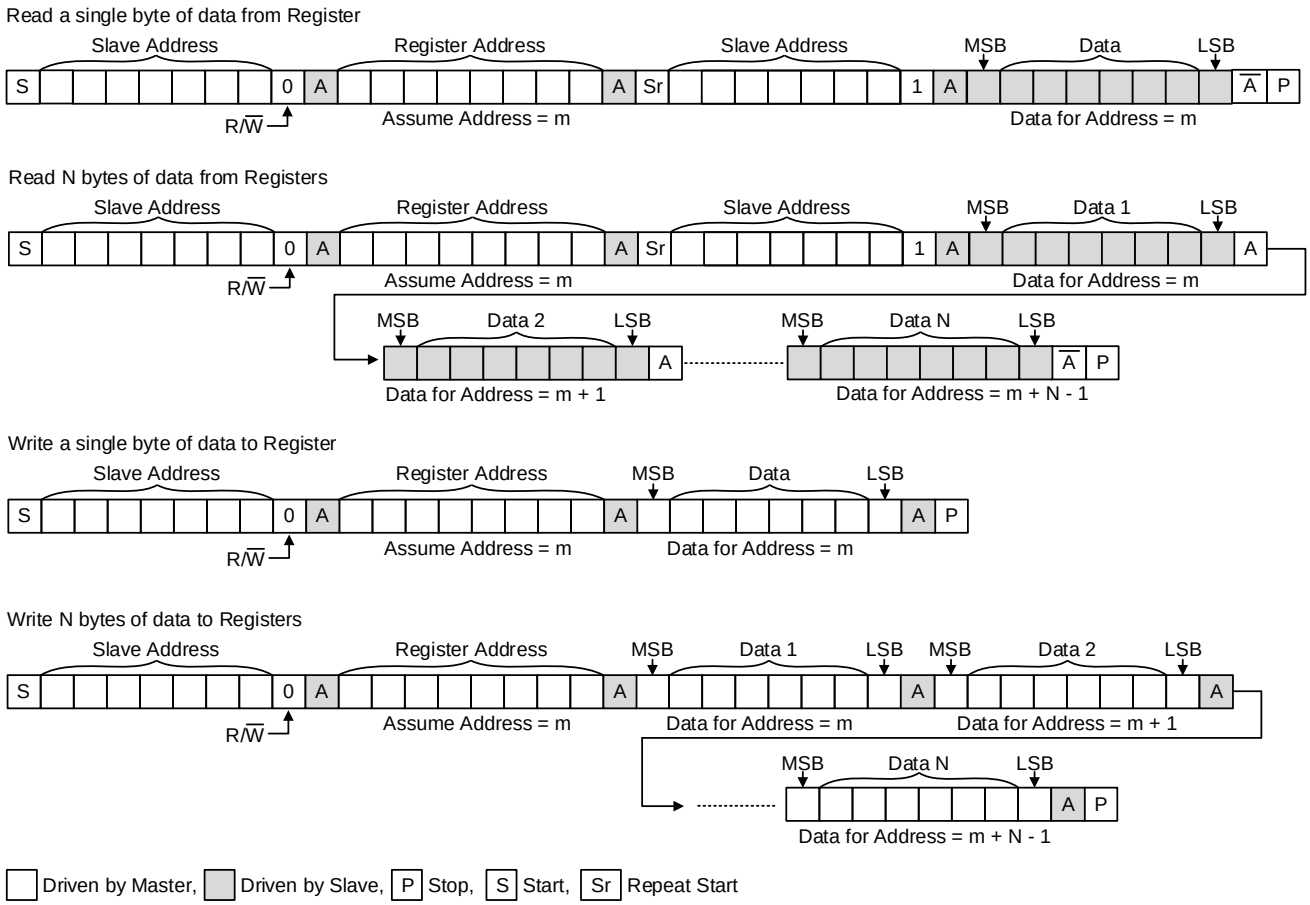
Taking the 0x43 in 7bit for example.

RT1718S I²C Slave Address			
MSB	**LSB**	**R/W bit**	**R/W**
100001	1	1/0	87/86

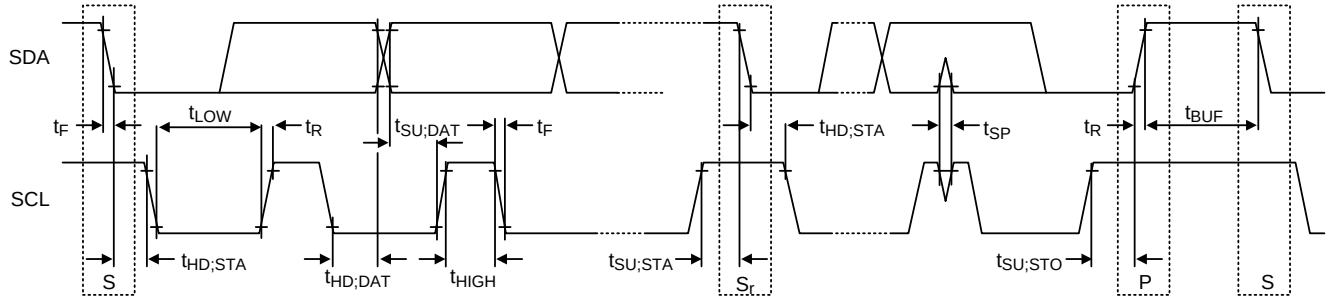
The I²C interface bus must be connected to a 1kΩ resistor to the power node and independently connected to the processor.

The I²C timing diagrams are listed below.

13.8.2 Read and Write Function



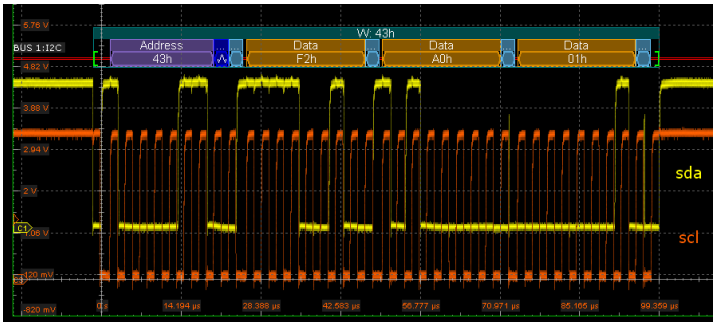
13.8.3 I^2C Waveform Information



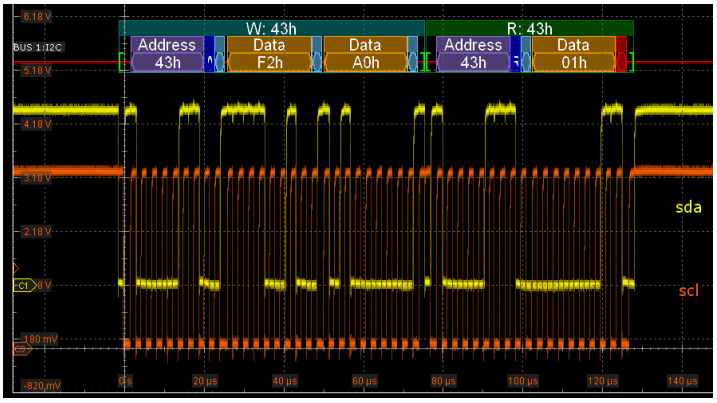
13.8.4 Operation for Page 2 of Register Map

If the registers in page 2 are read/written, 0xF2 has to be increased between slave address and the register address of page 2. The following are the example patterns of read and write for 0xA0 in page 2 with slave address 0x43.

- Example pattern to write 0xA0 = 01h in page 2.

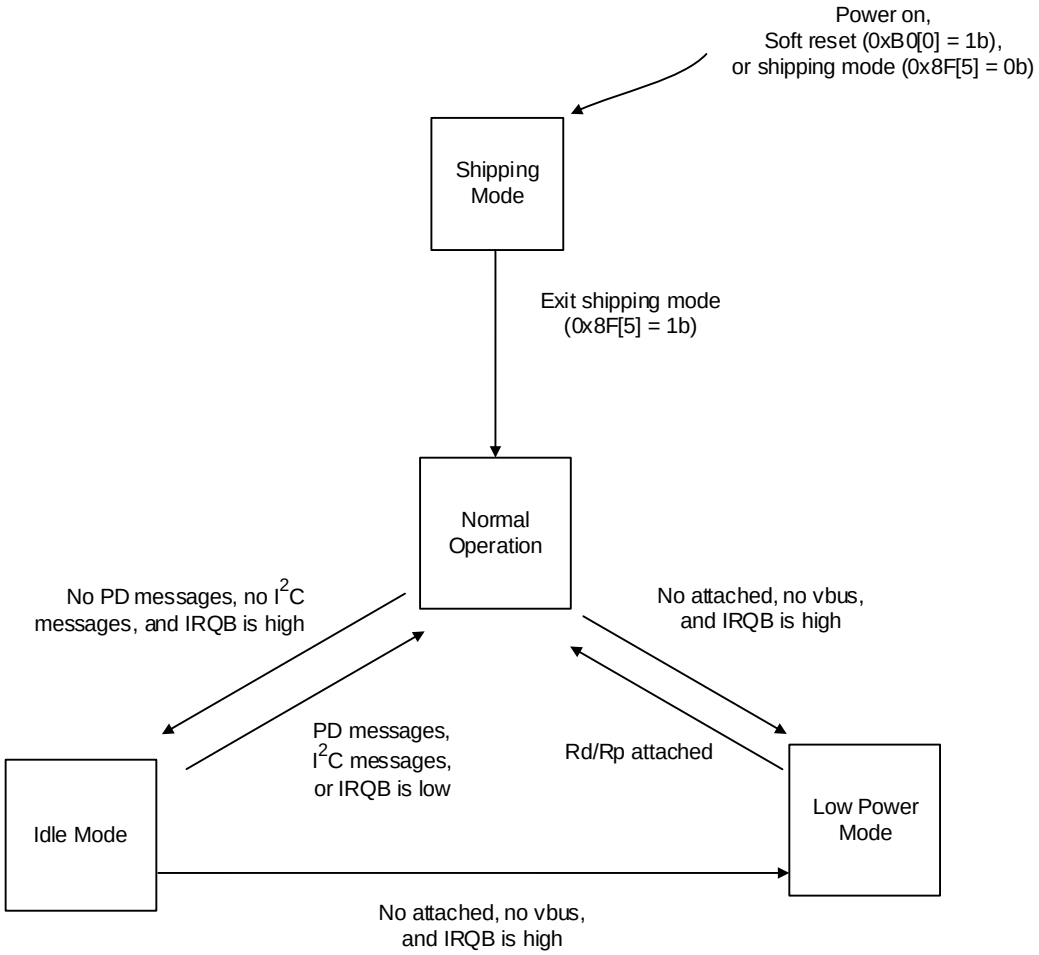


- Example pattern to read 0xA0 in page 2.



13.9 USB PD Power Mode

There are four power modes in the RT1718S during operation. Shipping mode after power on, normal operation after exiting shipping mode, auto idle mode mainly for attached, and auto low power mode for non-attached. The following diagram shows the power mode transition between each mode.



13.10 Shipping Mode

The RT1718S will be in shipping mode after power on. The RT1718S will not response to I^{2}C commands for 3ms after VCC > 2.7V.

In shipping mode, only the I^{2}C function work.

- 0x8F[5] = 1b:

The RT1718S will exit from shipping mode to normal operation. Do not send I^{2}C commands for 2ms after writing 0x8F[5] = 1b. During this 2ms, the RT1718S will not respond to I^{2}C commands.

- 0x8F[5] = 0b:

Writing 0x8F[5] = 0b to return the RT1718S to shipping mode.

Address	Length	Bit	Bit Name	Default	Type	Description
0x8F	1	5	SHIPPING_OFF	0	RW	0: Shipping mode 1: Non-shipping mode

13.11 Auto Idle Mode

When the auto idle function is enabled, auto idle mode timer starts to count if there is no RX or TX of PD commands, no I^{2}C commands, and the IRQB (pin 20) is high. if there is RX or TX of PD commands, I^{2}C commands, or the IRQB (pin 20) is low, auto idle mode timer will be reset. The RT1718S will enter idle mode automatically after the auto idle timer expires. In idle mode, only the 24MHz oscillator for RX of PD commands is off. However, if there is RX of PD commands transmitted from the port partner, the RT1718S can still catch the commands and inform the TCPM by setting IRQB low due to 0x10[2] = 1b.

The RT1718S will also exit from idle mode to normal operation when there is I^{2}C processing, PD commands, or IRQB is low.

- 0x8F[3] = 1b:

Auto idle mode is enabled.

- 0x8F[3] = 0b:

Auto idle mode is disabled. The RT1718S will be in normal operation if there is no other power-saving mode set.

Address	Length	Bit	Bit Name	Default	Type	Description
0x8F in Page 1	1	3	AUTOIDLE_EN	0	RW	The auto idle mode control 0: Auto enter idle mode disabled (default) 1: Auto enter idle mode enabled
	3	2:0	AUTOIDLE_TIMEOUT	000	RW	These bits can be used to set the time before entering into auto idle. The time setting is based on: (AUTOIDLE_TIMEOUT * 2 + 1) * 6.4ms 000: 6.4ms (default) 001: 19.2ms 010: 32ms …… 111: 96ms

13.12 Auto Low Power Mode

When auto low power function is enabled, auto low power timer starts to count if there is no attachment on CC, the vbus is not present (0x1E[2] = 0b), and the IRQB (pin 20) is high. If there is attachment on CC, the vbus is present (0x1E[2] = 0b), or the IRQB (pin 20) is low, auto low power timer will be reset. 0x90 at page 1 will be updated by 0xB8 in page1 when auto low power timer is expired. The main recommended updated bits in 0x90 are 0x90[3] and 0x90[0]. There are no RX and TX functions of PD when the RT1718S is in low power mode. The RT1718S will exit from low power mode to normal operation (0x90[3] = 0b) when there is Rd or Rp attachment. RX and TX functions of PD can be active again (0x90[0] = 1b) only when there are attach events except for single Ra attached.

- 0xF210[6] = 1b.
- 0xF210[5:4] is the setting for auto low power timer.
- 0xF210[2:0] = 000b:

Auto low power mode is disabled.

- 0xF210[2:0] = 101b:

Auto low power mode is enabled.

The recommended 0xB8 value is 1Ah.

- 0xB8[4] = 1b:

When the auto low power mode timer expires, 0x90[4] is updated to 0xB8[4] = 1b, and then the bandgap reference current is on in low power mode for VBUS detection.

- 0xB8[3] = 1b:

When the auto low power mode timer expires, 0x90[3] is updated to 0xB8[3] = 1b, and then the RT1718S enters low power mode.

- 0xB8[1] = 1b:

When the auto low power mode timer expires, 0x90[1] is updated to 0xB8[1] = 1b, and then VBUS detection is on.

- 0xB8[0] = 0b:

When the auto low power mode timer expires, 0x90[0] is updated to 0xB8[0] = 0b, and then the 24MHz oscillator is off.

Address	Bit	Bit Name	Default	Type	Description
0xB8 at Page 1	7:0	RTINI_REG90	00000000	RW	Update to 0x90 when auto low power timer is expired with 0xF210[2:0] = 101b.
0x10 at Page 2	5:4	AUTO_LPWR_ TIMEOUT	00	RW	These bits can be used to set the time before entering into auto low power. 00: 1.0s (default) 01: 1.5s 10: 2.0s 11: 2.5s
	2:0	AUTO_LPWR_EN	000	RW	For open source TCPM to enter low power mode when unattached, auto write the low power control register per the scenario Below: 000: Disable (default) 100: HW auto updates 0x90 to RTINI_REG90 when the auto low power timeout is reached. The auto low power timer is enabled when the TCPC is in normal mode with both CCx_Status opened, no IRQB event, and VBUS_PRESENT = 0. 101: HW auto updates 0x90 to RTINI_REG90 when the auto low power timeout is reached. The auto low power timer is enabled when the TCPC is in normal mode with both CCx_Status opened for Sink or CCx_Status has a single RA for Source, no IRQB event, and VBUS_PRESENT = 0. 110/111: Disable The other settings are reserved.

13.13 Soft Reset

All registers of the RT1718S can be reset to their default values by writing SOFT_RESET (0xB0[0]) as 1b, except for the SRCDET function. Refer to the SRCDET section for more detail information. The RT1718S will not response to the I^2C commands for 2ms after writing SOFT_RESET (0xB0[0]) as 1b.

Address	Bit	Bit Name	Default	Type	Description
0xB0	0	SOFT_RESET	0	W	When writing 1b to this bit, it will trigger a soft-reset event, and all register settings will reset to their default values.

13.14 Fast Role Swap (Initial Sink)

As an initial sink in FRS, here is the introduction to the settings.

- 0xCC[6] = 1b: Set FRS RX detection enabled.
- 0xCB[3:2]: Set the FRS RX detection threshold.

When the voltage level of the CC pin is lower than 0xCB[3:2] for 40μs, the INT_RX_FRS (0x98[6]) will be 1b. The RX_FRS (0x9F[6]) will be 1b only between the FRS signal received (0x98[6] = 0b→1b) and the voltage level of the CC pin being higher than 0xCB[3:2] again.

- 0xCC[3] = 1b: Set FRS VBUS detection enabled.
- 0xCC[2:0]: Set the FRS VBUS detection threshold.

When the voltage level of the VBUS pin is lower than 0xCC[2:0], the INT_VBUS_FRS_LOW (0x98[7]) will be 1b and the VBUS_RX_FRS_LOW (0x9F[7]) will be 0b. When the voltage level of the VBUS pin is higher than 0xCC[2:0] again, the VBUS_RX_FRS_LOW (0x9F[7]) will be 1b.

- 0xCE[3:0]: Set the reload condition of GPIO2, GPIO1, GPB, and GPB for FRS RX events.

For controlling the sink path, it is recommended to set as 0b. This means turning off the sink path right after the FRS signal is received.

For controlling the source path, it is recommended to set as 1b. This means turning on the source path after the FRS signal is received and VBUS is low enough.

Refer to GPA/B or GPIO1/2 for reload values setting.

Address	Bit	Bit Name	Default	Type	Description
0xCB	3:2	VREF_RX_FRS	10	RW	Fast role-swap detection threshold on CC pin 00: 0.48V 01: 0.50V 10: 0.52V (default) 11: 0.54V
0xCC	6	RX_FRS_EN	0	RW	Fast-role swap RX detection enable 0: Disable (default) 1: Enable
0xCC	4	FR_VBUS_SELECT	1	RW	FR_VBUS_FLAG is de-bounced or not. 0: Not de-bounce FR_VBUS_VALID 1: De-bounce FR_VBUS_VALID (default)
	3	VBUS_FRS_EN	0	RW	VBUS Fast Role-Swap detection enable 0: Disable (default) 1: Enable
	2:0	VREF_VBUS_FRS	000	RW	VBUS Fast Role-Swap detection threshold selection 000: 4.8V (default) 001: 4.9V 010: 5.0V 011: 5.1V 100: 5.2V 101: 5.3V 110: 5.4V 111: 5.5V
0xCE	3	FRS_RX_WAIT_GPIO2	0	RW	GPIO2 reload when receiving fast role swap event 0: Reload setting when receiving a fast role swap event (default) 1: Reload setting when receiving a fast role swap event and VBUS < VREF_VBUS_FRS
	2	FRS_RX_WAIT_GPIO1	0	RW	GPIO1 reload when receiving fast role swap event 0: Reload setting when receiving a fast role swap event (default) 1: Reload setting when receiving a fast role swap event and VBUS < VREF_VBUS_FRS
	1	FRS_RX_WAIT_GPB	0	RW	GPB reload when receiving fast role swap event 0: Reload setting when receiving a fast role swap event (default) 1: Reload setting when receiving a fast role swap event and VBUS < VREF_VBUS_FRS
	0	FRS_RX_WAIT_GPA	0	RW	GPA reload when receiving fast role swap event 0: Reload setting when receiving a fast role swap event (default) 1: Reload setting when receiving a fast role swap event and VBUS < VREF_VBUS_FRS
0x91	7	M_VBUS_FRS_LOW	0	RW	0: Interrupt masked (default) 1: Interrupt unmasked
	6	M_RX_FRS	0	RW	0: Interrupt masked (default) 1: Interrupt unmasked

Address	Bit	Bit Name	Default	Type	Description
0x98	7	INT_VBUS_FRS_LOW	0	WC	0: Cleared (default) 1: Fast Role Swap Vbus Valid Falling (< 4.75V)
	6	INT_RX_FRS	0	WC	0: Cleared (default) 1: Fast-role swap RX detection alert.
0x9F	7	VBUS_FRS_LOW	0	R	VBUS FRS voltage detection 0: VBUS < VREF_VBUS_FRS (default) 1: VBUS > VREF_VBUS_FRS
	6	RX_FRS	0	R	Fast-role swap RX detection alert. 0: CC > VREF_RX_FR (default) 1: CC < VREF_RX_FR

13.15 Gate Control

13.15.1 General Setting

The output voltage high level of GPA and GPB is up to VBUS + 4.5V and the low level is GND. GPA and GPB are recommended to control the paths for VBUS only. The charge pumps (0xEC[1:0]) of GPB and GPA default to being on after the RT1718S exits shipping mode. There is an option to disable the charge pump of GPB or GPA (0xEC[3:2]) when the RT1718S enters low power mode. When the RT1718S enters normal operation from low power mode, the status of the charge pump of GPB or GPA depends on 0xEC[1:0] and 0xDD. If 0xEC[5] = 1b or 0xEC[4] = 1b, GPB or GPA can be controlled by 0x23 and be updated due to VBUS fault events and FRS.

Address	Bit	Bit Name	Default	Type	Description
0xEC	5	GPB_VBUS_PATH_EN	1	RW	GPB setting (GPB_CTRL) auto reload with TCPC command, VBUS OV/OC/RC event, and FRS event 0: GPB setting (GPB_CTRL) will not auto reload 1: GPB setting (GPB_CTRL) will auto reload (default)
	4	GPA_VBUS_PATH_EN	1	RW	GPA setting (GPA_CTRL) auto reload with TCPC command, VBUS OV/OC/RC event, and FRS event 0: GPA setting (GPA_CTRL) will not auto reload 1: GPA setting (GPA_CTRL) will auto reload (default)
	3	VBUS_CPGPB_AUTO_OFF	1	RW	Auto disable VBUS charge pump for GPB when in low power mode 0: Not auto disable 1: Auto disable when in low power mode (default)
	2	VBUS_CPGPA_AUTO_OFF	1	RW	Auto disable VBUS charge pump for GPB when in low power mode 0: Not auto disable 1: Auto disable when in low power mode (default)
	1	VBUS_CPGPB_EN	1	RW	VBUS charge pump for GPB 0: Disable 1: Enable (default)
	0	VBUS_CPGPA_EN	1	RW	VBUS charge pump for GPA 0: Disable 1: Enable (default)

13.15.2 GPB/GPA Auto Reloaded

GPB and GPA can be controlled directly by writing to 0xDD with 0xEC[1:0] = 11b, regardless of what 0xEC[5:4] is. If 0xEC[5] = 1b, 0xDD[7:4] will be updated according to the relative events. If 0xEC[4] = 1b, 0xDD[3:0] will be updated according to the relevant events. 0xEC[5:4] = 11b in the following tables.

Writing 0x23 with	0xDD is updated by
44h (Disable Sink Vbus)	The value of 0xDE
55h (Sink Vbus)	The value of 0xDF
66h (Disable Source Vbus)	The value of 0xE0
77h (Source Vbus Default Voltage)	The value of 0xE1
88h (Source Vbus High Voltage)	The value of 0xE2

VBUS fault	0xDD is updated by
VBUS OCP1	The value of 0xE3
VBUS OCP2	The value of 0xE4
VBUS OCP3	The value of 0xE5
VBUS OVP	The value of 0xE6
VBUS RCP1/3	The value of 0xE7

FRS	0xDD is updated by
FRS signal received	The value of 0xE9

13.16 GPIO

13.16.1 General Setting

As output, the output voltage high level of GPIOx is up to VCCIO and the low level is GND. If 0xEC[7] = 1b or 0xEC[6] = 1b, GPIO2 or GPIO1 can be controlled by 0x23 and be updated due to FRS.

Address	Bit	Bit Name	Default	Type	Description
0xEC	7	GPIO2_VBUS_PATH_EN	0	RW	GPIO2 setting (GPIO2_OD_N/GPIO2_OE/GPIO2_O) auto reload with TCPC command and FRS event 0: GPIO2 setting (GPIO2_OD_N/GPIO2_OE/GPIO2_O) will not auto reload (default) 1: GPIO2 setting (GPIO2_OD_N/GPIO2_OE/GPIO2_O) will auto reload
	6	GPIO1_VBUS_PATH_EN	0	RW	GPIO1 setting (GPIO1_OD_N/GPIO1_OE/GPIO1_O) auto reload with TCPC command and FRS event 0: GPIO1 setting (GPIO1_OD_N/GPIO1_OE/GPIO1_O) will not auto reload (default) 1: GPIO1 setting (GPIO1_OD_N/GPIO1_OE/GPIO1_O) will auto reload

13.16.2 GPIO1/GPIO2 Auto Reloaded

GPIO1 and GPIO2 can be controlled directly by writing to 0xED and 0xEE, regardless of what 0xEC[7:6] is. If 0xEC[7] = 1b, 0xEE[3:1] will be updated according to the relative events. If 0xEC[6] = 1b, 0xED[3:1] will be updated according to the relevant events. 0xEC[7:6] = 11b in the following tables.

Writing 0x23 with	GPIO2: 0xEE[3:2] = 11b 0xEE[1] is updated by	GPIO1: 0xED[3:2] = 11b 0xED[1] is updated by
44h (Disable Sink Vbus)	0xEB[0]	0xEA[0]
55h (Sink Vbus)	0xEB[1]	0xEA[1]
66h (Disable Source Vbus)	0xEB[2]	0xEA[2]
77h (Source Vbus Default Voltage)	0xEB[3]	0xEA[3]
88h (Source Vbus High Voltage)	0xEB[4]	0xEA[4]

FRS	GPIO2: 0xEE[3:2] = 11b 0xEE[1] is updated by	GPIO1: 0xED[3:2] = 11b 0xED[1] is updated by
FRS signal received	0xEB[6]	0xEA[6]

13.17 VBUS OCP

There are three VBUS OCP functions in RT1718S. The sensing current is through the sensing resistor between the CS pin (pin 29) and VBUS pin (pin 30). The current direction is from CS to VBUS. The resistance should be 10mΩ.

13.17.1 VBUS OCP1

If VBUS_OC is enabled (0x1B[2] = 0b) and the VBUS current through the sensing resistor exceeds the threshold (0x16 in page 2) for the debounce time (0x19 in page 2), the Vbus_OC fault status (0x1F[3]) will be set to 1b, and GPA as well as GPB (0xDD) will be updated by Fault_OC1_VBUS_CTRL (0xE3).

For example, if the VBUS OCP1 is designed to trigger at 3A for a duration of 400ms, then 0x16 in page 2 should be set to 1Ch and 0x19 in page 2 should be set to 28h or 88h.

Address	Bit	Bit Name	Default	Type	Description
0x1B	2	DIS_VBUS_OC	0	RW	0: VBUS OCP1 enabled. (default) 1: VBUS OCP1 disabled
0x16 in Page 2	6:0	VBUS_OCP1_SEL	0100010	RW	0000000: 0.2A 0000001: 0.3A … 0100010: 3.6A (default) … 1111111: 12.9A

Address	Bit	Bit Name	Default	Type	Description
0x19 in Page 2	7	VBUS_OCP1_50MS	0	RW	0b: 10ms/step (default) 1b: 50ms/step
	6:0	VBUS_OCP1_TIME	1010000	RW	0000000: 0 step 0000001: 1 step … 1010000: 80 steps (default) … 1111111: 127 steps
0x15	3	M_VBUS_OC	1	RW	0: Interrupt masked 1: Interrupt unmasked (default)
0x1F	3	VBUS_OC	0	RW	0: Not in an OC protection state (default) 1: Overcurrent fault latched

13.17.2 VBUS OCP2

If VBUS _OC2 is enabled (0x14[1] in page 2 as 1b) and the VBUS current through the sensing resistor exceeds the threshold (0x17 in page 2) for the debounce time (0x1A in page 2), INT_VBUS_OC2 (0xA9[0]) will be set to 1b, and GPA as well as GPB (0xDD) will be updated by Fault_OC2_VBUS_CTRL (0xE4).

For example, if the VBUS OCP2 is designed to trigger at 6A for a duration of 50ms, then 0x17 in page 2 should be set to 3Ah and 0x1A in page 2 should be set to 05h or 81h.

Address	Bit	Bit Name	Default	Type	Description
0x14 in Page 2	1	VBUS_OC2_EN	0	RW	0: VBUSOCP2 disabled (default) 1: VBUSOCP2 enabled
0x17 in page2	6:0	VBUS_OCP2_SEL	0100010	RW	0000000: 0.2A 0000001: 0.3A … 0100010: 3.6A (default) … 1111111: 12.9A
0x1A in page2	7	VBUS_OCP2_50MS	0	RW	0b: 10ms/step (default) 1b: 50ms/step
	6:0	VBUS_OCP2_TIME	1010000	RW	0000000: 0 step 0000001: 1 step … 1010000: 80 steps … 1111111: 127 steps
0xA7	0	MASK_VBUS_OC2	0	RW	0: Interrupt masked (default) 1: Interrupt unmasked
0xA9	0	INT_VBUS_OC2	0	RW	0: No action (default) 1: VBUS OCP2 occurred Note: This bit cannot be cleared until VBUS OCP2 events disappear.

13.17.3 VBUS OCP3

If VBUS_OC3 is enabled (0x14[4] in page 2 as 1b) and the VBUS current through the sensing resistor exceeds the threshold (0x18 in page 2), INT_VBUS_OC3 (0xA9[1]) will be set to 1b, and GPA as well as GPB (0xDD) will be updated by Fault_OC3_VBUS_CTRL (0xE5).

Address	Bit	Bit Name	Default	Type	Description
0x14 in Page 2	4	VBUS_OC3_EN	0	RW	0: VBUS OCP3 disabled (default) 1: VBUS OCP3 enabled
0x18 in Page 2	1:0	VBUS_OCP3_SEL	10	RW	00: 7.25A 01: 9A 10: 12A (default) 11: 15A
0xA7	1	MASK_VBUS_OC3	0	RW	0: Interrupt masked (default) 1: Interrupt unmasked
0xA9	1	INT_VBUS_OC3	0	RW	0: No action (default) 1: VBUS OCP3 occurred Note: This bit cannot be cleared until VBUS OCP3 events disappear.

13.18 VBUS OVP

If VBUS_OV enabled (0x1B[1] = 0b) and the VBUS is higher than the threshold (0x13 in page 2) for the debounce time (0x13[6] in page 2), Vbus_OV of fault status (0x1F[2]) will be set to 1b, and GPA as well as GPB (0xDD) will be updated by Fault_OV_VBUS_CTRL (0xE6). For example, if the VBUS is 15V and the VBUS OVP is designed to trigger at 20% higher than VBUS, then 0x13 in page 2 should be set to 7Ah. No debounce for VBUS OVP is recommended (0x13[6] in page 2 should be set to 1b).

Address	Bit	Bit Name	Default	Type	Description
0x1B	1	DIS_VBUS_OV	0	RW	0: VBUS OVP enabled (default) 1: VBUS OVP disabled
0x13 in Page 2	6	VBUS_OVP_NODEB	0	RW	0: 25μs deglitch for VBUS OVP (default) 1: No deglitch for VBUS OVP
	5:4	VBUS_OVP_SEL	10	RW	VBUS overvoltage protection level percentage. OVP = VBUS_VOL_SEL * (100 + X)% 00: X = 5 01: X = 10 10: X = 15 (default) 11: X = 20
	3:0	VBUS_VOL_SEL	1000	RW	VBUS voltage range 0000: 5V 0001: 6V …… 1000: 13V (default) …… 1110: 19V 1111: 20V

Address	Bit	Bit Name	Default	Type	Description
0x15	2	M_VBUS_OV	1	RW	0: Interrupt masked 1: Interrupt unmasked (default)
0x1F	2	VBUS_OV	0	RW	0: Not in an OV protection state (default) 1: Overvoltage fault latched

13.19 VCONN

13.19.1 VCONN OCP

If VCONN_EN (0x1C[0] = 1b) and VCONN_OC are enabled (0x1B[0] = 0b) and the VCONN current (from VCONN to the CC pin) exceeds the threshold (0x8C[7:5]), VCONN_OC of fault status (0x1F[1]) will be set to 1b, and there will be no VCONN output.

Address	Bit	Bit Name	Default	Type	Description
0x1B	0	DIS_VCONN_OC	0	RW	0: Fault detection circuit enabled (default) 1: Fault detection circuit disabled
0x8C	7:5	VCONN_OCP_SEL	010	RW	PD_VCONN OCP level selection 000: 100mA 001: 200mA 010: 300mA (default) 011: 400mA 100: 500mA 101: 600mA 110: 700mA 111: 800mA
0x15	1	M_VCONN_OC	1	RW	0: Interrupt masked 1: Interrupt unmasked (default)
0x1F	1	VCONN_OC	0	RW	0: No fault detected (default) 1: VCONN overcurrent fault latched

13.19.2 VCONN OVP

If VCONN_OVP_EN_CC1 is enabled (0x8B[7] = 1b) and the voltage at CC1 is higher than 5.75V (typical), VCONN_OV_CC1 (0xA0[0]) and INT_VCONN_OV_ CC1 (0x99[0]) will be set to 1b, and there will be no VCONN output. VCONN_OV_CC1 becomes 0b when the voltage at CC1 is lower than 5.7V. If VCONN_OVP_EN_CC2 is enabled (0x8B[6] = 1b) and the voltage at CC2 is higher than 5.75V (typical), VCONN_OV_CC2 (0xA0[1]) and INT_VCONN_OV_CC2 (0x99[1]) will be set to 1b, and there will be no VCONN output. VCONN_OV_CC2 becomes 0b when the voltage at CC2 is lower than 5.7V.

Address	Bit	Bit Name	Default	Type	Description
0x8B	7	VCONN_OVP_EN_CC1	0	RW	Enable CC1 OVP. The OVP threshold is 5.75V at CC1. 0: Disable (default) 1: Enable
	6	VCONN_OVP_EN_CC2	0	RW	Enable CC2 OVP. The OVP threshold is 5.75V at CC2. 0: Disable (default) 1: Enable
0x92	1	M_VCONN_OV_CC2	0	RW	0: Interrupt masked (default) 1: Interrupt unmasked
	0	M_VCONN_OV_CC1	0	RW	0: Interrupt masked (default) 1: Interrupt unmasked
0x99	1	INT_VCONN_OV_CC2	0	RW	0: Cleared (default) 1: CC2 OVP event is detected.
	0	INT_VCONN_OV_CC1	0	RW	0: Cleared (default) 1: CC1 OVP event is detected.
0xA0	1	VCONN_OV_CC2	0	R	0: CC2 voltage is lower than 5.7V. (default) 1: CC2 voltage is higher than 5.75V. Note: This bit works when VCONN_OVP_EN_CC2 is enabled.
	0	VCONN_OV_CC1	0	R	0: CC1 voltage is lower than 5.7V. (default) 1: CC1 voltage is higher than 5.75V. Note: This bit works when VCONN_OVP_EN_CC1 is enabled.

13.19.3 VCONN Reverse Voltage Protection (RVP)

If VCONN_RVP_EN is enabled (0x8B[3] = 1b) and the voltage at CC (depending on 0x19[0]) is higher than VCONN by the voltage specified in (0x8B[2]), VCONN_RVP (0xA0[2]) and INT_VCONN_RVP (0x99[2]) will be set to 1b, and there is no VCONN output. VCONN_RVP becomes 0b when the voltage at CC is lower than VCONN by 50mV.

Address	Bit	Bit Name	Default	Type	Description
0x8B	5:4	VCONN_SHT_GND_TIMER	10	RW	When VCONN_EN = 1 (0x1E[0] = 1b), VCONN_SHT_GND will be set to 1 (0xA0[5] = 1b) if VCONN_PRESENT is always 0 and lasts for VCONN_SHT_GND_TIMER. 00: 0.5ms 01: 0.75ms 10: 1ms (default) 11: 3ms
	0	VCONN_SOFTEND_TIMER	0	RW	The time for which VCONN current limit is enabled after VCONN EN (0x1C[0] = 1b) 0: 3ms (default) 1: 5ms

Address	Bit	Bit Name	Default	Type	Description
0x92	5	M_VCONN_SHT_GND	0	RW	0: Interrupt masked (default) 1: Interrupt unmasked
0x99	5	INT_VCONN_SHT_GND	0	RW	0: Cleared (default) 1: VCONN RVP event is detected.
0xA0	5	VCONN_SHT_GND	0	R	VCONN-short-to-GND means VCONN at CC is not higher than 2.4V after VCONN_SHT_GND_TIMER when VCONN_EN is enabled. 0: No VCONN short to GND (default) 1: VCONN short to GND

13.19.4 VCONN Short to GND

INT_VCONN_SHT_GND (0x99[5]) will be set to 1b and there will be no VCONN output if the voltage at CC (depending on 0x19[0]) is lower than VCONN present (2.4V) with the timeout of VCONN_SHT_GND_TIMER (0x8B[5:4]), which started from VCONN_EN = 1b. Even if the voltage at CC (depending on 0x19[0]) is higher than VCONN present (2.4V) with the timeout of VCONN_SHT_GND_TIMER (0x8B[5:4]), INT_VCONN_SHT_GND (0x99[5]) will still be set to 1b, and there will be no VCONN output if the voltage at CC (depending on 0x19[0]) is lower than VCONN present (2.4V) with the timeout of VCONN_SOFTEND_TIMER (0x8B[0]), which starts from VCONN_EN = 1b.

Address	Bit	Bit Name	Default	Type	Description
0x8B	5:4	VCONN_SHT_GND_TIMER	10	RW	When VCONN_EN = 1 (0x1E[0] = 1b), VCONN_SHT_GND will be set to 1 (0xA0[5] = 1b) if VCONN_PRESENT is always 0 and lasts for VCONN_SHT_GND_TIMER. 00: 0.5ms 01: 0.75ms 10: 1ms (default) 11: 3ms
	0	VCONN_SOFTEND_TIMER	0	RW	The time for which VCONN current limit is enabled after VCONN EN (0x1C[0] = 1b.) 0: 3ms (default) 1: 5ms
0x92	5	M_VCONN_SHT_GND	0	RW	0: Interrupt masked (default) 1: Interrupt unmasked
0x99	5	INT_VCONN_SHT_GND	0	RW	0: Cleared (default) 1: VCONN pre-short to ground
0xA0	5	VCONN_SHT_GND	0	R	VCONN-short-to-GND means VCONN at CC is not higher than 2.4V after VCONN_SHT_GND_TIMER when VCONN_EN is enabled. 0: No VCONN short to GND (default) 1: VCONN short to GND

13.19.5 VCONN UVP

INT_VCONN_UVP (0x99[4]) will be set to 1b and there will be no VCONN output if the voltage at CC (depending on 0x19[0]) is between 2.4V and VCONN_UVP_SEL (0x8A[5]) with the timeout of VCONN_SOFTEND_TIMER (0x8B[0]), which starts from VCONN_EN = 1b. VCONN output is successful if the voltage at CC is higher than VCONN_UVP_SEL (0x8A[5]) with the timeout of VCONN_SOFTEND_TIMER (0x8B[0]). After that, INT_VCONN_UVP (0x99[4]) will be set to 1b, and there will be no VCONN output if the voltage at CC is lower than VCONN_UVP_SEL (0x8A[5]).

Address	Bit	Bit Name	Default	Type	Description
0x8A	5	VCONN_UVP_SEL	0	RW	VCONN UVP level selection 0: 2.7V (default) 1: 2.4V
0x8B	0	VCONN_SOFTEND_TIMER	0	RW	The time for which VCONN current limit is enabled after VCONN EN (0x1C[0] = 1b). 0: 3ms (default) 1: 5ms
0x92	4	M_VCONN_UVP	0	RW	0: Interrupt masked (default) 1: Interrupt unmasked
0x99	4	INT_VCONN_UVP	0	RW	0: Cleared (default) 1: VCONN voltage less than VCONN_INVALID (2.7V) when VCONN_UVP_SEL = 0 (0x8A[5]), or VCONN voltage less than VCONN_PRESENT (2.4V) when VCONN_UVP_SEL = 1 (0x8A[5])
0xA0	4	VCONN_UVP	0	R	VCONN undervoltage protect 0: VCONN voltage at CC is higher than VCONN_INVALID (2.7V) when VCONN_UVP_SEL = 0 (0x8A[5]), or VCONN voltage is higher than VCONN_PRESENT (2.4V) when VCONN_UVP_SEL = 1 (0x8A[5]) (default) 1: VCONN voltage at CC is less than VCONN_INVALID(2.7V) when VCONN_UVP_SEL = 0 (0x8A[5]), or VCONN voltage is less than VCONN_PRESENT (2.4V) when VCONN_UVP_SEL = 1 (0x8A[5])

13.20 SBU and DPDM Switches

13.20.1 SBU and DPDM Switches Control

SBU and DPDM switches are on and the OVP function is on as VCC powers on. To control the DP/DM Switch and SBU Switch, the RT1718S must be in Non-SHIPPING Mode (0x8F[5] = 1b).

To turn on SBU switches, the SBU switches OVP source must be on (0xF23A[7] = 1b). SBU2 switch and SBU1 switch can be controlled independently (0xF23A[3] for SBU2 and 0xF23A[2] for SBU1).

To turn on DPDM switches, the DPDM switches OVP source must be on (0xF23A[6] = 1b). DM switch and DP switch can be controlled independently (0xF23A[1] for DM and 0xF23A[0] for DP).

Addr	Length	RegName	Bit	BitName	Default	Type	Description
0x3A in Page 2	1	SBU_CTRL_01	7	SBU_VIEN	1	RW	SBU protection VI source enable 0: Disable 1: Enable (default)
			6	DPDM_VIEN	1	RW	DPDM protection VI source enable 0: Disable 1: Enable (default)
			5:4	Reserved	00	R	Reserved
			3	SBU2_SWEN	1	RW	SBU2 switch enable 0: Disable 1: Enable (default)
			2	SBU1_SWEN	1	RW	SBU1 switch enable 0: Disable 1: Enable (default)
			1	DM_SWEN	1	RW	DM switch enable 0: Disable 1: Enable (default)
			0	DP_SWEN	1	RW	DP switch enable 0: Disable 1: Enable (default)

13.20.2 4-Channels USB and SBU Switch Input Overvoltage Protection

The RT1718S has 4-channels of short-to-VBUS overvoltage protection for the DP, DM, SBU1, and SBU2 pins of the USB Type-C receptacle via an internal OVP level. When the voltage at DP_CON, DM_COM, SBU1_CON, and SBU2_CON exceeds the OVP level, the RT1718S will ultra-fast turn off internal switches around in approximately 60ns to prevent the high input voltage from damaging the end system. When the DPDM/SBU voltage returns to the normal operating voltage range with hysteresis of 60mV, the switch will turn on.

The switch turned off by OVP will recover to being on after the recovery time (0xF23C[5:4].) As the recovery time expires and there is no OV fault at the switch, the switch will turn on automatically. The recovery time can be started at the rising or falling edge of the OV event (0xF23C[3]).

If any one of the channel voltages exceeds the OVP threshold, the channel switch will be turned off, and the status of the other switches depend on the register setting 0xF23C[2:0].

Addr	Length	RegName	Bit	BitName	Default	Type	Description
0x3C in Page 2	1	SBU_ CTRL_03	5:4	SBUDPDM_REC _TIME	00	RW	DPDM OVP recovery time 00: 400μs (default) 01: 600μs 10: 800μs 11: 1000μs Note: ±8μs
			3	SBUDPDM_REC _TYPE	0	RW	SBU OVP recovery type select 0: Recovery time starts at OV rising (default) 1: Recovery time starts at OV falling
			2	VCONN_OV_ OFF	0	RW	Switch off when VCONN OV 0: Turn off VCONN (default) 1: Turn off SBU1/SBU2/DP/DM/VC ONN
			1	DPDM_OV_OFF	0	RW	Switch off when DPDM OV 0: Turn off DP/DM (default) 1: Turn off SBU1/SBU2/DP/DM/VC ONN
			0	SBU_OV_OFF	0	RW	Switch off when SBU OV 0: Turn off SBU1/SBU2 (default) 1: Turn off SBU1/SBU2/DP/DM/VC ONN

The OVP status and switch status can be checked in register 0xF23D. If one of switch OVP status (0xF23D[7:4]) changes, the INT_SBUDPDM_SW will be set to 1b (0x9D[2] = 1b).

Addr	Length	RegName	Bit	BitName	Default	Type	Description
0x3D in Page 2	1	SBUDPDM_OV_STS	7	SBU2_OV_FLAG	0	R	SBU2 OVP status 0: No OVP occurs (default) 1: OVP occurs
			6	SBU1_OV_FLAG	0	R	SBU1 OVP status 0: No OVP occurs (default) 1: OVP occurs
			5	DM_OV_FLAG	0	R	DM OVP status 0: No OVP occurs (default) 1: OVP occurs
			4	DP_OV_FLAG	0	R	DP OVP status 0: No OVP occurs (default) 1: OVP occurs
			3	STS_SBU2_SWEN	0	R	SBU2 switch status 0: Switch off (default) 1: Switch on
			2	STS_SBU1_SWEN	0	R	SBU1 switch status 0: Switch off (default) 1: Switch on
			1	STS_DM_SWEN	0	R	DM switch status 0: Switch off (default) 1: Switch on
			0	STS_DP_SWEN	0	R	DP switch status 0: Switch off (default) 1: Switch on
0x96	1	RT_MASK6	2	M_SBUDPDM_SW	0	RW	0: Interrupt masked (default) 1: Interrupt unmasked
0x9D	1	RT_INT6	2	INT_SBUDPDM_SW	0	RW	0: Cleared (default) 1: SBU/DPDM switch status change

The OVP threshold range of the SBU switch is from 3.6V to 4.5V, which can be set at register 0xF23F[7:6]. It is recommended to set the OVP threshold of the SBU switch to 4.5V (0xF23F[7:6] = 11b) for better compliance. The OVP threshold of DPDM switches is 4.5V.

Addr	Length	RegName	Bit	BitName	Default	Type	Description
0x3F in Page 2	1	SBU_CTRL_04	7:6	SBU_OV_SEL	10	RW	SBU1/SBU2 OVP level selection 00: 3.6V 01: 3.7V 10: 3.8V (default) 11: 4.5V

13.21 Source Detection

The source detection function is used in UFP-powered applications. The GPIO3 (for sink path) will be high (0xEF = 0Eh) if the Rp level is 1.5A or 3A. The setting is according to the resistance on SRCDET (pin 14). The setting status is reported in SRCDET_SETTING (0xF2C1[5:4]). For the source detection function, the power of VCCIO (pin 24) is recommended to be from VCCO and VCC as shown in sink application circuit. If the RT1718S is soft-reset (0xB0[0] = 1b) during general operation after power on, the GPIO3 setting (0xEF) and the driving ability of GPIO3 (0xF2C0[5:4]) will not reset by setting GPIO3_SOFT_RSTN_EN (0xF2C1[1] = 0b). The source detection function can be disabled in SRCDET_CTRL_EN (0xF2C1[0] = 0b) even if the setting on SRCDET (pin 14) is enabled.

Resistance between SRCDET and GND (Unit: kΩ)	Function	0xF2C1[5:4]
0	SRCDET is disabled	00b
274	GPIO3 is high if a 1.5A or 3A Rp is attached	01b
649	GPIO3 is high if a 3A Rp is attached	10b
open	Disabled	00b

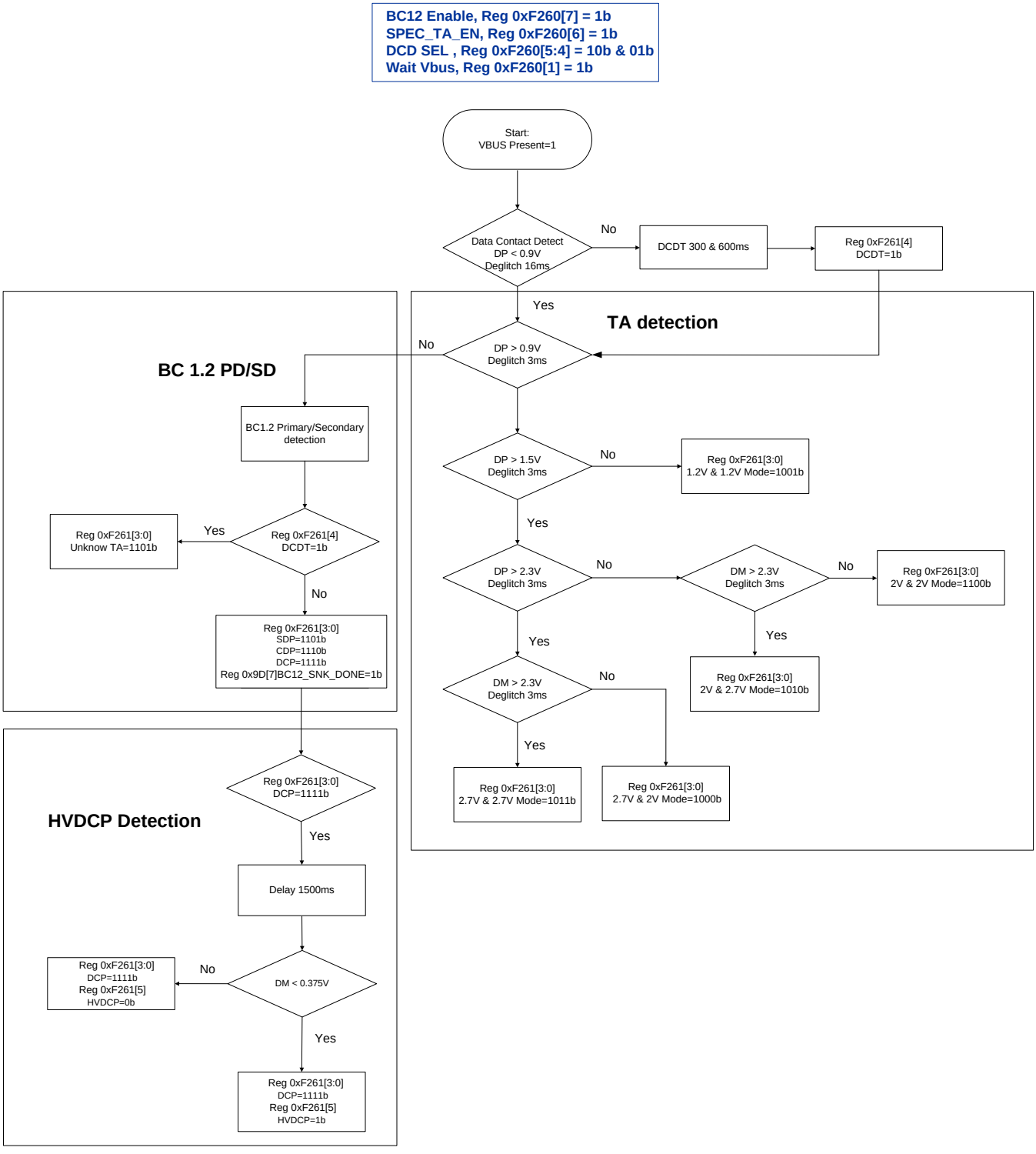
Addr	Length	Bit	BitName	Default	Type	Description
0xC1 in Page 2	1	5:4	SRCDET_SETTING	00	R	SRCDET setting 00: No SRCDET function (default) 01: Check CC for 1.5A 10: Check CC for 3.0A 11: Reserved
		1	GPIO3_SOFT_RSTN_EN	1	RW	GPIO3_SOFT_RSTN_EN When a soft reset is triggered, REG 0xEF[3:1] (GPIO3_OD_N, GPIO3_OE, GPIO3_O) and RT2_REG 0xC0[5:4] GPIO3_DRV will be reset. 0: Disable 1: Enable (default)
		0	SRCDET_CTRL_EN	1	RW	SRCDET_CTRL_EN Turn on VBUS (GPIO3) when a special Rp level is attached, depending on the SRCDET PIN 0: Disable 1: Enable (default)

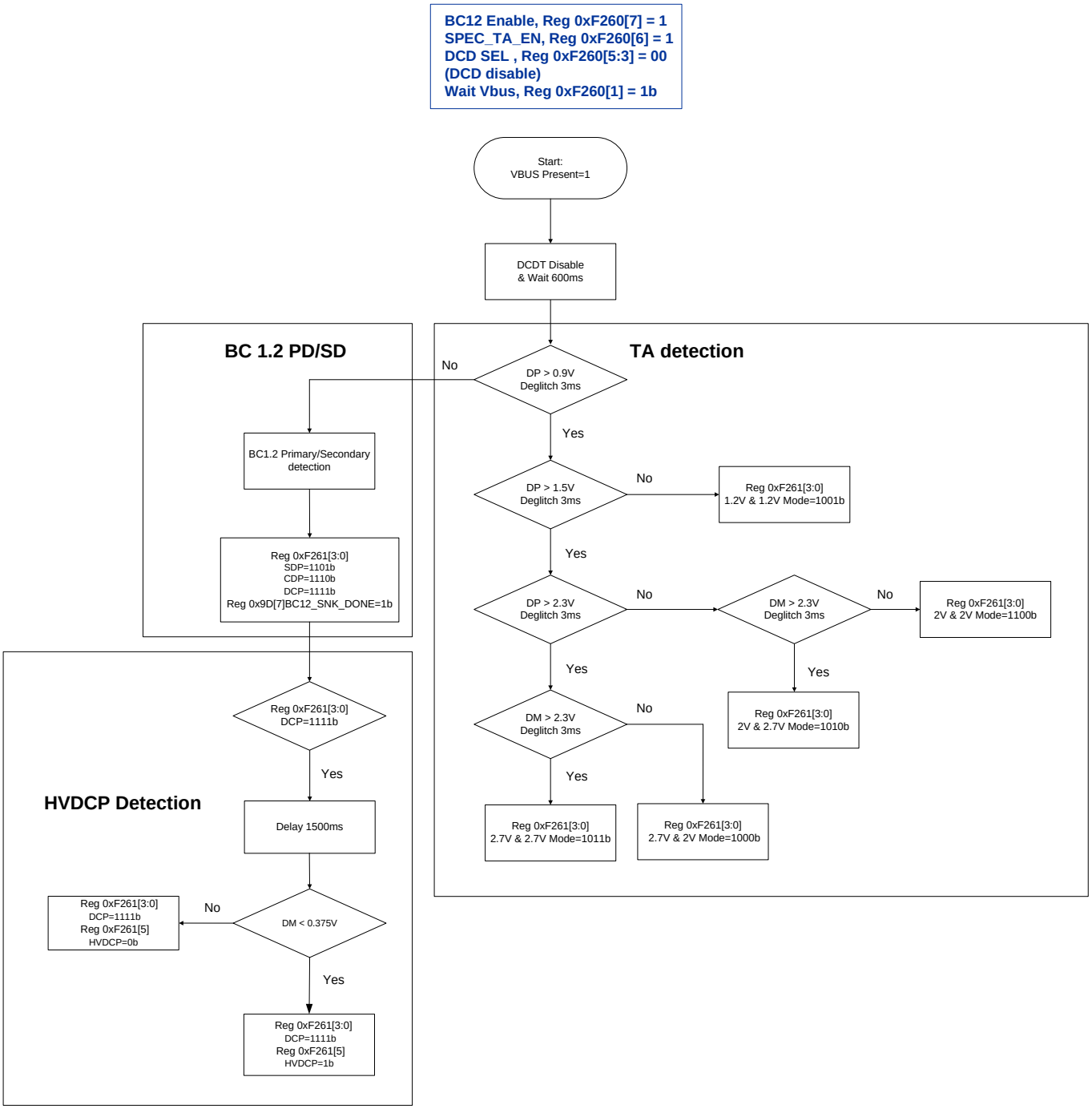
13.22 BC1.2 General Description

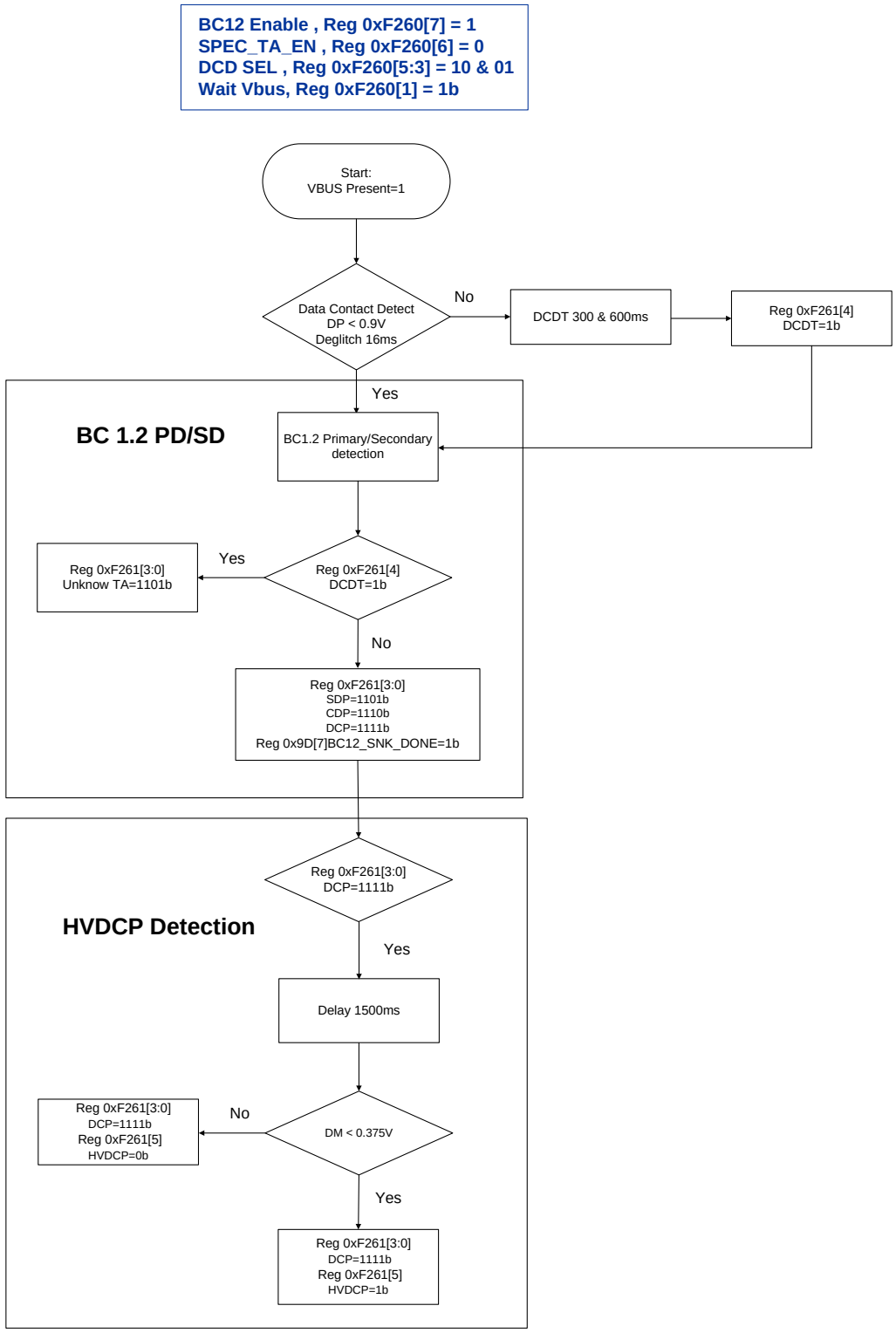
The BC1.2 specification defines the mechanisms to permit USB devices to draw current higher than standard USB current: 900mA for USB 3.0 and 500mA for USB 2.0. According to the BC1.2 spec, the devices can draw up to 1.5 A of current. The detection and advertisement of the higher current capable port are through USB2.0 D+ and D- lines upon connection. There are three charging ports defined in the BC1.2 spec: Dedicated Charging Port (DCP), Charging Downstream Port (CDP), and Standard Downstream Port (SDP). The RT1718S supports both portable device role (sink role) and downstream port or charging downstream port (source role). The BC1.2 function can work only with DPDM switches on (0xF23A[6] = 1b and 0xF23A[1:0] = 11b).

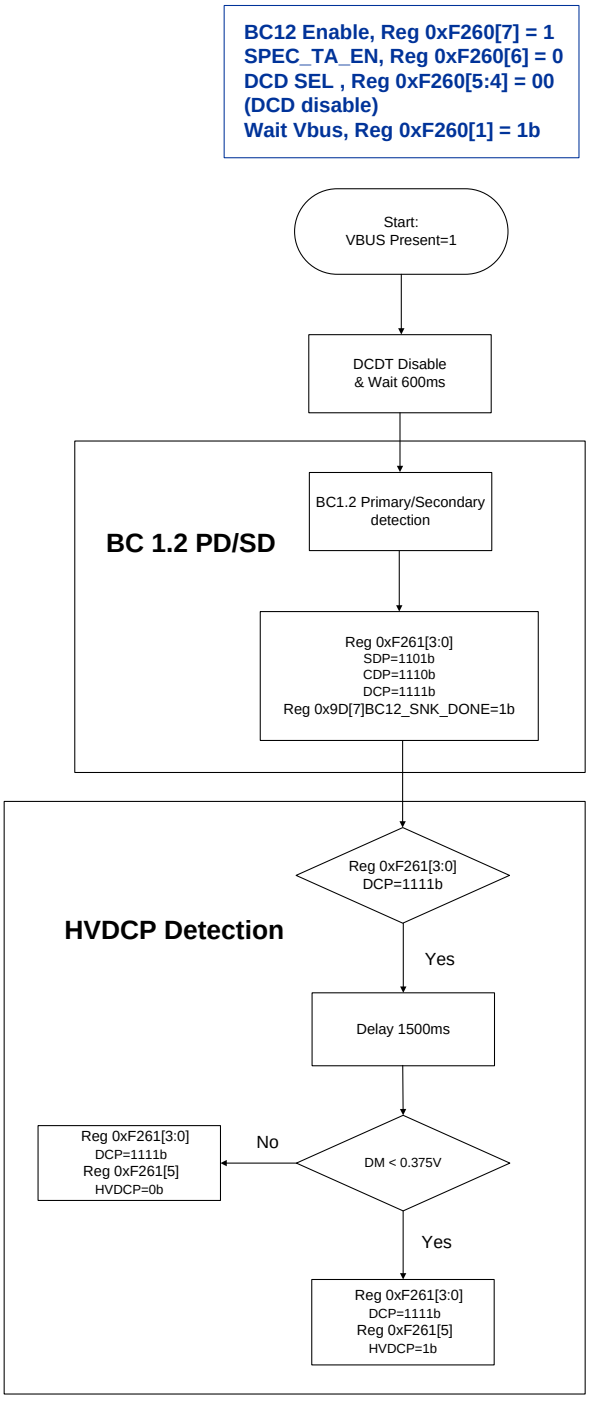
13.22.1 DPDM BC1.2 Sink Role

The RT1718S supports the BC1.2 Sink Role, Data Contact Detection (DCD) and DP 2.7V to 1.2V TA detection (TA detection for short). DCD and TA detection can work only with BC1.2 sink role enabled (0xF260[7] = 1b). The detection results are reported in BC12_STAT (0xF261[5:0]). This status register will be set to 00h after detachment. If the BC1.2 sink flow is done, it will be reported in RT_ST6 (0xA4[7]) and inform the master by IRQB (0x9D[7]). The HVDCP is also particularly reported in RT_ST6 (0xA4[6]) and inform the master by IRQB (0x9D[6]). The BC1.2 sink flow status and HVDCP status (0xA4[7:6]) will be 00b after detachment. The following four flow charts show the detection flows depending on the enabled detection functions.









Addr	Length	Bit	BitName	Default	Type	Description
0x3A in Page 2	1	6	DPDM_VIEN	0	RW	DPDM protection VI source enable 0: Disable (default) 1: Enable
		1	DM_SWEN	0	RW	DM switch enable 0: Disable (default) 1: Enable
		0	DP_SWEN	0	RW	DP switch enable 0: Disable (default) 1: Enable
0x60 in Page 2	1	7	BC12_SNK_EN	0	RW	Enable BC12 sink side function 0: Disable (default) 1: Enable
		6	SPEC_TA_EN	0	RW	Enable DPDM 2.7V ,1.2V mode TA detection 0: Disable (default) 1: Enable
		5:4	DCDT_SEL	10	RW	DCD timeout function select 00: Disable dcd timeout function 01: Enable 300ms dcd timeout function 10: Enable 600ms dcd timeout function (default) 11: Wait data contact
		1	BC12_WAIT_VBUS	0	RW	BC12 sink function wait and check VBUS 0: Not wait VBUS > 3.8V (default) 1: Wait and check VBUS When this bit is set to 1'b1, BC12 sink function will be enabled when VBUS > 3.8V. BC12 sink function will be disabled when VBUS < 3.6V.

Addr	Length	Bit	BitName	Default	Type	Description
0x61 In Page 2	1	5	HVDCP	0	R	0: TA is not HVDCP (default) 1: TA is HVDCP
		4	DCDT	0	R	0: DCD without time out (default) 1: DCD time out
		3:0	PORT_STAT	0000	R	0000: No information (default) 1000: VBUS = device 1 (2.7V & 2V mode) 1001: VBUS = device 2 (1.2V & 1.2V mode) 1010: VBUS = device 3 (2V & 2.7V mode) 1011: VBUS = device 4 (2.7V & 2.7V mode) 1100: VBUS = device 5 (2V & 2V mode)/unknown TA (500mA) 1101: VBUS = SDP (500mA) 1110: VBUS = CDP (1500mA) 1111: VBUS = DCP (2400mA)
0x96	1	7	M_BC12_SNK_DONE	0	RW	0: Interrupt masked (default) 1: Interrupt unmasked
		6	M_HVDCP_CHK_DONE	0	RW	0: Interrupt masked (default) 1: Interrupt unmasked
0x9D	1	7	INT_BC12_SNK_DONE	0	RW	0: Cleared (default) 1: BC12 sink flow done
		6	INT_HVDCP_CHK_DONE	0	RW	0: Cleared (default) 1: HVDCP flow check done (sink side)
0xA4	1	7	BC12_SNK_DONE	0	R	0: Cleared (default) 1: BC12 sink flow done
		6	HVDCP_CHK_DONE	0	R	0: Cleared (default) 1: HVDCP flow check done (sink side)

13.22.2 2.7V and 1.2V Mode Chargers Detection

The following table shows the source ability if the source advertisement is according to the voltages of DP and DM.

0xF261[3:0]	Voltage on D+ (V)	Voltage on D- (V)	Charging Current (A)	Comments
1000b	2.7	2	2	2.7V & 2V Mode
1001b	1.2	1.2	2	1.2V & 1.2V Mode
1010b	2	2.7	1	2V & 2.7V Mode
1011b	2.7	2.7	2.4	2.7V & 2.7V Mode
1100b	2	2	0.5	2V & 2V Mode

13.22.3 DPDM BC1.2 SRC Role

The RT1718S supports the BC1.2 source role (SDP, CDP, and DCP.) To enable the BC1.2 source role, set BC12_SRC_EN to 1b (0xF26D[7] = 1b). Set the source role mode in SRC_MODE_SEL (0xF26D[6:4]).

As a CDP, the DP voltage should be between DPDM_VOL_L (0xF273[4:0]) and DPDM_VOL_H (0xF272[4:0]). The time width of DP should be between the CDP_VSRC_ON_SEL (0xF270[1:0]) and PRIMARY_TIMEOUT_SEL (0xF270[3:2]) during the primary detection, or the STS_CDP_DONE (0xF26[0]) will be 0b. The time width of DM of RT1718S will be equal to that of DP if the time width of DP is less than PRIMARY_TIMEOUT_SEL (0xF270[3:2]). After the valid primary detection (DP falling), the USBDET_TIMEOUT_SEL (0xF270[5:4]) timer will start. If DP is not higher than DPDM_VOL_H2 (0xF271[4:0]) between secondary detection done and USBDET_TIMEOUT_SEL timeout, the STS_CDP_ERR (0xF26[1]) will be 1b and the STS_CDP_DONE (0xF26[0]) will be 0b. If DP is higher than DPDM_VOL_H2 (0xF271[4:0]) between secondary detection done and USBDET_TIMEOUT_SEL timeout, the STS_CDP_ERR (0xF26[1]) will be 0b and the STS_CDP_DONE (0xF26[0]) will be 1b.

Any changes in STS_CDP_ERR (0xF26[1]) or STS_CDP_DONE (0xF26[0]) will set INT_BC12_TA_CHG (0x9D[5]) to 1b.

Addr	Length	Bit	BitName	Default	Type	Description
0x6D in Page 2	1	7	BC12_SRC_EN	0	RW	BC12 TA function enable 0: Disable (default) 1: Enable
		6:4	SRC_MODE_SEL	000	RW	Mode select 000: BC12 SDP (default) 001: BC12 CDP 010: BC12 DCP 011 to 111: Reserved
		0	WAIT_VBUS_ON	1	RW	Wait VBUS > 4.0V (VBUS_PRESENT_FLAG = 1) to enable BC12 TA function 0: Not wait VBUS > 4.0V. BC12 TA function will enable when BC12_SRC_EN = 1b 1: Wait VBUS > 4.0V. BC12 TA function will enable when BC12_SRC_EN = 1b and VBUS_PRESENT_FLAG = 1 (default)
0x70 in Page 2	1	5:4	USBDET_TIMEOUT_SEL	10	RW	USB device detect timeout 00: 1.024s 01: 2.048s 10: 4.096s (default) 11: 8.192s
		3:2	PRIMARY_TIMEOUT_SEL	00	RW	Primary detection timeout 00: 1.0s (default) 01: 1.3s 10: 1.6s 11: 2.0s
		1:0	CDP_VSRC_ON_SEL	10	RW	Vsrc_on time detection 00: 16ms 01: 24ms 10: 32ms (default) 11: 40ms

Addr	Length	Bit	BitName	Default	Type	Description
0x71 in Page 2	1	4:0	DPDM_VOL_H2	10011	RW	DPDM voltage detection setting (HI/LO) Threshold: 0.1V to 2.6V (LSB = 0.1V) 00000: 0.1V … 10011: 2.0V (default) … 11001: 2.6V ---------- 11010: 0.275V (BC1.2 VDAT_REF_MIN) 11011: 0.375V (BC1.2 VDAT_REF_MAX) 11100: 0.9V (BC1.2 VLGC_MIN) 11101: 1.975V (BC1.2 VLGC_MAX) 11110: 1.5V (A_DET_LO) 11111: 2.3V (A_DET_HI) Note: In CDP mode, this register is used to check the USB attach level. In private protocol mode/auto TA mode, this register is used to check the DPDM high level after device attach.
0x72 in Page 2	1	4:0	DPDM_VOL_H	01001	RW	DPDM voltage detection setting (HI/LO) Threshold: 0.1V to 2.6V (LSB = 0.1V) 00000: 0.1V … 01001: 1.0V (default) … 11001: 2.6V ---------- 11010: 0.275V (BC1.2 VDAT_REF_MIN) 11011: 0.375V (BC1.2 VDAT_REF_MAX) 11100: 0.9V (BC1.2 VLGC_MIN) 11101: 1.975V (BC1.2 VLGC_MAX) 11110: 1.5V (A_DET_LO) 11111: 2.3V (A_DET_HI) Note: This register is used for CDP/ private protocol to check Vdp_src high level.

Addr	Length	Bit	BitName	Default	Type	Description
0x73 in Page 2	1	4:0	DPDM_VOL_L	11010	RW	DPDM voltage detection setting (HI/LO) Threshold: 0.1V to 2.6V (LSB = 0.1V) 00000: 0.1V … 11001: 2.6V ---------- 11010: 0.275V (BC1.2 VDAT_REF_MIN) (default) 11011: 0.375V (BC1.2 VDAT_REF_MAX) 11100: 0.9V (BC1.2 VLGC_MIN) 11101: 1.975V (BC1.2 VLGC_MAX) 11110: 1.5V (A_DET_LO) 11111: 2.3V (A_DET_HI) Note: This register is used for CDP/ private protocol to check Vdp_src high level.
0x6E in Page 2	1	1	STS_CDP_ERR	0	R	CDP flow error 0: No CDP flow error (default) 1: CDP flow error Note: This bit is updated after INT_BC12_TA_CHG have been set to 1b. It will remain set until next time INT_BC12_TA_CHG is set to 1b. Check this bit only after INT_BC12_TA_CHG has been set to 1b.
		0	STS_CDP_DONE	0	R	CDP flow done 0: No CDP flow (default) 1: CDP flow done Note: This bit is updated after INT_BC12_TA_CHG has been set to 1b. It will remain set until next time INT_BC12_TA_CHG is set to 1b. Check this bit only after INT_BC12_TA_CHG has been set to 1b.
0x96	1	5	M_BC12_TA_CHG	0	RW	0: Interrupt masked (default) 1: Interrupt unmasked
0x9D	1	5	INT_BC12_TA_CHG	0	RW	0: Cleared (default) 1: BC12 source flow status change (CDP)
0xA4	1	5	BC12_TA_CHG	0	R	0: Cleared (default) 1: BC12 source flow status change (CDP/ private protocol) Note: This flag only keeps 0.33μs.

13.23 Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula:

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a WQFN-32L 4x4 package, the thermal resistance, θ_{JA}, is 27.8°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below:

$P_{D(MAX)}$ = (125°C - 25°C) / (27.8°C/W) = 3.59W for a WQFN-32L 4x4 package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curve in Figure 1 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

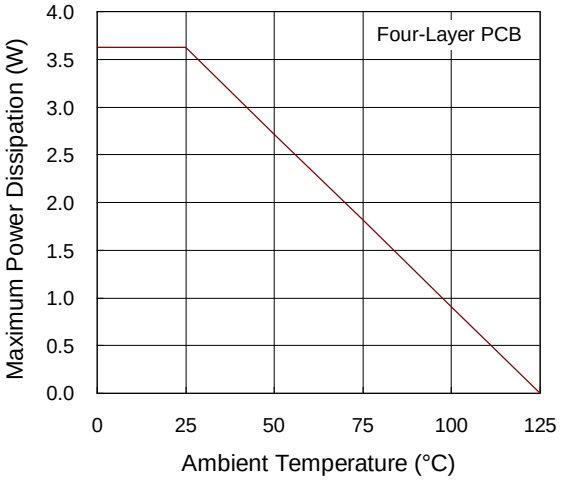


Figure 1. Derating Curve of Maximum Power Dissipation

Note 6. The information provided in this section is for reference only. The customer is solely responsible for designing, validating, and testing any applications incorporating Richtek's product(s). The customer is also responsible for applicable standards and any safety, security, or other requirements.

14 Functional Register Description

14.1 Page 1 of Register Table

Address	Length	Register Name	Bit	Bit Name	Default	Type	Description
0x00	1	VENDOR_ID	7:0	VID[7:0]	0xCF	R	A unique 16-bit unsigned integer. Assigned by the USB-IF to the vendor.
0x01	1		7:0	VID[15:8]	0x29	R	
0x02	1	PRODUCT_ID	7:0	PID[7:0]	0x18	R	A unique 16-bit unsigned integer. Assigned uniquely by the vendor to identify the TCPC.
0x03	1		7:0	PID[15:8]	0X17	R	
0x04	1	DEVICE_ID	7:0	DID[7:0]	0x14	R	A unique 16-bit unsigned integer. Assigned by the vendor to identify the version of the TCPC.
0x05	1		7:0	DID[15:8]	0x45	R	
0x06	1	USBTYPEC_REV	7:0	USBTYPEC_REV	0x12	R	Byte 0 of a 16-bit USB Type-C Revision 1.2.
0x07	1		7:0	Reserved	0	R	Reserved
0x08	1	USBPD_REV_VER	7:0	USBPD_VER	0x11	R	Byte 0 of a 16-bit USB PD Version 1.1.
0x09	1		7:0	USBPD_REV	0x30	R	Byte 1 of a 16-bit USB PD Revision 3.0.
0x0A	1	PD_INTERFACE_REV	7:0	PDIF_VER	0x12	R	Byte 0 of a 16-bit PD Interface (TCPC) Version 1.2.
0x0B	1		7:0	PDIF_REV	0x10	R	Byte 1 of a 16-bit PD Interface (TCPC) Revision 1.0.

Address	Length	Register Name	Bit	Bit Name	Default	Type	Description
0x10	1	ALERT	7	ALARM_ VBUS_ VOLTAGE_H	0	RW	0: Cleared (default) 1: A high-voltage alarm has occurred
			6	TX_ SUCCESS	0	RW	0: Cleared (default) 1: Reset or SOP* message transmission successful.
			5	TX_ DISCARD	0	RW	0: Cleared (default) 1: Reset or SOP* message transmission not sent due to incoming receive message.
			4	TX_FAIL	0	RW	0: Cleared (default) 1: SOP* message transmission not successful, no GoodCRC response received on SOP* message transmission.
			3	RX_HARD_ RESET	0	RW	0: Cleared (default) 1: Received Hard Reset message
			2	RX_SOP_ MSG_ STATUS	0	RW	0: Cleared (default) 1: Receive status register changed
			1	POWER_ STATUS	1	RW	0: Cleared 1: Port status changed (default)
			0	CC_STATUS	0	RW	0: Cleared (default) 1: CC status changed
0x11	1	ALERT	7	VENDOR_ DEFINED_ ALERT Reserved	0	RW	0: Cleared (default) 1: A vendor defined alert has been detected. Defined in the VENDOR_DEFINED registers. Refer to the vendor datasheet for details. This bit can be cleared, regardless of the current status of the alert source.
			6:4	Reserved	000	R	Reserved
			3	VBUS_SINK_ DISCNT	0	RW	0: Cleared (default) 1: A VBUS sink disconnect threshold crossing has been detected.
			2	RXBUF_ OVFLOW	0	RW	0: TCPC RX buffer is functioning properly. (default) 1: TCPC RX buffer has overflowed.
			1	FAULT	0	RW	0: No Fault (default) 1: A Fault has occurred. Read the FAULT_STATUS register.
			0	ALARM_ VBUS_ VOLTAGE_L	0	RW	0: Cleared (default) 1: A low-voltage alarm has occurred

Address	Length	Register Name	Bit	Bit Name	Default	Type	Description
0x12	1	ALERT_ MASK	7	M_ALARM_ VBUS_ VOLTAGE_H	1	RW	0: Interrupt masked 1: Interrupt unmasked (default)
			6	M_TX_ SUCCESS	1	RW	0: Interrupt masked 1: Interrupt unmasked (default)
			5	M_TX_ DISCARD	1	RW	0: Interrupt masked 1: Interrupt unmasked (default)
			4	M_TX_FAIL	1	RW	0: Interrupt masked 1: Interrupt unmasked (default)
			3	M_RX_HARD_ RESET	1	RW	0: Interrupt masked 1: Interrupt unmasked (default)
			2	M_RX_SOP_ MSG_ STATUS	1	RW	0: Interrupt masked 1: Interrupt unmasked (default)
			1	M_POWER_ STATUS	1	RW	0: Interrupt masked 1: Interrupt unmasked (default)
			0	M_CC_ STATUS	1	RW	0: Interrupt masked 1: Interrupt unmasked (default)
0x13	1	ALERT_ MASK	7	M_VENDOR_ DEFINED_ ALERT	0	R	0: Interrupt masked (default) 1: Interrupt unmasked
			6:4	Reserved	000	R	Reserved
			3	M_VBUS_ SINK_ DISCNT	1	R	0: Interrupt masked 1: Interrupt unmasked (default)
			2	M_RXBUF_ OVFLOW	1	RW	0: Interrupt masked 1: Interrupt unmasked (default)
			1	M_FAULT	1	RW	0: Interrupt masked 1: Interrupt unmasked (default)
			0	M_ALARM_ VBUS_ VOLTAGE_L	1	R	0: Interrupt masked 1: Interrupt unmasked (default)

Address	Length	Register Name	Bit	Bit Name	Default	Type	Description
0x14	1	POWER_ STATUS_ MASK	7	M_DEBUG_ ACCESSORY_ CONNECT	1	RW	0: Interrupt masked 1: Interrupt unmasked (default)
			6	M_TCPC_ INITIAL	1	RW	0: Interrupt masked 1: Interrupt unmasked (default)
			5	M_SRC_HV	1	RW	0: Interrupt masked 1: Interrupt unmasked (default)
			4	M_SRC_VBUS	1	RW	0: Interrupt masked 1: Interrupt unmasked (default)
			3	M_VBUS_ PRESENT_ DETC	1	RW	0: Interrupt masked 1: Interrupt unmasked (default)
			2	M_VBUS_ PRESENT	1	RW	0: Interrupt masked 1: Interrupt unmasked (default)
			1	M_VCONN_ PRESENT	1	RW	0: Interrupt masked 1: Interrupt unmasked (default)
			0	M_SINK_ VBUS	1	RW	0: Interrupt masked 1: Interrupt unmasked (default)
0x15	1	FAULT_ STATUS_ MASK	7	M_ALL_ REGISTERS_R ESET_TO_ DEFAULT	1	RW	0: Interrupt masked 1: Interrupt unmasked (default)
			6	M_FORCE_ OFF_VBUS	1	RW	0: Interrupt masked 1: Interrupt unmasked (default)
			5	M_AUTO_ DISC_FAIL	1	RW	0: Interrupt masked 1: Interrupt unmasked (default)
			4	M_FORCE_ DISC_FAIL	1	RW	0: Interrupt masked 1: Interrupt unmasked (default)
			3	M_VBUS_OC	1	RW	0: Interrupt masked 1: Interrupt unmasked (default)
			2	M_VBUS_OV	1	RW	0: Interrupt masked 1: Interrupt unmasked (default)
			1	M_VCONN_ OC	1	RW	0: Interrupt masked 1: Interrupt unmasked (default)
			0	M_I2C_ ERROR	1	RW	0: Interrupt masked 1: Interrupt unmasked (default)

Address	Length	Register Name	Bit	Bit Name	Default	Type	Description
0x18	1	CONFIG_ STANDARD _OUTPUT	7	H_ IMPEDENCE	0	R	0: Standard output control (default) 1: Force all outputs to high impedance This can be used to save power in sleep mode. Controlled by the TCPM.
			6	DBG_ACC_ CONNECT	1	RW	0: Debug Accessory Connected# output is driven low. Debug accessory connected. 1: Debug Accessory Connected# output is driven high. No debug accessory connected. (default) Controlled by either the TCPM or TCPC. The TCPC shall ignore writes to this bit if TCPC_CONTROL.DebugAccessoryControl = 0.
			5	AUDIO_ACC_ CONNECT	1	R	Not support.
			4	ACTIVE_ CABLE_ CONNECT	0	R	Not support.
			3:2	MUX_CTRL	00	R	Not support.
			1	CONNECT_ PRESENT	0	R	0: No Connection (default) 1: Connection
			0	CONNECT_ ORIENTATION	0	RW	0: Normal (CC1 = A5, CC2 = B5, TX1=A2/A3, RX1=B10/B11) (default) 1: Flipped (CC2 = A5, CC1 = B5, TX1 = B2/B3, RX1 = A10/A11) Controlled by the TCPM The TCPC shall ignore writes to this bit if TCPC_CONTROL.DebugAccessoryControl = 0.

Address	Length	Register Name	Bit	Bit Name	Default	Type	Description
0x19	1	TCPC_ CONTROL	7:6	Reserved	00	R	Reserved
			5	ENABLE_ WATCHDOG_ TIMER	0	RW	0: Watchdog monitoring is disabled. (default) 1: Watchdog monitoring is enabled.
			4	DEBUG_ ACCESSORY_ CONTROL	0	RW	0: Controlled by TCPC. (default) 1: Controlled by TCPM. The TCPM writes 1 to this register to take over control of asserting the DebugAccessoryConnected#.
			3:2	I2C_CK_ STRETCH	00	R	Not support.
			1	BIST_TEST_ MODE	0	RW	0: Normal operation. Incoming messages enabled by RECEIVE_DETECT are passed to TCPM via Alert. (default) 1: BIST test mode. Incoming messages enabled by RECEIVE_DETECT result in a GoodCRC response but may not be passed to the TCPM via Alert. The TCPC may temporarily store incoming messages in the receive message buffer, but this may or may not result in a receive SOP* message status or a RX buffer overflow alert.
			0	PLUG_ ORIENT	0	RW	0: When VCONN is enabled, apply it to the CC2 pin. Monitor the CC1 pin for BMC communications if PD messaging is enabled. (default) 1: When VCONN is enabled, apply it to the CC1 pin. Monitor the CC2 pin for BMC communications if PD messaging is enabled. Required

Address	Length	Register Name	Bit	Bit Name	Default	Type	Description
0x1A	1	ROLE_ CONTROL	7	Reserved	0	R	Reserved
			6	DRP	0	RW	0: No DRP. 0x1A[3:0] determines Rp/Rd/Ra settings (default) 1: DRP
			5:4	RP_VALUE	00	RW	00: Rp default (default) 01: Rp 1.5A 10: Rp 3.0A 11: Reserved
			3:2	CC2	10	RW	00: Reserved 01: Rp (Use Rp definition in 0x1A[5:4]) 10: Rd(default) 11: Open (Disconnect or Do not care) Set to 11b if enabling DRP in 0x1A[7:6]
			1:0	CC1	10	RW	00: Reserved 01: Rp (Use Rp definition in 0x1A[5:4]) 10: Rd (default) 11: Open (Disconnect or Do not care) Set to 11b if enabling DRP in 0x1A[7:6]
0x1B	1	FAULT_ CONTROL	7:5	Reserved	000	R	Reserved
			4	DIS_FORCE_ OFF_VBUS	0	R	Not support.
			3	DIS_VBUS_ DISC_FAULT_ TIMER	0	RW	0: VBUS discharge fault detection timer enabled (default) 1: VBUS discharge fault detection timer disabled
			2	DIS_VBUS_OC	0	RW	0: Internal and external OCP circuit enabled (default) 1: Internal and external OCP circuit disabled
			1	DIS_VBUS_OV	0	RW	0: Internal and external OVP circuit enabled (default) 1: Internal and external OVP circuit disabled
			0	DIS_VCONN_ OC	0	RW	0: Fault detection circuit enabled (default) 1: Fault detection circuit disabled

Address	Length	Register Name	Bit	Bit Name	Default	Type	Description
0x1C	1	POWER_ CONTROL	7	Reserved	0	R	Reserved
			6	VBUS_VOL_ MONITOR	1	RW	0: VBUS_VOLTAGE monitoring is enabled. 1: VBUS_VOLTAGE monitoring is disabled. (default)
			5	DIS_VOL_ ALARM	1	RW	0: Voltage alarms power status reporting is enabled. 1: Voltage alarms power status reporting is disabled. (default)
			4	AUTO_DISC_ DISCNCT	0	RW	0: The TCPC shall not automatically discharge VBUS based on VBUS voltage. (default) 1: The TCPC shall automatically discharge.
			3	EN_BLEED_ DISC	0	RW	0: Disable bleed discharge. (default) 1: Enable bleed discharge of VBUS
			2	FORCE_DISC	0	RW	0: Disable force discharge. (default) 1: Enable force discharge of VBUS.
			1	VCONN_ POWER_SPT	0	RW	0: TCPC delivers at least 1W on VCONN (default) 1: TCPC delivers at least the power indicated in DEVICE_CAPABILITIES.VCONNPowerSupported
			0	EN_VCONN	0	RW	0: Disable VCONN source (default) 1: Enable VCONN source to CC

Address	Length	Register Name	Bit	Bit Name	Default	Type	Description
0x1D	1	CC_ STATUS	7:6	Reserved	00	R	Reserved
			5	LOOKING4 CONNECTION	0	R	0: TCPC is not actively looking for a connection. A transition from “1” to “0” indicates a potential connection has been found. (default) 1: TCPC is looking for a connection (toggling as a DRP or looking for a connection as sink/source only condition).
			4	Connect_ RESULT	0	R	0: The TCPC is presenting Rp. (default) 1: The TCPC is presenting Rd.

			3:2	CC2_STATUS	00	R	If (ROLE_CONTROL.CC2 = Rp) or (Connect_Result = 0)
							00: SRC.Open (open, Rp) (default)
							01: SRC.Ra (below maximum vRa)
							10: SRC.Rd (within the vRd range)
							11: Reserved
							If (ROLE_CONTROL.CC2 = Rd) or (Connect_Result = 1)
							00: SNK.Open (below maximum vRa) (default)
							01: SNK.Default (above minimum vRd-Connect)
							10: SNK.Power1.5 (above minimum vRd-Connect) Detects Rp 1.5A
							11: SNK.Power3.0 (above minimum vRd-Connect) detects Rp 3.0A
							If ROLE_CONTROL.CC2 = Ra, this field is set to 00b.
							If ROLE_CONTROL.CC2 = Open, this field is set to 00b.
							This field always returns 00b if (Looking4Connection = 1) or (POWER_CONTROL.EnableVCONN =
							1 and POWER_CONTROL.PlugOrientation =
							0). Otherwise, the returned value depends upon ROLE_CONTROL.CC2.

Address	Length	Register Name	Bit	Bit Name	Default	Type	Description

			1:0	CC1_STATUS	00	R	If (ROLE_CONTROL.CC1 = Rp) or (Connect_Result = 0)
							00: SRC.Open (open, Rp) (default)
							01: SRC.Ra (below maximum vRa)
							10: SRC.Rd (within the vRd range)
							11: Reserved
							
							If (ROLE_CONTROL.CC1 = Rd) or (Connect_Result = 1)
							00: SNK.Open (below maximum vRa) (default)
							01: SNK.Default (above minimum vRd-Connect)
							10: SNK.Power1.5 (above minimum vRd-Connect) Detects Rp-1.5A
							11: SNK.Power3.0 (above minimum vRd-Connect) Detects Rp-3.0A
							
							If ROLE_CONTROL.CC1 = Ra, this field is set to 00b
							If ROLE_CONTROL.CC1 = Open, this field is set to 00b
							
							This field always returns 00b if (Looking4Connection = 1) or (POWER_CONTROL.EnableVCONN =
							1 and POWER_CONTROL.PlugOrientation = 0). Otherwise, the returned value depends upon ROLE_CONTROL.CC1.

Address	Length	Register Name	Bit	Bit Name	Default	Type	Description
0x1E	1	POWER_ STATUS	7	DBG_ACC_ CONNECT	0	R	0: No debug accessory connected (default) 1: Debug accessory connected Reflects the state of the DebugAccessoryConnected# output if supported.
			6	TCPC_INITIAL	0	R	0: The TCPC has completed initialization and all registers are valid. (default) 1: The TCPC is still performing internal initialization and the only registers that are guaranteed to return the correct values are 00h..0Fh.
			5	SRC_HV	0	R	0: vSafe5V (default) 1: High voltage This does not control the path, it just provides a monitor of the status. Assert as long as supplying voltage greater than vSafe5V.
			4	SRC_VBUS	0	R	0: Sourcing VBUS is disabled. (default) 1: Sourcing VBUS is enabled. This does not control the path, it just provides a monitor of the status.
			3	VBUS_ PRESENT_ DETC	1	R	0: VBUS present detection disabled 1: VBUS present detection enabled (default)
			2	VBUS_ PRESENT	0	R	0: VBUS disconnected (default) 1: VBUS connected
			1	VCONN_ PRESENT	0	R	0: VCONN is not present (default) 1: This bit is asserted when VCONN Is present on CC1 or CC2. The threshold is fixed at 2.4V
			0	SINK_VBUS	0	R	0: Sink is disconnected (default) 1: TCPC is sinking VBUS to the system load.

Address	Length	Register Name	Bit	Bit Name	Default	Type	Description
0x1F	1	FAULT_STATUS	7	ALL_REGISTERS_RESET_TO_DEFAULT	1	RW	0: Bit cleared. 1: When the TCPC resets all registers to their default value. This happens at initial power up or if an unexpected power reset occurs. (default)
			6	FORCE_OFF_VBUS	0	RW	Not support.
			5	AUTO_DISC_FAIL	0	RW	0: No discharge failure (default) 1: Discharge commanded by the TCPM failed
			4	FORCE_DISC_FAIL	0	RW	0: No discharge failure (default) 1: Discharge commanded by the TCPM failed.
			3	VBUS_OC	0	RW	0: Not in an overcurrent protection state (default) 1: Overcurrent fault latched
			2	VBUS_OV	0	RW	0: Not in an overvoltage protection state (default) 1: Overvoltage fault latched.
			1	VCONN_OC	0	RW	0: No fault detected (default) 1: Overcurrent VCONN fault latched
			0	I2C_ERROR	0	RW	0: No Error (default) 1: I^2C error has occurred.

Address	Length	Register Name	Bit	Bit Name	Default	Type	Description
0x23	1	COMMAND	7:0	COMMAND	00000000	W	0000 0000: No action (default) 0001 0001: Not support 0010 0010: DisableVbusDetect: Disable Vbus present and vSafe0V detection. 0011 0011: EnableVbusDetect: Enable Vbus present and vSafe0V detection. 0100 0100: DisableSinkVbus: Disable sinking power over Vbus. This COMMAND does not disable POWER_STATUS.VBUSPresent detection. 0101 0101: SinkVbus. Enable sinking power over Vbus and enable Vbus present detection. The TCPC shall ignore this command and assert the FAULT_STATUS.I2CInterfaceError if it has sourcing power over Vbus enabled. 0110 0110: DisableSourceVbus. Disable sourcing power over Vbus. The TCPC shall stop reporting FAULT_STATUS. Internal or External OCP or OVP Faults. This COMMAND does not disable POWER_STATUS.VBUSPresent detection. 0111 0111: SourceVbusDefaultVoltage. Enable sourcing vSafe5V over Vbus and enable Vbus present detection. The source shall transition to vSafe5V if at a high voltage. The TCPC shall ignore this command and assert the FAULT_STATUS.I2CInterfaceError if it has sinking power over Vbus enabled. 1000 1000: SourceVbusHighVoltage. Execute sourcing high voltage over Vbus. The TCPC shall ignore this command and assert the FAULT_STATUS.I2CInterfaceError if it is currently sinking voltage from Vbus or does not have the ability to source voltages higher than vSafe5V. The TCPC shall ignore this command and assert the FAULT_STATUS.I2CInterfaceError if not already sourcing vSafe5V. 1001 1001b: Start DRP Toggling if ROLE_CONTROL.DRP = 1b. If ROLE_CONTROL.CC1/CC2= 01b, startwith Rp, if ROLE_CONTROL.CC1/CC2

Address	Length	Register Name	Bit	Bit Name	Default	Type	Description
							= 10b, start with Rd. Other settings: Reserved
0x24	1	DEVICE_ CAPABILITIES_1L	7:5	ROLES_ SUPPORT	110	R	000: Type-C Port Manager can configure the port as source only or sink only (not DRP) 001: Source only 010: Sink only 011: Sink with accessory support (optional) 100: DRP only 101: Adapter or Cable (Ra) only 110: Source, Sink, DRP, Adapter/Cable all supported (default) 111: Not valid
			4	ALL_SOP_ SUPPORT	1	R	0: All SOP* except SOP'_DBG/SOP"_DBG 1: All SOP* messages are supported (default)
			3	SOURCE_ VCONN	1	R	0: TCPC is not capable of switching VCONN 1: TCPC is capable of switching VCONN (default)
			2	CPB_SINK_ VBUS	1	R	0: TCPC is not capable controlling the sink path to the system load. 1: TCPC is capable of controlling the sink path to the system load. (default)
			1	SOURCE_ HV_VBUS	1	R	0: TCPC is not capable of controlling the source high voltage path to VBUS. 1: TCPC is capable of controlling the source high voltage path to VBUS. (default)
			0	SOURCE_ VBUS	1	R	0: TCPC is not capable of controlling the source path to VBUS. 1: TCPC is capable of controlling the source path to VBUS. (default)

Address	Length	Register Name	Bit	Bit Name	Default	Type	Description
0x25	1	DEVICE_ CAPABILITIES_1H	7	Reserved	0	R	Reserved
			6	CPB_VBUS_ OC	1	R	0: VBUS OCP is not reported by the TCPC 1: VBUS OCP is reported by the TCPC (default)
			5	CPB_VBUS_ OV	1	R	0: VBUS OVP is not reported by the TCPC 1: VBUS OVP is reported by the TCPC (default)
			4	CPB_BLEED_ DISC	1	R	0: No bleed discharge implemented in TCPC 1: Bleed discharge is implemented in the TCPC (default)
			3	CPB_FORCE_ DISC	1	R	0b: No force discharge implemented in TCPC 1b: Force discharge is implemented in the TCPC (default)
			2	VBUS_ MEASURE_ ALARM	1	R	0: No VBUS voltage measurement nor VBUS alarms 1: VBUS voltage measurement and VBUS alarms (default)
			1:0	SOURCE_ RP_SUPPORT	10	R	00: Rp default only 01: Rp 1.5A and default 10: Rp 3.0A, 1.5A, and default (default) 11: Reserved Rp values configurable by the TCPM via the ROLE_CONTROL register

Address	Length	Register Name	Bit	Bit Name	Default	Type	Description
0x26	1	DEVICE_CAPABILITIES_2L	7	SINK_DISCONNECT_DET	1	R	0: VBUS_SINK_DISCONNECT_THRESHOLD is not implemented (default: use POWER_STATUS.VbusPresent = 0b to indicate a sink disconnect) 1: VBUS_SINK_DISCONNECT_THRESHOLD is implemented (default)
			6	STOP_DISC_THD	1	R	0: VBUS_STOP_DISCHARGE_THRESHOLD is not implemented 1: VBUS_STOP_DISCHARGE_THRESHOLD is implemented (default)
			5:4	VBUS_VOL_ALARM_LSB	00	R	00: TCPC has 25mV LSB for its voltage alarm and uses all 10 bits in VBUS_VOLTAGE_ALARM_HI_CFG and VBUS_VOLTAGE_ALARM_LO_CFG. (default) 01: TCPC has 50mV LSB for its voltage alarm and uses only 9 bits. VBUS_VOLTAGE_ALARM_HI_CFG[0] and VBUS_VOLTAGE_ALARM_LO_CFG[0] are ignored by TCPC. 10: TCPC has 100mV LSB for its voltage alarm and uses only 8 bits. VBUS_VOLTAGE_ALARM_HI_CFG[1:0] and VBUS_VOLTAGE_ALARM_LO_CFG[1:0] are ignored by TCPC. 11: Not support this function.
			3:1	VCONN_POWER	000	R	000: 1.0W (default) 001: 1.5W 010: 2.0W 011: 3W 100: 4W 101: 5W 110: 6W 111: External
			0	VCONN_OCF	1	R	0: TCPC is not capable of detecting a VCONN fault 1: TCPC is capable of detecting a VCONN fault (default)
0x27	1	DEVICE_CAPABILITIES_2H	7:1	Reserved	0000000	R	Reserved
			0	CPB_WATCHDOG	1	R	0: TCPC_CONTROL.Enable Watchdog timer is not implemented 1: TCPC_CONTROL.Enable Watchdog timer is implemented (default)

Address	Length	Register Name	Bit	Bit Name	Default	Type	Description
0x28	1	STANDARD_INPUT_CAPABILITIES	7:3	Reserved	00000	R	Reserved
			2	VBUS_EXT_OVF	0	R	0: Not present in TCPC (default) 1: Present in TCPC
			1	VBUS_EXT_OCF	0	R	0: Not present in TCPC (default) 1: Present in TCPC
			0	FORCE_OFF_VBUS_IN	0	R	0: Not present in TCPC (default) 1: Present in TCPC
0x29	1	STANDARD_OUTPUT_CAPABILITIES	7	Reserved	0	R	Reserved
			6	CPB_DBG_ACC_IND	0	R	0: Not present in TCPC (default) 1: Present in TCPC
			5	CPB_VBUS_PRESENT_MNT	0	R	0: Not present in TCPC (default) 1: Present in TCPC
			4	CPB_AUDIO_ADT_ACC_IND	0	R	0: Not present in TCPC (default) 1: Present in TCPC
			3	CPB_ACTIVE_CABLE_IND	0	R	0: Not present in TCPC (default) 1: Present in TCPC
			2	CPB_MUX_CFG_CTRL	0	R	0: Not present in TCPC (default) 1: Present in TCPC
			1	CPB_CONNECT_PRESENT	0	R	0: Not present in TCPC (default) 1: Present in TCPC
			0	CPB_CONNECT_ORIENT	0	R	0: Not present in TCPC (default) 1: Present in TCPC
0x2E	1	MESSAGE_HEADER_INFO	7:5	Reserved	000	R	Reserved
			4	CABLE_PLUG	0	RW	0: Message originated from source, sink, or DRP (default) 1: Message originated from a cable plug
			3	DATA_ROLE	0	RW	0: Sink (default) 1: Source
			2:1	USBPD_SPECREV	01	RW	00: Revision 1.0 01: Revision 2.0 (default) 10: Revision 3.0 11: Reserved
			0	POWER_ROLE	0	RW	0: Sink (default) 1: Source

Address	Length	Register Name	Bit	Bit Name	Default	Type	Description
0x2F	1	RECEIVE_DETECT	7	Reserved	0	R	Reserved
			6	EN_CABLE_RST	0	RW	0: TCPC does not detect Cable Reset signaling (default) 1: TCPC detects Cable Reset signaling
			5	EN_HARD_RST	0	RW	0: TCPC does not detect Hard Reset signaling (default) 1: TCPC detects Hard Reset signaling
			4	EN_SOP2DB	0	RW	0: TCPC does not detect SOP_DBG' message (default) 1: TCPC detects SOP_DBG'' message
			3	EN_SOP1DB	0	RW	0: TCPC does not detect SOP_DBG' message (default) 1: TCPC detects SOP_DBG' message
			2	EN_SOP2	0	RW	0: TCPC does not detect SOP'' message (default) 1: TCPC detects SOP'' message
			1	EN_SOP1	0	RW	0b: TCPC does not detect SOP' message (default) 1b: TCPC detects SOP' message
			0	EN_SOP	0	RW	0: TCPC does not detect SOP message (default) 1: TCPC detects SOP message
0x30	1	RX_BYTE_COUNT	7:0	RX_BYTE_COUNT	0x00	RW	Indicates number of bytes in this register that are not stale. The TCPM should read the first RECEIVE_BYTE_COUNT bytes in this register.
0x31	1	RX_BUF_FRAME_TYPE	7:3	Reserved	00000	R	Reserved
			2:0	RX_FRAME_TYPE	000	R	Type of received frame 000: Received SOP (default) 001: Received SOP' 010: Received SOP'' 011: Received SOP_DBG' 100: Received SOP_DBG'' 110: Received Cable Reset. All others are reserved.
0x32	1	RX_BUF_HEADER_BYTE_0	7:0	RX_HEAD_0	0x00	R	Byte 0 (0x32[7:0]) of message header
0x33	1	RX_BUF_HEADER_BYTE_1	7:0	RX_HEAD_1	0x00	R	Byte 1 (0x33[15:8]) of message header
0x34	1	RX_BUF_OBJ1_BYTE_0	7:0	RX_OBJ1_0	0x00	R	Byte 0 (0x34[7:0]) of 1st data object
0x35	1	RX_BUF_OBJ1_BYTE_1	7:0	RX_OBJ1_1	0x00	R	Byte 1 (0x35[15:8]) of 1st data object

Address	Length	Register Name	Bit	Bit Name	Default	Type	Description
0x36	1	RX_BUF_OBJ1_BYTE_2	7:0	RX_OBJ1_2	0x00	R	Byte 2 (0x36[23:16]) of 1st data object
0x37	1	RX_BUF_OBJ1_BYTE_3	7:0	RX_OBJ1_3	0x00	R	Byte 3 (0x37[31:24]) of 1st data object
0x38	1	RX_BUF_OBJ2_BYTE_0	7:0	RX_OBJ2_0	0x00	R	Byte 0 (0x38[7:0]) of 2st data object
0x39	1	RX_BUF_OBJ2_BYTE_1	7:0	RX_OBJ2_1	0x00	R	Byte 1 (0x39[15:8]) of 2st data object
0x3A	1	RX_BUF_OBJ2_BYTE_2	7:0	RX_OBJ2_2	0x00	R	Byte 2 (0x3A[23:16]) of 2st data object
0x3B	1	RX_BUF_OBJ2_BYTE_3	7:0	RX_OBJ2_3	0x00	R	Byte 3 (0x3B[31:24]) of 2st data object
0x3C	1	RX_BUF_OBJ3_BYTE_0	7:0	RX_OBJ3_0	0x00	R	Byte 0 (0x3C[7:0]) of 3st data object
0x3D	1	RX_BUF_OBJ3_BYTE_1	7:0	RX_OBJ3_1	0x00	R	Byte 1 (0x3D[15:8]) of 3st data object
0x3E	1	RX_BUF_OBJ3_BYTE_2	7:0	RX_OBJ3_2	0x00	R	Byte 2 (0x3E[23:16]) of 3st data object
0x3F	1	RX_BUF_OBJ3_BYTE_3	7:0	RX_OBJ3_3	0x00	R	Byte 3 (0x3F[31:24]) of 3st data object
0x40	1	RX_BUF_OBJ4_BYTE_0	7:0	RX_OBJ4_0	0x00	R	Byte 0 (0x40[7:0]) of 4st data object
0x41	1	RX_BUF_OBJ4_BYTE_1	7:0	RX_OBJ4_1	0x00	R	Byte 1 (0x41[15:8]) of 4st data object
0x42	1	RX_BUF_OBJ4_BYTE_2	7:0	RX_OBJ4_2	0x00	R	Byte 2 (0x42[23:16]) of 4st data object
0x43	1	RX_BUF_OBJ4_BYTE_3	7:0	RX_OBJ4_3	0x00	R	Byte 3 (0x43[31:24]) of 4st data object
0x44	1	RX_BUF_OBJ5_BYTE_0	7:0	RX_OBJ5_0	0x00	R	Byte 0 (0x44[7:0]) of 5st data object
0x45	1	RX_BUF_OBJ5_BYTE_1	7:0	RX_OBJ5_1	0x00	R	Byte 1 (0x45[15:8]) of 5st data object

Address	Length	Register Name	Bit	Bit Name	Default	Type	Description
0x46	1	RX_BUF_OBJ5_BYTE_2	7:0	RX_OBJ5_2	0x00	R	Byte 2 (0x46[23:16]) of 5st data object
0x47	1	RX_BUF_OBJ5_BYTE_3	7:0	RX_OBJ5_3	0x00	R	Byte 3 (0x47[31:24]) of 5st data object
0x48	1	RX_BUF_OBJ6_BYTE_0	7:0	RX_OBJ6_0	0x00	R	Byte 0 (0x48[7:0]) of 6st data object
0x49	1	RX_BUF_OBJ6_BYTE_1	7:0	RX_OBJ6_1	0x00	R	Byte 1 (0x49[15:8]) of 6st data object
0x4A	1	RX_BUF_OBJ6_BYTE_2	7:0	RX_OBJ6_2	0x00	R	Byte 2 (0x4A[23:16]) of 6st data object
0x4B	1	RX_BUF_OBJ6_BYTE_3	7:0	RX_OBJ6_3	0x00	R	Byte 3 (0x4B[31:24]) of 6st data object
0x4C	1	RX_BUF_OBJ7_BYTE_0	7:0	RX_OBJ7_0	0x00	R	Byte 0 (0x4C[7:0]) of 7st data object
0x4D	1	RX_BUF_OBJ7_BYTE_1	7:0	RX_OBJ7_1	0x00	R	Byte 1 (0x4D[15:8]) of 7st data object
0x4E	1	RX_BUF_OBJ7_BYTE_2	7:0	RX_OBJ7_2	0x00	R	Byte 2 (0x4E[23:16]) of 7st data object
0x4F	1	RX_BUF_OBJ7_BYTE_3	7:0	RX_OBJ7_3	0x00	R	Byte 3 (0x4F[31:24]) of 7st data object

Address	Length	Register Name	Bit	Bit Name	Default	Type	Description
0x50	1	X_BUF_FRAME_TYPE	7:6	Reserved	00	R	Reserved
			5:4	TX_RETRY_CNT	00	RW	00: No message retry is required (default) 01: Automatically retry message transmission once 10: Automatically retry message transmission twice 11: Automatically retry message transmission three times
			3	Reserved	0	R	Reserved
			2:0	TX_FRAME_TYPE	000	RW	000: Transmit SOP (default) 001: Transmit SOP' 010: Transmit SOP'' 011: Transmit SOP_DBG' 100: Transmit SOP_DBG'' 101: Transmit Hard Reset 110: Transmit Cable Reset 111: Transmit BIST Carrier Mode 2 (TCPC shall exit the BIST mode no later than tBISTContMode max)
0x51	1	TX_BYTE_COUNT	7:0	TX_BYTE_COUNT	0x00	RW	The number of bytes the TCPM will write
0x52	1	TX_BUF_HEADER_BYTE_0	7:0	TX_HEAD_0	0x00	RW	Byte 0 (0x52[7:0]) of message header
0x53	1	TX_BUF_HEADER_BYTE_1	7:0	TX_HEAD_1	0x00	RW	Byte 1 (0x53[15:8]) of message header
0x54	1	TX_BUF_OBJ1_BYTE_0	7:0	TX_OBJ1_0	0x00	RW	Byte 0 (0x54[7:0]) of 1st data object
0x55	1	TX_BUF_OBJ1_BYTE_1	7:0	TX_OBJ1_1	0x00	RW	Byte 1 (0x55[15:8]) of 1st data object
0x56	1	TX_BUF_OBJ1_BYTE_2	7:0	TX_OBJ1_2	0x00	RW	Byte 2 (0x56[23:16]) of 1st data object
0x57	1	TX_BUF_OBJ1_BYTE_3	7:0	TX_OBJ1_3	0x00	RW	Byte 3 (0x57[31:24]) of 1st data object
0x58	1	TX_BUF_OBJ2_BYTE_0	7:0	TX_OBJ2_0	0x00	RW	Byte 0 (0x58[7:0]) of 2st data object
0x59	1	TX_BUF_OBJ2_BYTE_1	7:0	TX_OBJ2_1	0x00	RW	Byte 1 (0x59[15:8]) of 2st data object
0x5A	1	TX_BUF_OBJ2_BYTE_2	7:0	TX_OBJ2_2	0x00	RW	Byte 2 (0x5A[23:16]) of 2st data object

Address	Length	Register Name	Bit	Bit Name	Default	Type	Description
0x5B	1	TX_BUF_OBJ2_BYTE_3	7:0	TX_OBJ2_3	0x00	RW	Byte 3 (0x5B[31:24]) of 2st data object
0x5C	1	TX_BUF_OBJ3_BYTE_0	7:0	TX_OBJ3_0	0x00	RW	Byte 0 (0x5C[7:0]) of 3st data object
0x5D	1	TX_BUF_OBJ3_BYTE_1	7:0	TX_OBJ3_1	0x00	RW	Byte 1 (0x5D[15:8]) of 3st data object
0x5E	1	TX_BUF_OBJ3_BYTE_2	7:0	TX_OBJ3_2	0x00	RW	Byte 2 (0x5E[23:16]) of 3st data object
0x5F	1	TX_BUF_OBJ3_BYTE_3	7:0	TX_OBJ3_3	0x00	RW	Byte 3 (0x5F[31:24]) of 3st data object
0x60	1	TX_BUF_OBJ4_BYTE_0	7:0	TX_OBJ4_0	0x00	RW	Byte 0 (0x60[7:0]) of 4st data object
0x61	1	TX_BUF_OBJ4_BYTE_1	7:0	TX_OBJ4_1	0x00	RW	Byte 1 (0x61[15:8]) of 4st data object
0x62	1	TX_BUF_OBJ4_BYTE_2	7:0	TX_OBJ4_2	0x00	RW	Byte 2 (0x62[23:16]) of 4st data object
0x63	1	TX_BUF_OBJ4_BYTE_3	7:0	TX_OBJ4_3	0x00	RW	Byte 3 (0x63[31:24]) of 4st data object
0x64	1	TX_BUF_OBJ5_BYTE_0	7:0	TX_OBJ5_0	0x00	RW	Byte 0 (0x64[7:0]) of 5st data object
0x65	1	TX_BUF_OBJ5_BYTE_1	7:0	TX_OBJ5_1	0x00	RW	Byte 1 (0x65[15:8]) of 5st data object
0x66	1	TX_BUF_OBJ5_BYTE_2	7:0	TX_OBJ5_2	0x00	RW	Byte 2 (0x66[23:16]) of 5st data object
0x67	1	TX_BUF_OBJ5_BYTE_3	7:0	TX_OBJ5_3	0x00	RW	Byte 3 (0x67[31:24]) of 5st data object
0x68	1	TX_BUF_OBJ6_BYTE_0	7:0	TX_OBJ6_0	0x00	RW	Byte 0 (0x68[7:0]) of 6st data object
0x69	1	TX_BUF_OBJ6_BYTE_1	7:0	TX_OBJ6_1	0x00	RW	Byte 1 (0x69[15:8]) of 6st data object
0x6A	1	TX_BUF_OBJ6_BYTE_2	7:0	TX_OBJ6_2	0x00	RW	Byte 2 (0x6A[23:16]) of 6st data object

Address	Length	Register Name	Bit	Bit Name	Default	Type	Description
0x6B	1	TX_BUF_OBJ6_BYTE_3	7:0	TX_OBJ6_3	0x00	RW	Byte 3 (0x6B[31:24]) of 6st data object
0x6C	1	TX_BUF_OBJ7_BYTE_0	7:0	TX_OBJ7_0	0x00	RW	Byte 0 (0x6C[7:0]) of 7st data object
0x6D	1	TX_BUF_OBJ7_BYTE_1	7:0	TX_OBJ7_1	0x00	RW	Byte 1 (0x6D[15:8]) of 7st data object
0x6E	1	TX_BUF_OBJ7_BYTE_2	7:0	TX_OBJ7_2	0x00	RW	Byte 2 (0x6E[23:16]) of 7st data object
0x6F	1	TX_BUF_OBJ7_BYTE_3	7:0	TX_OBJ7_3	0x00	RW	Byte 3 (0x6F[31:24]) of 7st data object
0x70	1	VBUS_VOLTAGE_L	7:0	VBUS_VOLTAGE [7:0]	0x00	R	VBUS voltage [7:0] The LSB is 25mV.
0x71	1	VBUS_VOLTAGE_H	7:4	Reserved	0000	R	Reserved
			3:2	Scale_Factor	00	RW	00: VBUS measurement not scaled. (default) 01: VBUS measurement divided by 2 10: VBUS measurement divided by 4 11: Reserved
			1:0	VBUS_VOLTAGE[9:8]	00	R	VBUS voltage [9:8]
0x72	1	VBUS_SINK_DISCONNECT_THRESHOLD_L	7:0	VBUS_SINK_DISCNT_THD[7:0]	0x8C	RW	VBUS_SINK_DISCNT_THD[7:0] The LSB is 25mV.
0x73	1	VBUS_SINK_DISCONNECT_THRESHOLD_H	7:2	Reserved	000000	R	Reserved
			1:0	VBUS_SINK_DISCNT_THD[9:8]	00	RW	VBUS_SINK_DISCNT_THD[9:8]
0x74	1	VBUS_STOP_DISCHARGE_THRESHOLD_L	7:0	VBUS_STOP_DISCHARGE_THRESHOLD [7:0]	0x20	RW	VBUS_STOP_DISCHARGE_THRESHOLD[7:0] The LSB is 25mV.
0x75	1	VBUS_STOP_DISCHARGE_THRESHOLD_H	7:2	Reserved	000000	R	Reserved
			1:0	VBUS_STOP_DISCHARGE_THRESHOLD [9:8]	00	RW	VBUS_STOP_DISCHARGE_THRESHOLD[9:8]
0x76	1	VBUS_VOLTAGE_ALARM_HI_L	7:0	VBUS_VOLTAGE_ALARM_HI [7:0]	0x00	RW	VBUS_VOLTAGE_ALARM_HI[7:0] The LSB is 25mV.

Address	Length	Register Name	Bit	Bit Name	Default	Type	Description
0x77	1	VBUS_VOLTAGE_ALARM_HI_H	7:2	Reserved	000000	R	Reserved
			1:0	VBUS_VOLTAGE_ALARM_HI[9:8]	00	RW	VBUS_VOLTAGE_ALARM_HI[9:8]
0x78	1	VBUS_VOLTAGE_ALARM_LO_L	7:0	VBUS_VOLTAGE_ALARM_LO[7:0]	0x00	RW	VBUS_VOLTAGE_ALARM_LO[7:0] The LSB is 25mV.
0x79	1	VBUS_VOLTAGE_ALARM_LO_H	7:2	Reserved	000000	R	Reserved
			1:0	VBUS_VOLTAGE_ALARM_LO[9:8]	00	RW	VBUS_VOLTAGE_ALARM_LO[9:8]
0x8A	1	VCONN_CONTROL_1	7	VCONN_DETECT_EN	0	RW	CC pin (Vconn) detection enable for Vconn_Present, Vconn_safe0V, and Vconn_Invalid. 0: Disable (default) 1: Enable
			6	VCONN_SWOFF	0	RW	PD_RP switch control when Vconn is enabled 0: PD_RP switch on when Vconn is enabled (default) 1: PD_RP switch off when Vconn is enabled
			5	VCONN_UVP_SEL	0	RW	VCONN UVP level selection 0: 2.7V (default) 1: 2.4V
			4:0	Reserved	00000	RW	Reserved

Address	Length	Register Name	Bit	Bit Name	Default	Type	Description
0x8B	1	VCONN_CONTROL_2	7	VCONN_OVP_EN_CC1	0	RW	Enable CC1 OVP. The OVP threshold is 5.75V at CC1. 0: Disable (default) 1: Enable
			6	VCONN_OVP_EN_CC2	0	RW	Enable CC2 OVP. The OVP threshold is 5.75V at CC2. 0: Disable (default) 1: Enable
			5:4	VCONN_SHT_GND_TIMER	10	RW	When VCONN_EN = 1 (0x1E[0] = 1b), VCONN_SHT_GND will be 1 (0xA0[5] = 1b) if VCONN_PRESENT is always 0 and lasts for VCONN_SHT_GND_TIMER. 00: 0.5ms 01: 0.75ms 10: 1ms (default) 11: 3ms
			3	VCONN_RVP_EN	0	RW	VCONN RVP Enable. VCONN switch will be off if the voltage at CC (selected for VCONN) is higher than VCONN by VCONN_RVP_SEL (0x8B[2]). 0: Disable (default) 1: Enable
			2	VCONN_RVP_SEL	0	RW	VCONN RVP threshold selection 0: 0.3V (default) 1: 0.5V
			1	VCONN_RVP_CP_EN	1	RW	VCONN RVP de-bounce time 0: de-bounce 3.125μs (typical) 1: No de-bounce (default)
			0	VCONN_SOFTEND_TIMER	0	RW	The time for which VCONN current limit is enabled after VCONN EN (0x1C[0] = 1b). 0: 3ms (default) 1: 5ms
0x8C	1	VCONN_CONTROL_3	7:5	VCONN_OCP_SEL	010	RW	PD_VCONN OCP level selection 000: 100mA 001: 200mA 010: 300mA (default) 011: 400mA 100: 500mA 101: 600mA 110: 700mA 111: 800mA
			4	Reserved	0	R	Reserved
			3:2	Reserved	00	RW	Reserved
			1	VCONN_OVP_DEG	0	RW	VCONN OVP de-bounce time 0: No de-bounce (default) 1: De-bounce 3.125μs (typical)
			0	Reserved	0	RW	Reserved

Address	Length	Register Name	Bit	Bit Name	Default	Type	Description
0x8F	1	SYS_CTRL_1	7	IRQB_SELECT	0	RW	Select IRQB from synchronous to 3M path or original path. 0: Original asynchronous path. (default) 1: Synchronous to 3M path.
			6	TCPC_CONN_INVALID	1	RW	Enable TCPC connect invalid state machine to trigger I^2C interface error interrupt. 0: Disable 1: Enable (default)
			5	SHIPPING_OFF	0	RW	Only I^2C function works in shipping mode. 0: Shipping mode (default) 1: Non shipping mode
			4	Reserved	1	R	Reserved
			3	AUTOIDLE_EN	0	RW	Auto entering idle mode 0: No entering idle mode (default) 1: Auto entering idle mode
			2:0	AUTOIDLE_TIMEOUT	010	RW	Auto idle mode timer 000: 6.4ms 001: 19.2ms 010: 32ms (default) 011: 44.8ms 100: 57.6ms 101: 70.4ms 110: 83.2ms 111: 96ms
0x90	1	SYS_CTRL_2	7	VBUS_SAFE0V_DET_EN	1	RW	VBUS Safe0V detection 0: Disable detection 1: Enable detection (default)
			6	Reserved	0	RW	Reserved
			5	VCONN_DISCHARGE_EN	0	RW	Discharge at VCONN pin (pin 6) when there is VCONN fault. 0: No discharge (default) 1: Discharge when there is VCONN fault
			4:3	Reserved	00	RW	Reserved
			2	VBUS_VALID_DET_EN	1	RW	VBUS valid detection 0: Disable detection 1: Enable detection (default)
			1	VBUS_PRESENT_DET_EN	1	RW	VBUS present detection 0: Disable detection 1: Enable detection (default)
			0	Reserved	1	RW	Reserved

Address	Length	Register Name	Bit	Bit Name	Default	Type	Description
0x91	1	RT_MASK_1	7	M_VBUS_FRS_LOW	0	RW	0: Interrupt masked (default) 1: Interrupt unmasked
			6	M_RX_FRS	0	RW	0: Interrupt masked (default) 1: Interrupt unmasked
			5	M_VBUS_VALID	0	RW	0: Interrupt masked (default) 1: Interrupt unmasked
			4	M_LEGACY_CABLE_CC2	0	RW	0: Interrupt masked (default) 1: Interrupt unmasked
			3	M_LEGACY_CABLE_CC1	0	RW	0: Interrupt masked (default) 1: Interrupt unmasked
			2	Reserved	0	RW	Reserved
			1	M_VBUS_SAFE0V	0	RW	0: Interrupt masked (default) 1: Interrupt unmasked
			0	M_WAKEUP	0	RW	0: Interrupt masked (default) 1: Interrupt unmasked
0x92	1	RT_MASK2	7	Reserved	0	RW	Reserved
			6	M_VCONN_SAFE0V	0	RW	0: Interrupt masked (default) 1: Interrupt unmasked
			5	M_VCONN_SHT_GND	0	RW	0: Interrupt masked (default) 1: Interrupt unmasked
			4	M_VCONN_UVP	0	RW	0: Interrupt masked (default) 1: Interrupt unmasked
			3	Reserved	0	RW	Reserved
			2	M_VCONN_RVP	0	RW	0: Interrupt masked (default) 1: Interrupt unmasked
			1	M_VCONN_OV_CC2	0	RW	0: Interrupt masked (default) 1: Interrupt unmasked
			0	M_VCONN_OV_CC1	0	RW	0: Interrupt masked (default) 1: Interrupt unmasked
0x93	1	RT_MASK3	7	M_CMP_VBUS_TO_CC2	0	RW	0: Interrupt masked (default) 1: Interrupt unmasked
			6	M_CMP_VBUS_TO_CC1	0	RW	0: Interrupt masked (default) 1: Interrupt unmasked
			5	M_TX_DISCARD_TIMEOUT	0	RW	0: Interrupt masked (default) 1: Interrupt unmasked
			4	M_CABLE_TYPE	0	RW	0: Interrupt masked (default) 1: Interrupt unmasked
			3:0	Reserved	0000	RW	Reserved

Address	Length	Register Name	Bit	Bit Name	Default	Type	Description
0x96	1	RT_MASK6	7	M_BC12_SNK_DONE	0	RW	0: Interrupt masked (default) 1: Interrupt unmasked
			6	M_HVDCP_CHK_DONE	0	RW	0: Interrupt masked (default) 1: Interrupt unmasked
			5	M_BC12_TA_CHG	0	RW	0: Interrupt masked (default) 1: Interrupt unmasked
			4:3	Reserved	00	RW	Reserved
			2	M_SBUDPDM_SW	0	RW	0: Interrupt masked (default) 1: Interrupt unmasked
			1	Reserved	0	RW	Reserved
			0	M_ADC_DONE	0	RW	0: Interrupt masked (default) 1: Interrupt unmasked
0x97	1	RT_MASK7	7	M_VDC_UVP	0	RW	0: Interrupt masked (default) 1: Interrupt unmasked
			6	M_TIMER_TIMEOUT	0	RW	0: Interrupt masked (default) 1: Interrupt unmasked
			5:0	Reserved	000000	RW	Reserved
0x98	1	RT_INT1	7	INT_VBUS_FRS_LOW	0	RW	0: Cleared (default) 1: Fast role swap Vbus valid falling (< 4.75V)
			6	INT_RX_FRS	0	RW	0: Cleared (default) 1: Fast-role swap Rx detection alert.
			5	INT_VBUS_VALID	0	RW	0: Cleared (default) 1: VBUS VALID rising or falling
			4	INT_LEGACY_CABLE_CC2	0	RW	0: Cleared (default) 1: Legacy cable status change
			3	INT_LEGACY_CABLE_CC1	0	RW	0: Cleared (default) 1: Legacy cable status change
			2	Reserved	0	RW	Reserved
			1	INT_VBUS_SAFE0V	0	RW	0: Cleared (default) 1: VBUS under 0.8V
			0	INT_WAKEUP	0	RW	0: Cleared (default) 1: Exit low-power mode

Address	Length	Register Name	Bit	Bit Name	Default	Type	Description
0x99	1	RT_INT2	7	Reserved	0	RW	Reserved
			6	INT_VCONN_SAFE0V	0	RW	0: Cleared or No VCONN_SAFE0V flag rising (default) 1: VCONN voltage drop from greater than 0.8V to lower than 0.8V.
			5	INT_VCONN_SHT_GND	0	RW	0: Cleared (default) 1: VCONN pre short to ground
			4	INT_VCONN_UVP	0	RW	0: Cleared (default) 1: VCONN voltage less than VCONN_INVALID (2.7V) when VCONN_UVP_SEL = 0 (0x8A[5]), or VCONN voltage less than VCONN_PRESENT (2.4V) when VCONN_UVP_SEL = 1 (0x8A[5])
			3	Reserved	0	RW	Reserved
			2	INT_VCONN_RVP	0	RW	0: Cleared (default) 1: VCONN RVP event is detected.
			1	INT_VCONN_OV_CC2	0	RW	0: Cleared (default) 1: CC2 OVP event is detected.
			0	INT_VCONN_OV_CC1	0	RW	0: Cleared (default) 1: CC1 OVP event is detected.
0x9A	1	RT_INT3	7	INT_CMP_VBUS_TO_CC2	0	RW	0: Cleared (default) 1: VBUS to CC voltage detection (> 3.45V)
			6	INT_CMP_VBUS_TO_CC1	0	RW	0: Cleared (default) 1: VBUS to CC voltage detection (> 3.45V)
			5	INT_TX_DISCARD_TIMEOUT	0	RW	Indicate TX_DISCARD interrupt is caused by TXINT_TIMER timeout. 0: Cleared (default) 1: TX DISCARD TIMEOUT
			4	INT_CTD	0	RW	0: Cleared (default) 1: Cable type detect done indication.
			3:0	Reserved	0000	RW	Reserved

Address	Length	Register Name	Bit	Bit Name	Default	Type	Description
0x9D	1	RT_INT6	7	INT_BC12_SNK_DONE	0	RW	0: Cleared (default) 1: BC12 sink flow done
			6	INT_HVDCP_CHK_DONE	0	RW	0: Cleared (default) 1: HVDCP flow check done (sink side)
			5	INT_BC12_TA_CHG	0	RW	0: Cleared (default) 1: BC12 source flow status change (CDP)
			4:3	Reserved	00	RW	Reserved
			2	INT_SBUDPDM_SW	0	RW	0: Cleared (default) 1: SBU/DPDM switch status change
			1	Reserved	0	RW	Reserved
			0	INT_ADC_DONE	0	RW	0: Cleared (default) 1: ADC done
0x9E	1	RT_INT7	7	INT_VDC_UVP	0	RW	0: Cleared (default) 1: VDC UVP flag rising/falling interrupt
			6	INT_TIMER_TIMEOUT	0	RW	0: Cleared (default) 1: Timer count reach
			5:0	Reserved	000000	RW	Reserved
0x9F	1	RT_ST1	7	VBUS_FRS_LOW	0	R	VBUS FRS voltage detection 0: VBUS < VREF_VBUS_FRS (default) 1: VBUS > VREF_VBUS_FRS
			6	RX_FRS	0	R	Fast-role swap RX detection alert. 0: CC > VREF_RX_FR (default) 1: CC < VREF_RX_FR
			5	VBUS_VALID	0	R	0: When VBUS voltage is lower than VREF_VBUS_VALID (default) 1: When VBUS voltage is higher than VREF_VBUS_VALID
			4	LEGACY_CABLE_CC2	0	R	Legacy cable detection 0: No legacy cable on CC2 (default) 1: Legacy cable on CC2
			3	LEGACY_CABLE_CC1	0	R	Legacy cable detection 0: No legacy cable on CC1 (default) 1: Legacy cable on CC1
			2	Reserved	0	R	Reserved
			1	VBUS_SAFE0V	0	R	0: When VBUS voltage is higher than 0.8V. (default) 1: When VBUS voltage is lower than 0.8V.
			0	Reserved	0	R	Reserved

Address	Length	Register Name	Bit	Bit Name	Default	Type	Description
0xA0	1	RT_ST2	7	Reserved	0	R	Reserved
			6	VCONN_ SAFE0V	0	R	VCONN compares to 0.8V result 0: indicate VCONN voltage at CC is higher than 0.8V (default) 1: indicate VCONN voltage at CC is less than 0.8V
			5	VCONN_SHT_ GND	0	R	VCONN-short-to-GND means VCONN at CC is not higher than 2.4V after VCONN_SHT_GND_TIMER when VCONN_EN is enabled. 0: No VCONN short to GND (default) 1: VCONN short to GND
			4	VCONN_UVP	0	R	VCONN undervoltage protect 0: VCONN voltage at CC is higher than VCONN_INVALID (2.7V) when VCONN_UVP_SEL = 0 (0x8A[5]), or VCONN voltage higher than VCONN_PRESENT (2.4V) when VCONN_UVP_SEL = 1 (0x8A[5]) (default) 1: VCONN voltage at CC is less than VCONN_INVALID (2.7V) when VCONN_UVP_SEL = 0 (0x8A[5]), or VCONN voltage is less than VCONN_PRESENT (2.4V) when VCONN_UVP_SEL = 1 (0x8A[5])
			3	VCONN_OCP_ FLAG	0	R	0: VCONN current is lower than VCONN_OCP_SEL setting. (default) 1: VCONN current is higher than VCONN_OCP_SEL setting.
			2	VCONN_RVP	0	R	When CC (selected for VCONN) voltage is higher than VCONN, VCONN RV event will occur. 0: No VCONN RV occurs (default) 1: VCONN RV occurs.
			1	VCONN_OV_ CC2	0	R	0: CC2 voltage is lower than 5.7V. (default) 1: CC2 voltage is higher than 5.75V. Note: This bit works when VCONN_OVP_EN_CC2 is enabled.
			0	VCONN_OV_ CC1	0	R	0: CC1 voltage is lower than 5.7V. (default) 1: CC1 voltage is higher than 5.75V. Note: This bit works when VCONN_OVP_EN_CC1 is enabled.

Address	Length	Register Name	Bit	Bit Name	Default	Type	Description
0xA1	1	RT_ST3	7	CMP_VBUS_TO_CC2	0	R	Result of VBUS short to CC2 detection. 0: CC2 voltage is less than 3.45V. (default) 1: CC2 voltage is higher than 3.45V. Note: This bit works when CMPEN_VBUS_TO_CC2 is set to 1.
			6	CMP_VBUS_TO_CC1	0	R	Result of VBUS short to CC1 detection. 0: CC1 voltage is less than 3.45V. (default) 1: CC1 voltage is higher than 3.45V. Note: This bit works when CMPEN_VBUS_TO_CC1 is set to 1.
			5	CABLE_TYPEA	0	R	Cable Type-A detect result. 0: No Type-A indication or cable type detection not done yet (default) 1: Type-A indication
			4	CABLE_TYPEC	0	R	Cable Type C detect result. 0: No Type-C indication or cable type detection not done yet (default) 1: Type-C
			3:0	Reserved	0000	R	Reserved
0xA4	1	RT_ST6	7	BC12_SNK_DONE	0	R	0: Cleared (default) 1: BC12 sink flow done
			6	HVDCP_CHK_DONE	0	R	0: Cleared (default) 1: HVDCP flow check done (sink side)
			5	BC12_TA_CHG	0	R	0: Cleared (default) 1: BC12 source flow status change (CDP/ private protocol) Note: This flag only keeps 0.33μs.
			4:3	Reserved	00	R	Reserved
			2	SBUDPDM_SW	0	R	0: Cleared (default) 1: SBU/DPDM switch status change Note: This flag only keeps 0.33μs
			1:0	Reserved	00	R	Reserved
0xA5	1	RT_ST7	7	VDC_UVP	0	R	0: No action or not done yet (default) 1: VDC UVP flag
			6:0	Reserved	0000000	R	Reserved

Address	Length	Register Name	Bit	Bit Name	Default	Type	Description
0xA6	1	RT_MASK8	7	MASK_BGOK_CHG	0	RW	0: Interrupt masked (default) 1: Interrupt unmasked
			6	MASK_GPIO3_F	0	RW	0: Interrupt masked (default) 1: Interrupt unmasked
			5	MASK_GPIO2_F	0	RW	0: Interrupt masked (default) 1: Interrupt unmasked
			4	MASK_GPIO1_F	0	RW	0: Interrupt masked (default) 1: Interrupt unmasked
			3	Reserved	0	RW	Reserved
			2	MASK_GPIO3_R	0	RW	0: Interrupt masked (default) 1: Interrupt unmasked
			1	MASK_GPIO2_R	0	RW	0: Interrupt masked (default) 1: Interrupt unmasked
			0	MASK_GPIO1_R	0	RW	0: Interrupt masked (default) 1: Interrupt unmasked
0xA7	1	RT_MASK9	7:5	Reserved	000	RW	Reserved
			4	MASK_VBUS_RC3	0	RW	0: Interrupt masked (default) 1: Interrupt unmasked
			3	MASK_VBUS_RC2	0	RW	0: Interrupt masked (default) 1: Interrupt unmasked
			2	MASK_VBUS_RC1	0	RW	0: Interrupt masked (default) 1: Interrupt unmasked
			1	MASK_VBUS_OC3	0	RW	0: Interrupt masked (default) 1: Interrupt unmasked
			0	MASK_VBUS_OC2	0	RW	0: Interrupt masked (default) 1: Interrupt unmasked
0xA8	1	RT_INT8	7	INT_BGOK_CHG	0	RW	0: No action (default) 1: BGOK Status change
			6	INT_GPIO3_F	0	RW	0: No action (default) 1: GPIO3 falling
			5	INT_GPIO2_F	0	RW	0: No action (default) 1: GPIO2 falling
			4	INT_GPIO1_F	0	RW	0: No action (default) 1: GPIO1 falling
			3	Reserved	0	RW	Reserved
			2	INT_GPIO3_R	0	RW	0: No action (default) 1: GPIO3 rising
			1	INT_GPIO2_R	0	RW	0: No action (default) 1: GPIO2 rising
			0	INT_GPIO1_R	0	RW	0: No action (default) 1: GPIO1 rising

Address	Length	Register Name	Bit	Bit Name	Default	Type	Description
0xA9	1	RT_INT9	7:5	Reserved	000	RW	Reserved
			4	INT_VBUS_RC3	0	RW	0: No action (default) 1: VBUS RCP3 occurs Note: This bit can only be cleared when VBUS RCP3 event disappears
			3	Reserved	0	RW	Reserved
			2	INT_VBUS_RC1	0	RW	0: No action (default) 1: VBUS RCP1 occurs Note: This bit can only be cleared when VBUS RCP1 event disappears
			1	INT_VBUS_OC3	0	RW	0: No action (default) 1: VBUS OCP3 occurs Note: This bit can only be cleared when VBUS OCP3 event disappears
			0	INT_VBUS_OC2	0	RW	0: No action (default) 1: VBUS OCP2 occurs Note: This bit can only be cleared when VBUS OCP2 event disappears
0xAA	1	RT_ST8	7	BGOK	0	R	BGOK status 0: BG not ok (default) 1: BG ok
			6	GPIO3_I	0	R	GPIO3 input data 0: Input low (default) 1: Input high
			5	GPIO2_I	0	R	GPIO2 input data 0: Input low (default) 1: Input high
			4	GPIO1_I	0	R	GPIO1 input data 0: Input low (default) 1: Input high
			3	Reserved	0	R	Reserved
			2	GPIO3_I	0	R	GPIO3 input data 0: Input low (default) 1: Input high
			1	GPIO2_I	0	R	GPIO2 input data 0: Input low (default) 1: Input high
			0	GPIO1_I	0	R	GPIO1 I input data 0: Input low (default) 1: Input high

Address	Length	Register Name	Bit	Bit Name	Default	Type	Description
0xAB	1	RT_ST9	7:5	Reserved	000	R	Reserved
			4	VBUS_RC3	0	R	VBUS RCP3 flag 0: No VBUS RCP3 event occurs (default) 1: VBUS RCP3 occur
			3	Reserved	0	R	Reserved
			2	VBUS_RC1	0	R	VBUS RCP1 flag 0: No VBUS RCP1 event occurs (default) 1: VBUS RCP1 occur
			1	VBUS_OC3	0	R	VBUS OCP3 flag 0: No VBUS OCP3 event occurs (default) 1: VBUS OCP3 occur
			0	VBUS_OC2	0	R	VBUS OCP2 flag 0: No VBUS OCP2 event occurs (default) 1: VBUS OCP2 occur
0xAF	1	TIMER_ CTRL	7	TIMER_EN	0	RW	Timer enable 0: Disable (default) 1: Enable
			6:4	Reserved	000	R	Reserved
			3:0	TIMER_SEL	1011	RW	Timer count select 0000: 0.4s 0001: 0.8s … 1011: 4.8s (default) … 1110: 6.0s 1111: 6.4s
0xB0	1	SYS_ CTRL3	7:1	Reserved	0000000	R	Reserved
			0	SOFT_RESET	0	W	When writing 1b to this bit, it will trigger soft-reset event, and all register setting will reset to default value.
0xB2	1	TCPC_ CTRL2	7:4	Reserved	0000	R	Reserved
			3:0	TDRP	0011	RW	During the period, a DRP will complete a source to sink and back advertisement. (Period = TDRP * 6.4 + 51.2ms) 0000: 51.2ms 0001: 57.6ms 0010: 64ms 0011: 70.4ms (default) … 1110: 140.8ms 1111: 147.2ms

Address	Length	Register Name	Bit	Bit Name	Default	Type	Description
0xB3	1	TCPC_ CTRL3	7:0	DCSRCDRP [7:0]	01000111	RW	The percent of time that a DRP will advertise source during tDRP. (DUTY = (DCSRCDRP[9:0] + 1)/1024) 0000000000: 1/1024 0000000001: 2/1024 … 0101000111: 328/1024 (default) … 1111111110: 1023/1024 1111111111: 1024/1024 Note: Setting with 0xB4[9:8]
0xB4	1	TCPC_ CTRL4	7:2	Reserved	000000	R	Reserved
			1:0	DCSRCDRP [9:8]	01	RW	The percent of time that a DRP will advertise source during tDRP. (DUTY = (DCSRCDRP[9:0] + 1)/1024) 0000000000: 1/1024 0000000001: 2/1024 … 0101000111: 328/1024 (default) … 1111111110: 1023/1024 1111111111: 1024/1024 Note: Setting with 0xB4[9:8]
0xB5	1	TCPC_ CTRL5	7:4	VBUS_ DISCHARGE_ TIME	0111	RW	Time for VBUS force/auto discharge 0000: 6.4ms 0001: 12.8ms 0010: 19.2ms 0011: 25.6ms 0100: 32ms 0101: 38.4ms 0110: 44.8ms 0111: 51.2ms (default) 1000: 76.8ms 1001: 102.4ms 1010: 153.6ms 1011: 204.8ms 1100: 307.2ms 1101: 409.6ms 1110: 524.8ms 1111: 652.8ms
			3:0	Reserved	0000	R	Reserved

Address	Length	Register Name	Bit	Bit Name	Default	Type	Description
0xB6	1	TCPC_CTRL6	7:0	TPDDEBOUNCE	10010110	RW	PD debounce time is the duration a sink port shall wait before it can determine it is detached. (tPDDebounce time = TPDDEBOUNCE * 0.1ms) 00000000: Reserved 00000001: Reserved 00000010: 0.2ms … 10010110: 15ms (default) … 11111110: 25.4ms 11111111: 25.5ms
0xB7	1	TCPC_CTRL7	7:0	TCCDEBOUNCE	10111100	RW	CC debounce time is the duration a port shall wait before it can determine it is attached. (tCCDebounce time = TCCDEBOUNCE * 0.8ms) 00000000: Reserved 00000001: Reserved 00000010: 1.6ms … 10111100: 150.4ms (default) … 11111110: 203.2ms 11111111: 204.0ms
0xB8	1	SYS_CTRL4	7:0	RTINI_REG90	00000000	RW	Pre-determined low power mode setting (0x90) for open source TCPM to enter low power mode when unattached. RT2 0x10[1:0] == 2'b01: TCPM writes 0x1A[6] = 1 will auto update 0x90 = RTINI_REG90. RT2 0x10[1:0] == 2'b10: TCPM writes 0x1A will auto update 0x90 = RTINI_REG90 while CCx_STATUS is open or single RA only. RT2 0x10[1:0] == 2'b11: TCPM writes 0x1A will auto update 0x90 = RTINI_REG90 while CCx_STATUS is open. RT2 0x10[1:0] == 2'b00: No auto update 0x90 = RTINI_REG90

Address	Length	Register Name	Bit	Bit Name	Default	Type	Description
0xBE	1	WATCHDOG_CTRL	7:4	Reserved	0000	RW	Reserved
			3:0	WATCHDOG_SEL	1011	RW	The watchdog timer shall start when any of the interrupts that are not masked in the Alert register are set or when the IRQB pin is asserted. (watchdog timeout time = (WATCHDOG_SEL + 1) * 0.4sec) 0000: 0.4s 0001: 0.8s … 1011: 4.8s (default) … 1110: 6.0s 1111: 6.4s
0xBF	1	I2C_TO_RST_CTRL	7	I2C_TO_RST_EN	0	RW	Set this bit to 1b to enable I^2C reset timer. When I^2C reset timer is enabled, it will monitor SCL and SDA. When SCL and SDA both keep low, I^2C reset timer will start to count. I^2C reset timer will be cleared to 0 when SCL or SDA becomes high. When I^2C reset timer gets timeout, it will trigger soft reset event and all registers will be reset to default value. 0: Disable I^2C reset timer (default) 1: Enable I^2C reset timer
			6:4	Reserved	000	RW	Reserved
			3:0	I2C_TO_RST_SEL	1000	RW	Timeout time for I^2C reset timer (timeout time = (I2C_TO_RST_SEL+1) * 12.5ms) 0000: 12.5ms 0001: 25.0ms … 1000: 112.5ms (default) … 1111: 200ms
0xC8	1	HILO_CTRL9	7:5	VREF_VBUS_VALID	000	RW	VBUS_VALID threshold: 2.6V to 4.0V, LSB = 0.2V 000: 2.6V (default) 001: 2.8V … 110: 3.8V 111: 4.0V
			4:0	Reserved	00000	RW	Reserved

Address	Length	Register Name	Bit	Bit Name	Default	Type	Description
0xCA	1	SHILED_ CTRL1	7:2	Reserved	101000	RW	Reserved
			1	CTD_EN	1	RW	Set this bit to 1b to enable auto cable type detection. For auto cable type detection, it will check if the cable is Type-C or Type-A every time after the cable is plugged in when CC acts as sink. 0: Disable auto cable type detection 1: Enable auto cable type detection (default)
			0	Reserved	1	RW	Reserved
0xCB	1	FRS_ CTRL1	7:4	FRSWAPRX	1100	RW	Initial sink detects FRS TX signal for at least this amount of time. 3.125μs per step (32k). 0000: 0μs 0001: 3.125μs … 1100: 37.5μs (default) … 1111: 46.875μs
			3:2	VREF_RX_ FRS	10	RW	Fast role-swap detection threshold on CC pin 00: 0.48V 01: 0.50V 10: 0.52V (default) 11: 0.54V
			1:0	Reserved	00	R	Reserved
0xCC	1	FRS_CTRL 2	7	Reserved	0	RW	Reserved
			6	RX_FRS_EN	0	RW	Fast-role swap RX detection enable 0: Disable (default) 1: Enable
			5	Reserved	0	RW	Reserved
			4	FR_VBUS_ SELECT	1	RW	FR_VBUS_FLAG de-bounce status 0: Not de-bounce FR_VBUS_VALID is not de-bounced 1: FR_VBUS_VALID is de-bounced (default)
			3	VBUS_FRS_ EN	0	RW	VBUSfast role-swap detection enable 0: Disable (default) 1: Enable

Address	Length	Register Name	Bit	Bit Name	Default	Type	Description
			2:0	VREF_VBUS_FRS	000	RW	VBUS fast role-swap detection threshold selection 000: 4.8V (default) 001: 4.9V 010: 5.0V 011: 5.1V 100: 5.2V 101: 5.3V 110: 5.4V 111: 5.5V

Address	Length	Register Name	Bit	Bit Name	Default	Type	Description
0xCE	1	FRS_CTRL3	7:4	Reserved	0000	R	Reserved
			3	FRS_RX_WAIT_GPIO2	0	RW	GPIO2 reload when receiving fast role swap event 0: Reload setting when receiving fast role swap event (default) 1: Reload setting when receiving fast role swap event and VBUS < VREF_VBUS_FRS
			2	FRS_RX_WAIT_GPIO1	0	RW	GPIO1 reload when receiving fast role swap event 0: Reload setting when receiving fast role swap event (default) 1: Reload setting when receiving fast role swap event and VBUS < VREF_VBUS_FRS
			1	FRS_RX_WAIT_GPB	0	RW	GPB reload when receiving fast role swap event 0: Reload setting when receiving fast role swap event (default) 1: Reload setting when receiving fast role swap event and VBUS < VREF_VBUS_FRS
			0	FRS_RX_WAIT_GPA	0	RW	GPA reload when receiving fast role swap event 0: Reload setting when receiving fast role swap event (default) 1: Reload setting when receiving fast role swap event and VBUS < VREF_VBUS_FRS
0xDD	1	VBUS_PATH_CTRL	7:4	GPB_CTRL	1000	RW	Path control for GPB 0000: Pull-down with 50μA 0001: Pull-down with 250μA 0010: Pull-down with 8kΩ 0011: Pull-down with 200μA 01x0: Pull-up with 50μA 01x1: Pull-up with 200μA 1xxx: Floating (default)
			3:0	GPA_CTRL	1000	RW	Path control for GPA 0000: Pull-down with 50μA 0001: Pull-down with 250μA 0010: Pull-down with 8kΩ 0011: Pull-down with 200μA 01x0: Pull-up with 50μA 01x1: Pull-up with 200μA 1xxx: Floating (default)

Address	Length	Register Name	Bit	Bit Name	Default	Type	Description
0xDE	1	DIS_SNK_VBUS_CTRL	7:4	DIS_SNK_VBUS_GPB	1000	RW	Path control for GPB when receiving TCPM disable sink VBUS command (0x23 = 44h) 0000: Pull-down with 50μA 0001: Pull-down with 250μA 0010: Pull-down with 8kΩ 0011: Pull-down with 200μA 01x0: Pull-up with 50μA 01x1: Pull-up with 200μA 1xxx: Floating (default)
			3:0	DIS_SNK_VBUS_GPA	1000	RW	Path control for GPA when receiving TCPM disable sink VBUS command (0x23 = 44h) 0000: Pull-down with 50μA 0001: Pull-down with 250μA 0010: Pull-down with 8kΩ 0011: Pull-down with 200μA 01x0: Pull-up with 50μA 01x1: Pull-up with 200μA 1xxx: Floating (default)
0xDF	1	ENA_SNK_VBUS_CTRL	7:4	ENA_SNK_VBUS_GPB	1000	RW	Path control for GPB when receiving TCPM enable sink VBUS command (0x23 = 55h) 0000: Pull-down with 50μA 0001: Pull-down with 250μA 0010: Pull-down with 8kΩ 0011: Pull-down with 200μA 01x0: Pull-up with 50μA 01x1: Pull-up with 200μA 1xxx: Floating (default)
			3:0	ENA_SNK_VBUS_GPA	1000	RW	Path control for GPA when receiving TCPM enable sink VBUS command (0x23 = 55h) 0000: Pull-down with 50μA 0001: Pull-down with 250μA 0010: Pull-down with 8kΩ 0011: Pull-down with 200μA 01x0: Pull-up with 50μA 01x1: Pull-up with 200μA 1xxx: Floating (default)

Address	Length	Register Name	Bit	Bit Name	Default	Type	Description
0xE0	1	DIS_SRC_VBUS_CTRL	7:4	DIS_SRC_VBUS_GPB	1000	RW	Path control for GPB when receiving TCPM disable source VBUS command (0x23 = 66h) 0000: Pull-down with 50μA 0001: Pull-down with 250μA 0010: Pull-down with 8kΩ 0011: Pull-down with 200μA 01x0: Pull-up with 50μA 01x1: Pull-up with 200μA 1xxx: Floating (default)
			3:0	DIS_SRC_VBUS_GPA	1000	RW	Path control for GPA when receiving TCPM disable sink VBUS command (0x23 = 66h) 0000: Pull-down with 50μA 0001: Pull-down with 250μA 0010: Pull-down with 8kΩ 0011: Pull-down with 200μA 01x0: Pull-up with 50μA 01x1: Pull-up with 200μA 1xxx: Floating (default)
0xE1	1	ENA_SRC_VBUS_CTRL	7:4	ENA_SRC_VBUS_GPB	1000	RW	Path control for GPB when receiving TCPM enable source VBUS command (0x23 = 77h) 0000: Pull-down with 50μA 0001: Pull-down with 250μA 0010: Pull-down with 8kΩ 0011: Pull-down with 200μA 01x0: Pull-up with 50μA 01x1: Pull-up with 200μA 1xxx: Floating (default)
			3:0	ENA_SRC_VBUS_GPA	1000	RW	Path control for GPA when receiving TCPM enable source VBUS command (0x23 = 77h) 0000: Pull-down with 50μA 0001: Pull-down with 250μA 0010: Pull-down with 8kΩ 0011: Pull-down with 200μA 01x0: Pull-up with 50μA 01x1: Pull-up with 200μA 1xxx: Floating (default)

Address	Length	Register Name	Bit	Bit Name	Default	Type	Description
0xE2	1	ENA_SRC_HV_VBUS_CTRL	7:4	ENA_SRC_HV_VBUS_GPB	1000	RW	Path control for GPB when receiving enable source HV VBUS command (0x23 = 88h) 0000: Pull-down with 50μA 0001: Pull-down with 250μA 0010: Pull-down with 8kΩ 0011: Pull-down with 200μA 01x0: Pull-up with 50μA 01x1: Pull-up with 200μA 1xxx: Floating (default)
			3:0	ENA_SRC_HV_VBUS_GPA	1000	RW	Path control for GPA when receiving enable source HV VBUS command (0x23 = 88h) 0000: Pull-down with 50μA 0001: Pull-down with 250μA 0010: Pull-down with 8kΩ 0011: Pull-down with 200μA 01x0: Pull-up with 50μA 01x1: Pull-up with 200μA 1xxx: Floating (default)
0xE3	1	FAULT_OC1_VBUS_CTRL	7:4	FAULT_OC1_VBUS_GPB	1000	RW	Path control for GPB when VBUS OC1 occurs 0000: Pull-down with 50μA 0001: Pull-down with 250μA 0010: Pull-down with 8kΩ 0011: Pull-down with 200μA 01x0: Pull-up with 50μA 01x1: Pull-up with 200μA 1xxx: Floating (default)
			3:0	FAULT_OC1_VBUS_GPA	1000	RW	Path control for GPA when VBUS OC1 occurs 0000: Pull-down with 50μA 0001: Pull-down with 250μA 0010: Pull-down with 8kΩ 0011: Pull-down with 200μA 01x0: Pull-up with 50μA 01x1: Pull-up with 200μA 1xxx: Floating (default)

Address	Length	Register Name	Bit	Bit Name	Default	Type	Description
0xE4	1	FAULT_OC2_VBUS_CTRL	7:4	FAULT_OC2_VBUS_GPB	1000	RW	Path control for GPB when VBUS OC2 occurs 0000: Pull-down with 50μA 0001: Pull-down with 250μA 0010: Pull-down with 8kΩ 0011: Pull-down with 200μA 01x0: Pull-up with 50μA 01x1: Pull-up with 200μA 1xxx: Floating (default)
			3:0	FAULT_OC2_VBUS_GPA	1000	RW	Path control for GPA when VBUS OC2 occrrs 0000: Pull-down with 50μA 0001: Pull-down with 250μA 0010: Pull-down with 8kΩ 0011: Pull-down with 200μA 01x0: Pull-up with 50μA 01x1: Pull-up with 200μA 1xxx: Floating (default)
0xE5	1	FAULT_OC3_VBUS_CTRL	7:4	FAULT_OC3_VBUS_GPB	1000	RW	Path control for GPB when VBUS OC3 occurs 0000: Pull-down with 50μA 0001: Pull-down with 250μA 0010: Pull-down with 8kΩ 0011: Pull-down with 200μA 01x0: Pull-up with 50μA 01x1: Pull-up with 200μA 1xxx: Floating (default)
			3:0	FAULT_OC3_VBUS_GPA	1000	RW	Path control for GPA when VBUS OC3 occurs 0000: Pull-down with 50μA 0001: Pull-down with 250μA 0010: Pull-down with 8kΩ 0011: Pull-down with 200μA 01x0: Pull-up with 50μA 01x1: Pull-up with 200μA 1xxx: Floating (default)

Address	Length	Register Name	Bit	Bit Name	Default	Type	Description
0xE6	1	FAULT_OV_VBUS_CTRL	7:4	FAULT_OV_VBUS_GPB	1000	RW	Path control for GPB when VBUS OV occurs 0000: Pull-down with 50μA 0001: Pull-down with 250μA 0010: Pull-down with 8kΩ 0011: Pull-down with 200μA 01x0: Pull-up with 50μA 01x1: Pull-up with 200μA 1xxx: Floating (default)
			3:0	FAULT_OV_VBUS_GPA	1000	RW	Path control for GPA when VBUS OV occurs 0000: Pull-down with 50μA 0001: Pull-down with 250μA 0010: Pull-down with 8kΩ 0011: Pull-down with 200μA 01x0: Pull-up with 50μA 01x1: Pull-up with 200μA 1xxx: Floating (default)
0xE7	1	FAULT_RC_VBUS_CTRL	7:4	FAULT_RC_VBUS_GPB	1000	RW	Path control for GPB when VBUS RC occurs 0000: Pull-down with 50μA 0001: Pull-down with 250μA 0010: Pull-down with 8kΩ 0011: Pull-down with 200μA 01x0: Pull-up with 50μA 01x1: Pull-up with 200μA 1xxx: Floating (default)
			3:0	FAULT_RC_VBUS_GPA	1000	RW	Path control for GPA when VBUS RC occurs 0000: Pull-down with 50μA 0001: Pull-down with 250μA 0010: Pull-down with 8kΩ 0011: Pull-down with 200μA 01x0: Pull-up with 50μA 01x1: Pull-up with 200μA 1xxx: Floating (default)

Address	Length	Register Name	Bit	Bit Name	Default	Type	Description
0xE9	1	FRS_RX_VBUS_CTRL	7:4	FRS_RX_VBUS_GPB	1000	RW	Path control for GPB when receiving fast role swap event 0000: Pull-down with 50μA 0001: Pull-down with 250μA 0010: Pull-down with 8kΩ 0011: Pull-down with 200μA 01x0: Pull-up with 50μA 01x1: Pull-up with 200μA 1xxx: Floating (default)
			3:0	FRS_RX_VBUS_GPA	1000	RW	Path control for GPA when receiving fast role swap event 0000: Pull-down with 50μA 0001: Pull-down with 250μA 0010: Pull-down with 8kΩ 0011: Pull-down with 200μA 01x0: Pull-up with 50μA 01x1: Pull-up with 200μA 1xxx: Floating (default)
0xEA	1	GPIO1_VBUS_CTRL	7	Reserved	0	R	Reserved
			6	FRS_RX_VBUS_GPIO1	0	RW	Path control for GPIO1 when receiving fast role swap event 0: Push-pull output 0 (default) 1: Push-pull output 1
			5	Reserved	0	R	Reserved
			4	ENA_SRC_HV_VBUS_GPIO1	0	RW	Path control for GPIO1 when receiving enable source HV VBUS command (0x23 = 88h) 0: Push-pull output 0 (default) 1: Push-pull output 1
			3	ENA_SRC_VBUS_GPIO1	0	RW	Path control for GPIO1 when receiving TCPM enable source VBUS command (0x23 = 77h) 0: Push-pull output 0 (default) 1: Push-pull output 1
			2	DIS_SRC_VBUS_GPIO1	0	RW	Path control for GPIO1 when receiving TCPM disable source VBUS command (0x23 = 66h) 0: Push-pull output 0 (default) 1: Push-pull output 1
			1	ENA_SNK_VBUS_GPIO1	0	RW	Path control for GPIO1 when receiving TCPM enable sink VBUS command (0x23 = 55h) 0: Push-pull output 0 (default) 1: Push-pull output 1
			0	DIS_SNK_VBUS_GPIO1	0	RW	Path control for GPIO1 when receiving TCPM disable sink VBUS command (0x23 = 44h) 0: Push-pull output 0 (default) 1: Push-pull output 1

Address	Length	Register Name	Bit	Bit Name	Default	Type	Description
0xEB	1	GPIO2_VBUS_CTRL	7	Reserved	0	R	Reserved
			6	FRS_RX_VBUS_GPIO2	0	RW	Path control for GPIO2 when receiving fast role swap event 0: Push-pull output 0 (default) 1: Push-pull output 1
			5	Reserved	0	R	Reserved
			4	ENA_SRC_HV_VBUS_GPIO2	0	RW	Path control for GPIO2 when receiving enable source HV VBUS command (0x23 = 88h) 0: Push-pull output 0 (default) 1: Push-pull output 1
			3	ENA_SRC_VBUS_GPIO2	0	RW	Path control for GPIO2 when receiving TCPM enable source VBUS command (0x23 = 77h) 0: Push-pull output 0 (default) 1: Push-pull output 1
			2	DIS_SRC_VBUS_GPIO2	0	RW	Path control for GPIO2 when receiving TCPM disable source VBUS command (0x23 = 66h) 0: Push-pull output 0 (default) 1: Push-pull output 1
			1	ENA_SNK_VBUS_GPIO2	0	RW	Path control for GPIO2 when receiving TCPM enable sink VBUS command (0x23 = 55h) 0: Push-pull output 0 (default) 1: Push-pull output 1
			0	DIS_SNK_VBUS_GPIO2	0	RW	Path control for GPIO2 when receiving TCPM disable sink VBUS command (0x23 = 44h) 0: Push-pull output 0 (default) 1: Push-pull output 1

Address	Length	Register Name	Bit	Bit Name	Default	Type	Description
0xEC	1	VBUS_CTRL_EN	7	GPIO2_VBUS_PATH_EN	0	RW	GPIO2 setting (GPIO2_OD_N/GPIO2_OE/GPIO2_O) auto reload with TCPC command and FRS event 0: GPIO2 setting (GPIO2_OD_N/GPIO2_OE/GPIO2_O) will not auto reload (default) 1: GPIO2 setting (GPIO2_OD_N/GPIO2_OE/GPIO2_O) will auto reload
			6	GPIO1_VBUS_PATH_EN	0	RW	GPIO1 setting (GPIO1_OD_N/GPIO1_OE/GPIO1_O) auto reload with TCPC command and FRS event 0: GPIO1 setting (GPIO1_OD_N/GPIO1_OE/GPIO1_O) will not auto reload (default) 1: GPIO1 setting (GPIO1_OD_N/GPIO1_OE/GPIO1_O) will auto reload
			5	GPB_VBUS_PATH_EN	1	RW	GPB setting (GPB_CTRL) auto reload with TCPC command, VBUS OV/OC/RC event, and FRS event 0: GPB setting (GPB_CTRL) will not auto reload 1: GPB setting (GPB_CTRL) will auto reload (default)
			4	GPA_VBUS_PATH_EN	1	RW	GPA setting (GPA_CTRL) auto reload with TCPC command, VBUS OV/OC/RC event, and FRS event 0: GPA setting (GPA_CTRL) will not auto reload 1: GPA setting (GPA_CTRL) will auto reload (default)
			3	VBUS_CPGPB_AUTO_OFF	1	RW	Auto disable VBUS charge pump for GPB when in low power mode 0: Not auto disable 1: Auto disable when in low power mode (default)
			2	VBUS_CPGPA_AUTO_OFF	1	RW	Auto disable VBUS charge pump for GPB when in low power mode 0: Not auto disable 1: Auto disable when in low power mode (default)
			1	VBUS_CPGPB_EN	1	RW	VBUS charge pump for GPB 0: Disable 1: Enable (default)
			0	VBUS_CPGPA_EN	1	RW	VBUS charge pump for GPA 0: Disable 1: Enable (default)

Address	Length	Register Name	Bit	Bit Name	Default	Type	Description
0xED	1	GPIO1_CTRL	7	GPIO1_DG_EN	0	RW	Deglitch for GPIO1 input 0: No deglitch (default) 1: Enable deglitch (3μs)
			6	GPIO1_SMT	0	RW	GPIO1 enable input data detection with Schmitter trigger hysteresis 0: Disable (default) 1: Enable
			5	GPIO1_PU	0	RW	GPIO1 internal pull-high enable 0: Disable (default) 1: Enable
			4	GPIO1_PD	0	RW	GPIO1 internal pull-low enable 0: Disable (default) 1: Enable
			3	GPIO1_OD_N	0	RW	GPIO1 push-pull/open-drain select 0: Open-drain (default) 1: Push-pull
			2	GPIO1_OE	0	RW	GPIO1 output data enable 0: GPIO1 as input (default) 1: GPIO1 as output
			1	GPIO1_O	0	RW	GPIO1 output data 0: GPIO1 output low (default) 1: GPIO1 output high
			0	GPIO1_I	0	R	GPIO1 input data 0: Input low (default) 1: Input high

Address	Length	Register Name	Bit	Bit Name	Default	Type	Description
0xEE	1	GPIO2_CTRL	7	GPIO2_DG_EN	0	RW	Deglitch for GPIO2 input 0: No deglitch (default) 1: Enable deglitch (3μs)
			6	GPIO2_SMT	0	RW	GPIO2 enable Input data detection with Schmitter trigger hysteresis 0: Disable (default) 1: Enable
			5	GPIO2_PU	0	RW	GPIO2 internal pull-high enable 0: Disable (default) 1: Enable
			4	GPIO2_PD	0	RW	GPIO2 internal pull-low enable 0: Disable (default) 1: Enable
			3	GPIO2_OD_N	0	RW	GPIO2 push-pull/open-drain select 0: Open-drain (default) 1: Push-pull
			2	GPIO2_OE	0	RW	GPIO2 output data enable 0: GPIO2 as input (default) 1: GPIO2 as output
			1	GPIO2_O	0	RW	GPIO2 output data 0: GPIO2 output low (default) 1: GPIO2 output high
			0	GPIO2_I	0	R	GPIO2 input data 0: Input low (default) 1: Input high

Address	Length	Register Name	Bit	Bit Name	Default	Type	Description
0xEF	1	GPIO3_CTRL	7	GPIO3_DG_EN	0	RW	Deglitch for GPIO3 input 0: No deglitch (default) 1: Enable deglitch (3μs)
			6	GPIO3_SMT	0	RW	GPIO3 enable input data detection with Schmitter trigger hysteresis 0: Disable (default) 1: Enable
			5	GPIO3_PU	0	RW	GPIO3 internal pull-high enable 0: Disable (default) 1: Enable
			4	GPIO3_PD	0	RW	GPIO3 internal pull-low enable 0: Disable (default) 1: Enable
			3	GPIO3_OD_N	0	RW	GPIO3 Push-pull/open-drain select 0: open-drain (default) 1: push-pull
			2	GPIO3_OE	0	RW	GPIO3 output data enable 0: GPIO3 as input (default) 1: GPIO3 as output
			1	GPIO3_O	0	RW	GPIO3 output data 0: GPIO3 output low (default) 1: GPIO3 output high
			0	GPIO3_I	0	R	GPIO3 input data 0: Input low (default) 1: Input high
0xF2	1	RT2_PAGE	7:0	RT2_PAGE	0x00	RW	Access port to RT2 PAGE

14.2 Page 2 of Register Table

Address	Length	Register Name	Bit	Bit Name	Default	Type	Description
0x10	1	SYS_CTRL5	7	FOD_DISLMT_EN	1	RW	Enable FOD discharge current limit. 0: Disable 1: Enable (default)
			6	LPWR_DRP_ROLE	0	RW	Option to apply LPRW_RPD_CCx (when not toggling) or Toggling Roles (when toggling) to CCx when enabling LPWR DRP and during setup states (st_off, st_start) or stop states (st_stop). When option is offed, LPWR DRP will present CCx open during setup states and stop states. 0: Disable (default) 1: Enable
			5:4	AUTO_LPWR_TIMEOUT	00	RW	These bits can be used to set the time before entering into auto low power. 00: 1.0s (default) 01: 1.5s 10: 2.0s 11: 2.5s
			3	AUTO_OSC_24M_EN	0	RW	Option to auto enable 0x90[0] when IRQB = low. 0: Disable (default) 1: Enable
			2:0	AUTO_LPWR_EN	000	RW	For open source TCPM to enter low power mode when unattached. Auto write low power control register per the below scenario. 000: Disable (default) 100: HW auto update 0x90 = RTINI_REG90 when reach auto low power timeout. Auto low power timer is enabled when TCPC is in normal mode with CCx_Status are both opened and no IRQB event and VBUS_PRESENT = 0. 101: HW auto update 0x90 = RTINI_REG90 when reach auto low power timeout. Auto low power timer is enabled when TCPC is in normal mode with CCx_Status are both opened for sink or CCx_Status has single RA for source and no IRQB event and VBUS_PRESENT = 0. 110/111: Disable The other settings are reserved.

Address	Length	Register Name	Bit	Bit Name	Default	Type	Description
0x11	1	VCON_CTRL4	7:6	Reserved	00	R	Reserved
			5	VCONN_UVP_CP_EN	1	RW	VCONN_INVALID_FLAG action selection: 0: Debounce 1: No debounce (default)
			4	VCONN_OCP_CP_EN	1	RW	VCONN_OCP_FLAG action selection: 0: Debounce 1: No debounce (default)
			3:2	Reserved	00	R	Reserved
			1	CMPEN_VBUS_TO_CC2	0	RW	CC2 short to VBUS detection, the trigger voltage is 3 x 1.15 = 3.45V 0: Disable (default) 1: Enable
			0	CMPEN_VBUS_TO_CC1	0	RW	CC1 short to VBUS detection, the trigger voltage is 3 x 1.15 = 3.45V 0: Disable (default) 1: Enable
0x12	1	VDC_CTRL	7:6	Reserved	00	R	Reserved
			5:4	VDC_VOL	00	RW	VDC undervoltage level selection 00: 0.55V (default) 01: 0.9V 10: 1.5V 11: 2.0V
			3:1	Reserved	000	R	Reserved
			0	VDC_DET_EN	0	RW	VDC detection enable 0: Disable 1: Enable

Address	Length	Register Name	Bit	Bit Name	Default	Type	Description
0x13	1	VBUS_VOL_CTRL	7	Reserved	0	R	Reserved
			6	VBUS_OVP_NODEB	0	RW	VBUS OVP no debounce 0: VBUS OVP has 25μs deglitch (default) 1: VBUS OVP no debounce/deglitch
			5:4	VBUS_OVP_SEL	10	RW	VBUS overvoltage protection level percentage. OVP = VBUS x (100 + X)% 00: X = 5 01: X = 10 10: X = 15 (default) 11: X = 20
			3:0	VBUS_VOL_SEL	1000	RW	VBUS voltage range 0000: 5V 0001: 6V …… 1000: 13V (default) …… 1110: 19V 1111: 20V
0x14	1	VBUS_OCRC_EN	7:5	Reserved	000	R	Reserved
			4	VBUS_OCRC3_EN	0	RW	VBUS OCP3/RCP3 enable setting 0: Disable (default) 1: Enable
			3	Reserved	0	R	Reserved
			2	VBUS_RCP1_EN	0	RW	VBUS RCP1 enable setting 0: Disable (default) 1: Enable
			1	VBUS_OCP2_EN	0	RW	VBUS OCP2 enable setting 0: Disable (default) 1: Enable
			0	VBUS_OCP1_EN	1	R	VBUS OCP1 enable setting 0: Disable 1: Enable (VBUS_OCP1_EN is from TCPC's OCP_EN reg 0x1B) (default)

Address	Length	Register Name	Bit	Bit Name	Default	Type	Description
0x15	1	VBUS_OCRC_STS	7	Reserved	0	R	Reserved
			6	VBUS_RCP3_STS	0	R	VBUS RCP3 status 0: No RCP3 occurs (default) 1: RCP3 occurs
			5	Reserved	0	R	Reserved
			4	VBUS_RCP1_STS	0	R	VBUS RCP1 status 0: No RCP1 occurs (default) 1: RCP1 occurs
			3	Reserved	0	R	Reserved
			2	VBUS_OCP3_STS	0	R	VBUS OCP3 status 0: No OCP3 occurs (default) 1: OCP3 occurs
			1	VBUS_OCP2_STS	0	R	VBUS OCP2 status 0: No OCP2 occurs (default) 1: OCP2 occurs
			0	VBUS_OCP1_STS	0	R	VBUS OCP1 status 0: No OCP1 occurs (default) 1: OCP1 occurs
0x16	1	VBUS_OCP_CTRL1	7	Reserved	0	R	Reserved
			6:0	VBUS_OCP1_SEL	0100010	RW	VBUS OCP1 level selection 0000000: 0.2A 0000001: 0.3A …… 0100010: 3.6A (default) …… 1111110: 12.8A 1111111: 12.9A
0x17	1	VBUS_OCP_CTRL2	7	Reserved	0	R	Reserved
			6:0	VBUS_OCP2_SEL	0100010	RW	VBUS OCP2 level selection 0000000: 0.2A 0000001: 0.3A …… 0100010: 3.6A (default) …… 1111110: 12.8A 1111111: 12.9A
0x18	1	VBUS_OCP_CTRL3	7:2	Reserved	000000	R	Reserved
			1:0	VBUS_OCP3_SEL	10	RW	VBUS OCP3 level selection 00: 7.25A 01: 9A 10: 12A (default) 11: 15A

Address	Length	Register Name	Bit	Bit Name	Default	Type	Description
0x19	1	VBUS_OCP_CRTL4	7	VBUS_OCP1_50MS	0	RW	VBUS OCP1 timer step 0: 10ms/step (default) 1: 50ms/Step
			6:0	VBUS_OCP1_TIME	1010000	RW	VBUS OCP1 detect time period When VBUS OCP is detected over VBUS_OCP1_SEL and remains over this time period, the VBUS_OCP interrupt will be triggered. 0000000: 0 step (trigger interrupt immediately when detected) 0000001: 1 step (10 or 50ms) 0000010: 2 step (20 or 100ms) … 1010000: 80 step (800 or 4000ms) (default) … 1111111: 127 step (1270 or 6350ms)
0x1A	1	VBUS_OCP_CRTL5	7	VBUS_OCP2_50MS	0	RW	VBUS OCP2 timer step 0: 10ms/step (default) 1: 50ms/Step
			6:0	VBUS_OCP2_TIME	1010000	RW	VBUS OCP2 detect time period When VBUS OCP is detected over VBUS_OCP2_SEL and remains over this time period, the VBUS_OCP interrupt will be triggered. 0000000: 0 step (trigger interrupt immediately when detected) 0000001: 1 step (10 or 50ms) 0000010: 2 step (20 or 100ms) … 1010000: 80 step (800 or 4000ms) (default) … 1111111: 127 step (1270 or 6350ms)
0x1B	1	VBUS_RCP_CTRL1	7	Reserved	0	R	Reserved
			6:0	VBUS_RCP1_SEL	0100010	RW	VBUS RCP1 level selection 0000000: –0.2A 0000001: –0.3A …… 0100010: –3.6A(default) …… 1111110: –12.8A 1111111: –12.9A
0x1D	1	VBUS_RCP_CTRL3	7:2	Reserved	000000	R	Reserved
			1:0	VBUS_RCP3_SEL	10	RW	VBUS RCP3 level selection 00: 7.25A 01: 9A 10: 12A (default) 11: 15A

Address	Length	Register Name	Bit	Bit Name	Default	Type	Description
0x1E	1	VBUS_RCP_CRTL4	7	VBUS_RCP1_50MS	0	RW	VBUS RCP1 timer step 0: 10ms/step (default) 1: 50ms/step
			6:0	VBUS_RCP1_TIME	1010000	RW	VBUS RCP1 detect time period When VBUS RCP is detected over VBUS_RCP1_SEL and remains over this time period, the VBUS_RCP interrupt will be triggered. 0000000: 0 step (trigger interrupt immediately when detected) 0000001: 1 step (10 or 50ms) 0000010: 2 step (20 or 100ms) … 1010000: 80 step (800 or 4000ms) (default) … 1111111: 127 step (1270 or 6350ms)
0x1F	1	VBUS_RCP_CRTL5	7:1	Reserved	0000000	R	Reserved
			0	HL_VBUS_SEL_OC	0	RW	High/Low VBUS select for OC detection 0: Low VBUS condition for OC detection (default) 1: High VBUS condition for OC detection

Address	Length	Register Name	Bit	Bit Name	Default	Type	Description
0x36	1	PATH_TO_CTRL	7:4	Reserved	0000	RW	Reserved
			3	TO_EN_GP2	0	RW	GPIO2 TCPC watchdog timeout reset to default enable 0: Disable (GPIO2 will not reset to default setting when TCPC watchdog timeout occurs) (default) 1: Enable (GPIO2 will reset to default setting when TCPC watchdog timeout occurs)
			2	TO_EN_GP1	0	RW	GPIO1 TCPC watchdog timeout reset to default enable 0: Disable (GPIO1 will not reset to default setting when TCPC watchdog timeout occurs) (default) 1: Enable (GPIO1 will reset to default setting when TCPC watchdog timeout occurs)
			1	TO_EN_GPB	0	RW	GPB TCPC watchdog timeout reset to default enable 0: Disable (GPB will not reset to default setting when TCPC watchdog timeout occurs) (default) 1: Enable (GPB will reset to default setting when TCPC watchdog timeout occurs)
			0	TO_EN_GPA	0	RW	GPA TCPC watchdog timeout reset to default enable 0: Disable (GPA will not reset to default setting when TCPC watchdog timeout occurs) (default) 1: Enable (GPA will reset to default setting when TCPC watchdog timeout occurs)
0x37	1	OTP_CTRL	7:2	Reserved	000000	RW	Reserved
			1	OTP_VCON_OFF	0	RW	VCONN off when OTP occurs 0: VCONN not off when OTP occurs (default) 1: VCONN off when OTP occurs
			0	OTP_EN	0	RW	OTP enable setting 0: Disable OTP (default) 1: Enable OTP

Address	Length	Register Name	Bit	Bit Name	Default	Type	Description
0x3A	1	SBU_CTRL_01	7	SBU_VIEN	1	RW	SBU protection VI source enable setting 0: Disable 1: Enable (default)
			6	DPDM_VIEN	1	RW	DPDM protection VI source enable setting 0: Disable 1: Enable (default)
			5:4	Reserved	00	R	Reserved
			3	SBU2_SWEN	1	RW	SBU2 switch enable setting 0: Disable 1: Enable (default)
			2	SBU1_SWEN	1	RW	SBU1 switch enable setting 0: Disable 1: Enable (default)
			1	DM_SWEN	1	RW	DM switch enable setting 0: Disable 1: Enable (default)
			0	DP_SWEN	1	RW	DP switch enable setting 0: Disable 1: Enable (default)
0x3C	1	SBU_CTRL_03	7	DPDM_OV_DEG	0	RW	DPDM OVP deglitch setting 0: Deglitch disable (default) 1: Deglitch enable
			6	SBU_OV_DEG	0	RW	SBU OVP deglitch setting 0: Deglitch disable (default) 1: Deglitch enable
			5:4	SBUDPDM_REC_TIME	00	RW	DPDM OVP recovery time selection 00: 400µs (default) 01: 600µs 10: 800µs 11: 1000µs Note: ±8µs
			3	SBUDPDM_REC_TYPE	0	RW	SBU OVP recovery type selection 0: Recovery time compute after OV rising(default) 1: Recovery time compute after OV falling
			2	VCONN_OV_OFF	0	RW	Switch off when VCONN OV 0: Turn off VCONN (default) 1: Turn off SBU1/SBU2/DP/DM/VCONN
			1	DPDM_OV_OFF	0	RW	Switch off when DPDM OV 0: Turn off DP/DM (default) 1: Turn off SBU1/SBU2/DP/DM/VCONN
			0	SBU_OV_OFF	0	RW	Switch off when SBU OV 0: Turn off SBU1/SBU2 (default) 1: Turn off SBU1/SBU2/DP/DM/VCONN

Address	Length	Register Name	Bit	Bit Name	Default	Type	Description
0x3D	1	SBUDPDM_OV_ STS	7	SBU2_OV_ FLAG	0	R	SBU2 OVP status 0: No OVP occurs (default) 1: OVP occurred
			6	SBU1_OV_ FLAG	0	R	SBU1 OVP status 0: No OVP occurs (default) 1: OVP occurred
			5	DM_OV_FLAG	0	R	DM OVP status 0: No OVP occurs (default) 1: OVP occurred
			4	DP_OV_FLAG	0	R	DP OVP status 0: No OVP occurs (default) 1: OVP occurs
			3	STS_SBU2_ SWEN	0	R	SBU2 switch status 0: Switch off (default) 1: Switch on
			2	STS_SBU1_ SWEN	0	R	SBU1 switch status 0: Switch off (default) 1: Switch on
			1	STS_DM_ SWEN	0	R	DM switch status 0: Switch off (default) 1: Switch on
			0	STS_DP_ SWEN	0	R	DP switch status 0: Switch off (default) 1: Switch on
0x3F	1	SBU_ CTRL_04	7:6	SBU_OV_SEL	10	RW	SBU1/SBU2 OVP level select 00: 3.6V 01: 3.7V 10: 3.8V (default) 11: 4.5V
			5:1	Reserved	00000	R	Reserved
			0	Reserved	1	RW	Reserved
0x53	1	FOD_ CTRL_01	7:4	CTD_TIMER	0000	RW	Cable type detection delay time to check VBUS_VALID for TYPEC_ST. Range from 70ms to 100ms. 70ms to meet maximum FOD processing time and 100ms to meet minimum VBUS on time. 0000: 70ms (default) 0001: 72ms … 1110: 98ms 1111: 100ms
			3:0	FOD_TIMER	1010	RW	FOD delay time for source role. Setting requires to meet constraints: TFOD * 0.9 > TCTD*1.1 FOD delay time equals to (CTD_TIMER + FOD_TIMER*2) ms

Address	Length	Register Name	Bit	Bit Name	Default	Type	Description
0x54	1	FOD_ CTRL_02	7	FODADC_SNK _EN	0	RW	Enable FOD with ADC trigger control by CC attached as SNK when FOD_SNK_EN = 0. 0: Disable FOD with ADC HW trigger by CC attached as SNK. (default) 1: Once the cable is connected (RPCONNECT_SNK = 1), FOD with ADC operation will be triggered.
			6:4	FODADC_T2	011	RW	FOD with ADC flow to do VBUS ADC measurement after FOD_ON pullsup for T2 time. 000: 45ms 001: 50ms 010: 55ms 011: 60ms (default) … 110: 75ms 111: 80ms
			3	TM_FOD_ DISC_EN	0	RW	Manual enable FOD_DISC_EN when FOD_TM_EN = 1. 0: Disable FOD_DISC_EN when FOD_TM_EN = 1 (default) 1: Enable FOD_DISC_EN when FOD_TM_EN = 1
			2:0	FODADC_T1	101	RW	FOD with ADC flow to do VBUS ADC measurement after FOD_ON pulls up for T1 time. 000: 5ms 001: 10ms … 101: 30ms … 110: 35ms 111: 40ms
0x55	1	FOD_ CTRL_03	7:0	FODADC_ VTH0_LB	01110000	RW	FOD discharge threshold before pulling up to check if initial voltage is around VBUS_SAFE0V. The default value is 0.448V. Threshold voltage = {FOD_VTH0_HB, FOD_VTH0_LB} * 4mV.

Address	Length	Register Name	Bit	Bit Name	Default	Type	Description
0x56	1	FOD_ CTRL_04	7:6	FODADC_ ISEL	10	RW	FOD with ADC flow to select pull-up current source. 00: 5mA 01: 10mA 10: 20mA (default) 11: 20mA
			5:4	FODADC_ ABN_TH	00	RW	FOD with ADC flow to select tolerance when comparing FOD_VBUS_T2 and FOD_VBUS_T1 due to ADC measure deviation. If FOD_VBUS_T2 + FODADC_ABN_TH ≥ FOD_VBUS_T1, then FOD_VBUS_T2 voltage is considered to be greater or equal. 00: 2 (default) 01: 4 10: 6 11: 8
			3:2	Reserved	00	R	Reserved
			1:0	FODADC_ VTH0_HB	00	RW	High bit of FOD_VTH0.
0x57	1	FOD_ CTRL_05	7:0	FODADC_ VTH1_LB	01110000	RW	FOD pull-up threshold to check if VBUS pin with 1000μF is low resistance. The default value is 0.448V. Threshold voltage = {FOD_VTH1_HB, FOD_VTH1_LB} * 4mV.
0x58	1	FOD_ CTRL_06	7:2	Reserved	000000	R	Reserved
			1:0	FODADC_ VTH1_HB	00	RW	High bit of FOD_VTH1.
0x59	1	FOD_ CTRL_05	7:0	FODADC_ VTH2_LB	00011011	RW	FOD pull-up threshold to check if VBUS pin with 1000μF is low resistance. The default value is 0.108V. Threshold voltage = {FOD_VTH2_HB, FOD_VTH2_LB} * 4mV.
0x5A	1	FOD_ CTRL_06	7:2	Reserved	000000	R	Reserved
			1:0	FODADC_ VTH2_HB	00	RW	High bit of FOD_VTH1.

Address	Length	Register Name	Bit	Bit Name	Default	Type	Description
0x60	1	BC12_SNK_FUNC	7	BC12_SNK_EN	0	RW	Enable BC12 sink side function 0: Disable (default) 1: Enable
			6	SPEC_TA_EN	1	RW	Enable apple TA detection 0: Disable 1: Enable (default)
			5:4	DCDT_SEL	10	RW	DCD timeout function selection 00: Disable DCD timeout function 01: Enable 300ms DCD timeout function 10: Enable 600ms DCD timeout function (default) 11: Wait data contact
			3	VLGC_OPT	0	RW	Enable primary detection high reference voltage option 0: Disable (default) 1: Enable
			2	VPORT_SEL	1	RW	Voltage select for primary detection, secondary detection and HVDCP detection 0: 0.6V 1: Depends on DPDM_VSRC_SEL (default)
			1	BC12_WAIT_VBUS	0	RW	BC12 sink function wait and check VBUS 0: Not wait VBUS > 3.8V(default) 1: Wait and check VBUS When this bit is set to 1'b1, BC12 sink function will be enabled when VBUS > 3.8V, and BC12 sink function will be disabled when VBUS < 3.6V.
			0	Reserved	0	R	Reserved
0x61	1	BC12_STAT	7:6	Reserved	00	R	Reserved
			5	HVDCP	0	R	0: TA is not HVDCP (default) 1: TA is HVDCP
			4	DCDT	0	R	0b: DCD without time out (default) 1b: DCD time out
			3:0	PORT_STAT	0000	R	0000: No information (default) 1000: VBUS = device 1 (2.7V & 2V mode) 1001: VBUS = device 2 (1.2V & 1.2V mode) 1010: VBUS = device 3 (2V & 2.7V mode) 1011: VBUS = device 4 (2.7V & 2.7V mode) 1100: VBUS = device 5 (2V & 2V mode)/unknown TA (500mA) 1101: VBUS = SDP (500mA) 1110: VBUS = CDP (1500mA) 1111: VBUS = DCP (2400mA)

Address	Length	Register Name	Bit	Bit Name	Default	Type	Description
0x63	1	DPDM_CTR1 DPDM_SET	7	MANUAL_MODE	0	RW	Enable DPDM control by SW manual mode
			6	DPDM_DET_EN	0	RW	Enable DPDM_DET BASE
			5	DPDM_SW_VCP_EN	0	RW	Enable DPDM HVSW and charge pump, pull gate voltage to VCP
			4	DPDM_SW_EN	0	RW	When DPDM_SW_VCP_EN = 0, enable DPDM HVSW, pull gate voltage to VDDA (Reg direct out)
			3	DPDM_SHORT_EN	0	RW	DPDM short enable 0: Not short (default) 1: Short
			2	Reserved	0	R	Reserved
			1:0	DPDM_VSRC_SEL	10	RW	VDP_SRC/VDM_SRC voltage selection 00: 0.55V 01: 0.60V 10: 0.65V (default) 11: 0.70V
0x64	1	DPDM_CTR2 LDO_VSET	7	DP_LDO_EN	0	RW	While manual mode = '1', change to manual mode 0: Disable (default) 1: Enable
			6:4	DP_LDO_VSEL	000	RW	DP LDO output voltage selection 000: 0.6V (DPDM_VSRC_SEL MUST = 00b) (default) 001: 1.8V (DPDM_VSRC_SEL MUST = 01b) 010: 2.8V (DPDM_VSRC_SEL MUST = 01b) 011: 3.3V (DPDM_VSRC_SEL MUST = 01b) 100: 1.2V 101: 2.7V The other settings are reserved.
			3	DM_LDO_EN	0	RW	While manual mode = '1', change to manual mode 0: Disable (default) 1: Enable
			2:0	DM_LDO_VSEL	000	RW	DM LDO output voltage selection 000: 0.6V (DPDM_VSRC_SEL MUST = 00b) (default) 001: 1.8V (DPDM_VSRC_SEL MUST = 01b) 010: 2.8V (DPDM_VSRC_SEL MUST = 01b) 011: 3.3V (DPDM_VSRC_SEL MUST = 01b) 100: 1.2V 101: 2.7V The other settings are reserved.

Address	Length	Register Name	Bit	Bit Name	Default	Type	Description
0x65	1	DPDM_CTR3 DISCHG_SET	7	DP_DISCHG_EN	0	RW	While manual mode = '1', change to manual mode 0: Disable (default) 1: Enable
			6:4	DP_DISCHG_RSEL	000	RW	DP discharge resistor selection 000: 6.0kΩ (default) 001: 20kΩ 010: 0.7μA 011: 100μA 1xx: 900kΩ
			3	DM_DISCHG_EN	0	RW	While manual mode = '1', change to manual mode 0: Disable (default) 1: Enable
			2:0	DM_DISCHG_RSEL	000	RW	DM discharge resistor selection 000: 6.0kΩ (default) 001: 20kΩ 010: 0.7μA 011: 100μA 1xx: 900kΩ
0x66	1	DPDM_CTR4 DP_PULL_SET	7	DP_PULL_REN	0	RW	While manual mode = '1', change to manual mode 0: Disable (default) 1: Enable
			6:4	DP_PULL_RSEL	011	RW	DP pull-up resistor selection 000: 1.2kΩ 001: 10kΩ 010: 15kΩ 011: Bypass (~120Ω) (default) 100: 30kΩ 101: 102kΩ The other settings are reserved.
			3	Reserved	0	R	Reserved
			2	DP_PULL_IEN	0	RW	While manual mode = '1', change to manual mode 0: Disable (default) 1: Enable
			1:0	DP_PULL_ISEL	01	RW	DP pull-up current selection 01: 10μA (default) Others: Reserved

Address	Length	Register Name	Bit	Bit Name	Default	Type	Description
0x67	1	DPDM_CTR5 DM_PULL_SET	7	DM_PULL_REN	0	RW	While manual mode = '1', change to manual mode 0: Disable (default) 1: Enable
			6:4	DM_PULL_RSEL	011	RW	DM pull-up resistor selection 000: 1.2kΩ 001: 10kΩ 010: 15kΩ 011: Bypass (~120Ω) (default) 100: 30kΩ 101: 102kΩ The other settings are reserved.
			3	Reserved	0	R	Reserved
			2	DM_PULL_IEN	0	RW	While manual mode = '1', change to manual mode 0: Disable (default) 1: Enable
			1:0	DM_PULL_ISEL	01	RW	DM pull-up current selection 01: 10μA (default) Others: Reserved
0x68	1	DPDM_CTR6 DPDM_VREF_HIDET	7:5	Reserved	000	R	Reserved
			4:0	VREF_HIDET	00000	RW	DPDM voltage detection setting (HI/LO) Threshold: 0.1V to 2.6V (LSB = 0.1V) 00000: 0.1V (default) … 11001: 2.6V ---------- 11010: 0.275V (BC1.2 VDAT_REF_MIN) 11011: 0.375V (BC1.2 VDAT_REF_MAX) 11100: 0.9V (BC1.2 VLGC_MIN) 11101: 1.975V (BC1.2 VLGC_MAX) 11110: 1.5V (A_DET_LO) 11111: 2.3V (A_DET_HI)
0x69	1	DPDM_CTR7 DPDM_VREF_LODET	7:5	Reserved	000	R	Reserved
			4:0	VREF_LODET	00000	RW	DPDM voltage detection setting (HI/LO) Threshold: 0.1V to 2.6V (LSB = 0.1V) 00000: 0.1V (default) … 11001: 2.6V ---------- 11010: 0.275V (BC1.2 VDAT_REF_MIN) 11011: 0.375V (BC1.2 VDAT_REF_MAX) 11100: 0.9V (BC1.2 VLGC_MIN) 11101: 1.975V (BC1.2 VLGC_MAX) 11110: 1.5V (A_DET_LO) 11111: 2.3V (A_DET_HI)

Address	Length	Register Name	Bit	Bit Name	Default	Type	Description
0x6D	1	BC12_SRC_FUNC	7	BC12_SRC_EN	0	RW	BC12 TA function enable 0: Disable (default) 1: Enable
			6:4	SRC_MODE_SEL	000	RW	Mode selection 000: BC12 SDP (default) 001: BC12 CDP 010: BC12 DCP 011 to 111: Reserved
			3	Reserved	0	R	Reserved
			2:1	Reserved	00	RW	Reserved
			0	WAIT_VBUS_ON	1	RW	Wait VBUS > 4.0V (VBUS_PRESENT_FLAG = 1) to enable BC12 TA function 0: Not wait VBUS > 4.0V. BC12 TA function will enable when BC12_SRC_EN = 1b 1: Wait VBUS > 4.0V. BC12 TA function will enable when BC12_SRC_EN = 1b and VBUS_PRESENT_FLAG = 1 (default)
0x6E	1	SRC_STS_01	7:2	Reserved	000000	R	Reserved
			1	STS_CDP_ERR	0	R	CDP flow error 0: No CDP flow error (default) 1: CDP flow error Note: This bit is updated after INT_BC12_TA_CHG has been set to 1b. It will keep until next time INT_BC12_TA_CHG has been set to 1b. Check this bit only after INT_BC12_TA_CHG has been set to 1b.
			0	STS_CDP_DONE	0	R	CDP flow done 0: No CDP flow (default) 1: CDP flow done Note: This bit is updated after INT_BC12_TA_CHG has been set to 1b. It will keep until next time INT_BC12_TA_CHG has been set to 1b. Check this bit only after INT_BC12_TA_CHG has been set to 1b.

Address	Length	Register Name	Bit	Bit Name	Default	Type	Description
0x70	1	SRC_ CTRL_01	7:6	DPDM_ GLITCH	00	RW	DP/DM deglitch 00: 100μs (default) 01: 132μs 10: 168μs 11: 200μs
			5:4	USBDET_ TIMEOUT_SEL	10	RW	USB device detect timeout 00: 1.024s 01: 2.048s 10: 4.096s (default) 11: 8.192s
			3:2	PRIMARY_ TIMEOUT_SEL	00	RW	Primary detection timeout 00: 1.0s (default) 01: 1.3s 10: 1.6s 11: 2.0s
			1:0	CDP_VSRC_ ON_SEL	10	RW	Vsrc_on time detect 00: 16ms 01: 24ms 10: 32ms (default) 11: 40ms
0x71	1	SRC_ CTRL_02	7	Reserved	0	R	Reserved
			6:5	Reserved	0	RW	Reserved
			4:0	DPDM_VOL_ H2	10011	RW	DPDM voltage detection setting (HI/LO) Threshold: 0.1V to 2.6V (LSB = 0.1V) 00000: 0.1V … 10011: 2.0V (default) … 11001: 2.6V ---------- 11010: 0.275V (BC1.2 VDAT_REF_MIN) 11011: 0.375V (BC1.2 VDAT_REF_MAX) 11100: 0.9V (BC1.2 VLGC_MIN) 11101: 1.975V (BC1.2 VLGC_MAX) 11110: 1.5V (A_DET_LO) 11111: 2.3V (A_DET_HI) Note: In CDP mode, this register is used to check USB attach level. In private protocol mode/auto TA mode, this register is used to check DPDM high level after the device is attached.

Address	Length	Register Name	Bit	Bit Name	Default	Type	Description
0x72	1	SRC_ CTRL_03	7:6	Reserved	01	RW	Reserved
			5	Reserved	0	R	Reserved
			4:0	DPDM_VOL_H	01001	RW	DPDM voltage detection setting (HI/LO) Threshold: 0.1V to 2.6V (LSB = 0.1V) 00000: 0.1V … 01001: 1.0V(default) … 11001: 2.6V ---------- 11010: 0.275V (BC1.2 VDAT_REF_MIN) 11011: 0.375V (BC1.2 VDAT_REF_MAX) 11100: 0.9V (BC1.2 VLGC_MIN) 11101: 1.975V (BC1.2 VLGC_MAX) 11110: 1.5V (A_DET_LO) 11111: 2.3V (A_DET_HI) Note: This register is used for CDP/ private protocol to check Vdp_src high level.
0x73	1	SRC_ CTRL_04	7:6	Reserved	01	RW	Reserved
			5	Reserved	0	R	Reserved
			4:0	DPDM_VOL_L	11010	RW	DPDM voltage detection setting (HI/LO) Threshold: 0.1V to 2.6V (LSB = 0.1V) 00000: 0.1V … 11001: 2.6V ---------- 11010: 0.275V (BC1.2 VDAT_REF_MIN) (default) 11011: 0.375V (BC1.2 VDAT_REF_MAX) 11100: 0.9V (BC1.2 VLGC_MIN) 11101: 1.975V (BC1.2 VLGC_MAX) 11110: 1.5V (A_DET_LO) 11111: 2.3V (A_DET_HI) Note: This register is used for CDP/ private protocol to check Vdp_src high level.

Address	Length	Register Name	Bit	Bit Name	Default	Type	Description
0xA0	1	ADC_ CTRL_01	7	ADC_CH07_ EN	0	RW	ADC CH07: SBU2, 4mV/LSB 0: Disable ADC CH07 (default) 1: Enable ADC CH07
			6	ADC_CH06_ EN	0	RW	ADC CH06: SBU1, 4mV/LSB 0: Disable ADC CH06 (default) 1: Enable ADC CH06
			5	ADC_CH05_ EN	0	RW	ADC CH05: CC2, 4mV/LSB 0: Disable ADC CH05 (default) 1: Enable ADC CH05
			4	ADC_CH04_ EN	0	RW	ADC CH04: CC1, 4mV/LSB 0: Disable ADC CH04 (default) 1: Enable ADC CH04
			3	ADC_CH03_ EN	0	RW	ADC CH03: VBUS current, 33mA/LSB 0: Disable ADC CH03 (default) 1: Enable ADC CH03
			2	ADC_CH02_ EN	0	RW	ADC CH02: VDC, 4mV/LSB 0: Disable ADC CH02 (default) 1: Enable ADC CH02
			1	ADC_CH01_ EN	0	RW	ADC CH01: VBUS2, 4mV/LSB 0: Disable ADC CH01 (default) 1: Enable ADC CH01
			0	ADC_CH00_ EN	0	RW	ADC CH00: VBUS1, 12.5mV/LSB 0: Disable ADC CH00 (default) 1: Enable ADC CH00
0xA1	1	ADC_ CTRL_02	7:2	Reserved	000000	R	Reserved
			1	ADC_CH09_ EN	0	RW	ADC CH09: DM, 4mV/LSB 0: Disable ADC CH09 (default) 1: Enable ADC CH09
			0	ADC_CH08_ EN	0	RW	ADC CH08: DP, 4mV/LSB 0: Disable ADC CH08C(default) 1: Enable ADC CH08
0xA2	1	ADC_ CTRL_03	7:4	PRIORITY_CH _SEL	1111	RW	Select priority channel 0000: CH00 0001: CH01 …… 1011: CH11 Other: No priority 1111: No priority (default)
			3:0	ADC_INT_SEL	0000	RW	Select INT_ADC report channel 0000: CH00 (default) 0001: CH01 …… 1011: CH11 1100: Reserved 1101: Reserved 1110: Reserved 1111: Report all channels

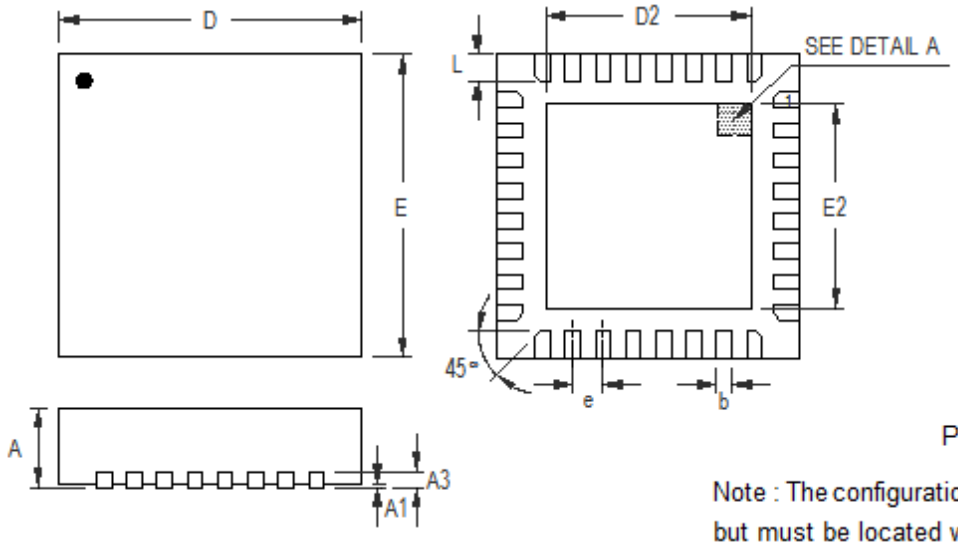
Address	Length	Register Name	Bit	Bit Name	Default	Type	Description
0xA3	1	ADC_ CTRL_04	7:6	EN_TIME	01	RW	ADC enable wait time 00: 7.33μs 01: 40μs (default) 10: 80μs 11: 160μs
			5	reserved	0	R	Reserved
			4	ADC_CLAMP_ EN	1	RW	ADC clamp enable 0: Disable clamp (get original ADC output) 1: Enable clamp (get clamp ADC output) (default)
			3:2	WAIT_TIME	01	RW	ADC channel switch wait time 00: 7.92μs 01: 10.66μs(default) 10: 13.33μs 11: 16μs
			1:0	AVG_SEL	11	RW	ADC average count selection 00: 1 01: 2 10: 4 11: 8 (default)
0xA4	1	ADC_ CTRL_05	7:3	Reserved	00000	R	Reserved
			2	OFF_VRPBUF	0	RW	Select the reference input 0: aVRP_bfr (default) 1: aVRP
			1:0	SEL_WIDTH	00	RW	Sample period duration 00: Sample time is 2T. (default) 01: Sample time is 4T. 10: Sample time is 6T. 11: Sample time is 8T. Where T is a period of clock.

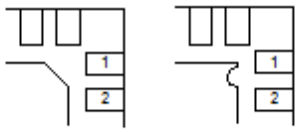
Address	Length	Register Name	Bit	Bit Name	Default	Type	Description
0xA5	1	ADC_CTRL_06	7	Reserved	0	R	Reserved
			6:4	SX_CMP	011	RW	Tuning comparator current 000: 120μA 001: 160μA 010: 200μA 011: 240μA (default) 100: 280μA 101: 320μA 110: 360μA 111: 400μA
			3:2	SX_BUF	01	RW	Tuning input unity-gain buffer bias current 00: 2.5μA 01: 5μA (default) 10: 7.5μA 11: 10μA
			1:0	SX_VREF	00	RW	Tuning aVRP_bfr buffer bias current 00: 2.5μA (default) 01: 5μA 10: 7.5μA 11: 10μA
0xA6	1	ADC_CH00_VOL_L	7:0	ADC_CH00_VOL_L	00000000	R	ADC CH00 (VBUS1) report low byte, 12.5mV/LSB
0xA7	1	ADC_CH00_VOL_H	7:4	Reserved	0000	R	Reserved
			3:0	ADC_CH00_VOL_H	0000	R	ADC CH00 (VBUS1) report high byte, 12.5mV/LSB
0xA8	1	ADC_CH01_VOL_L	7:0	ADC_CH01_VOL_L	00000000	R	ADC CH01 (VBUS2) report low byte, 4mV/LSB
0xA9	1	ADC_CH01_VOL_H	7:4	Reserved	0000	R	Reserved
			3:0	ADC_CH01_VOL_H	0000	R	ADC CH01 (VBUS2) report high byte, 4mV/LSB
0xAA	1	ADC_CH02_VOL_L	7:0	ADC_CH02_VOL_L	00000000	R	ADC CH02 (VDC) report low byte, 4mV/LSB
0xAB	1	ADC_CH02_VOL_H	7:4	Reserved	0000	R	Reserved
			3:0	ADC_CH02_VOL_H	0000	R	ADC CH02 (VDC) report high byte, 4mV/LSB
0xAC	1	ADC_CH03_VOL_L	7:0	ADC_CH03_VOL_L	00000000	R	ADC CH03 (VBUS current) report low byte, 33mA/LSB
0xAD	1	ADC_CH03_VOL_H	7:4	Reserved	0000	R	Reserved
			3:0	ADC_CH03_VOL_H	0000	R	ADC CH03 (VBUS current) report low byte, 33mA/LSB
0xAE	1	ADC_CH04_VOL_L	7:0	ADC_CH04_VOL_L	00000000	R	ADC CH04 (CC1) report low byte, 4mV/LSB

Address	Length	Register Name	Bit	Bit Name	Default	Type	Description
0xAF	1	ADC_CH04_VOL_H	7:4	Reserved	0000	R	Reserved
			3:0	ADC_CH04_VOL_H	0000	R	ADC CH04 (CC1) report high byte, 4mV/LSB
0xB0	1	ADC_CH05_VOL_L	7:0	ADC_CH05_VOL_L	00000000	R	ADC CH05 (CC2) report low byte, 4mV/LSB
0xB1	1	ADC_CH05_VOL_H	7:4	Reserved	0000	R	Reserved
			3:0	ADC_CH05_VOL_H	0000	R	ADC CH05 (CC2) report high byte, 4mV/LSB
0xB2	1	ADC_CH06_VOL_L	7:0	ADC_CH06_VOL_L	00000000	R	ADC CH06 (SBU1) report low byte, 4mV/LSB
0xB3	1	ADC_CH06_VOL_H	7:4	Reserved	0000	R	Reserved
			3:0	ADC_CH06_VOL_H	0000	R	ADC CH06 (SBU1) report high byte, 4mV/LSB
0xB4	1	ADC_CH07_VOL_L	7:0	ADC_CH07_VOL_L	00000000	R	ADC CH07 (SBU2) report low byte, 4mV/LSB
0xB5	1	ADC_CH07_VOL_H	7:4	Reserved	0000	R	Reserved
			3:0	ADC_CH07_VOL_H	0000	R	ADC CH07 (SBU2) report high byte, 4mV/LSB
0xB6	1	ADC_CH08_VOL_L	7:0	ADC_CH08_VOL_L	00000000	R	ADC CH08 (DP) report low byte, 4mV/LSB
0xB7	1	ADC_CH08_VOL_H	7:4	Reserved	0000	R	Reserved
			3:0	ADC_CH08_VOL_H	0000	R	ADC CH08 (DP) report high byte, 4mV/LSB
0xB8	1	ADC_CH09_VOL_L	7:0	ADC_CH09_VOL_L	00000000	R	ADC CH09 (DM) report low byte, 4mV/LSB
0xB9	1	ADC_CH09_VOL_H	7:4	Reserved	0000	R	Reserved
			3:0	ADC_CH09_VOL_H	0000	R	ADC CH09 (DM) report high byte, 4mV/LSB

Address	Length	Register Name	Bit	Bit Name	Default	Type	Description
0xC0	1	IO_CTRL	7	I2C_MODE	1	RW	I^2C max speed 0: Up to 400kHz 1: Up to 3.4MHz (default)
			6	Reserved	0	R	Reserved
			5:4	GPIO3_DRV	00	RW	GPIO3 output driving capability ability 00: 20mV/s (default) 01: 40mV/s 10: 60mV/s 11: 80mV/s
			3:2	GPIO2_DRV	00	RW	GPIO2 output driving capability ability 00: 20mV/s (default) 01: 40mV/s 10: 60mV/s 11: 80mV/s
			1:0	GPIO1_DRV	00	RW	GPIO1 output driving capability ability 00: 20mV/s (default) 01: 40mV/s 10: 60mV/s 11: 80mV/s
0xC1	1	SRCDET_CTRL	7:6	Reserved	00	R	Reserved
			5:4	SRCDET_SETTING	00	R	SRCDET Setting 00: No SRCDET function (default) 01: Check CC for 1.5A 10: Check CC for 3.0A 11: Reserved
			3:2	Reserved	00	R	Reserved
			1	GPIO3_SOFT_RSTN_EN	1	RW	Reset REG 0xEF[3:1] (GPIO3_OD_N, GPIO3_OE, GPIO3_O) and RT2_REG 0xC0[5:4] (GPIO3_DRV) when soft reset is triggered. 0: Disable 1: Enable (default)
			0	SRCDET_CTRL_EN	1	RW	Turn on VBUS (GPIO3) when special RP level is attached, depending on the SRCDET pin 0: Disable 1: Enable (default)

15 Outline Dimension





DETAIL A

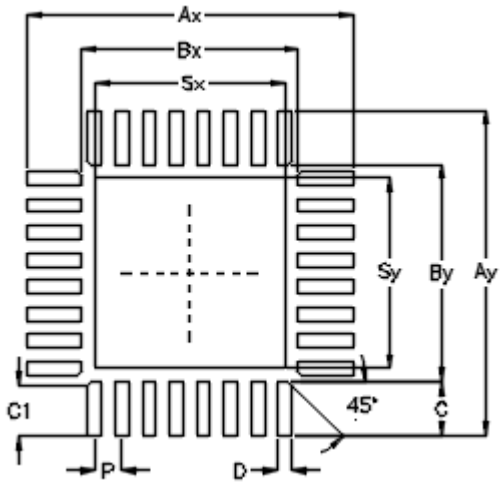
Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.150	0.250	0.006	0.010
D	3.900	4.100	0.154	0.161
D2	2.650	2.750	0.104	0.108
E	3.900	4.100	0.154	0.161
E2	2.650	2.750	0.104	0.108
e	0.400		0.016	
L	0.300	0.400	0.012	0.016

W-Type 32L QFN 4x4 Package

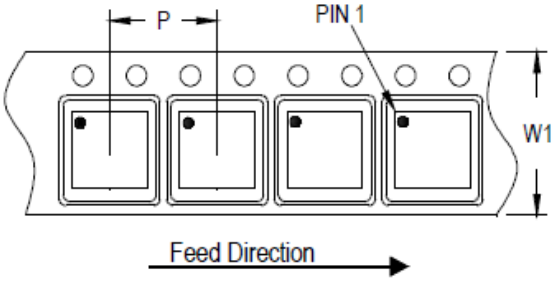
16 Footprint Information

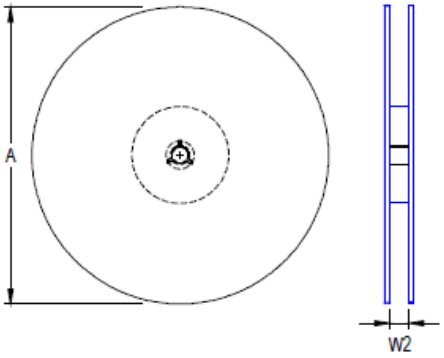


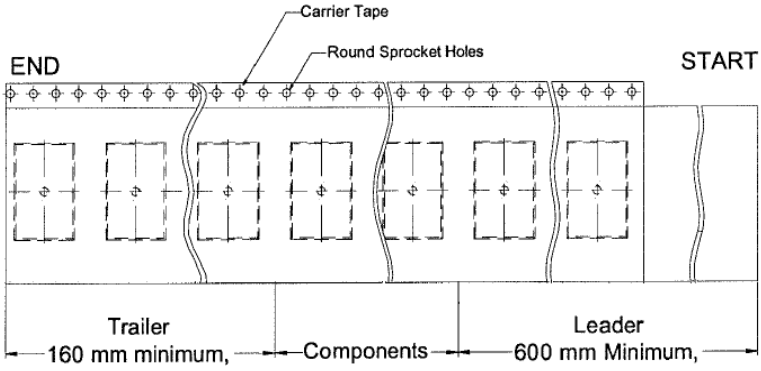
Package	Number of Pin	Footprint Dimension (mm)										Tolerance
		P	Ax	Ay	Bx	By	C*32	C1*8	D	Sx	Sy	
V/W/U/XQFN4*4-32	32	0.40	4.80	4.80	3.20	3.20	0.80	0.75	0.20	2.80	2.80	±0.05

17 Packing Information

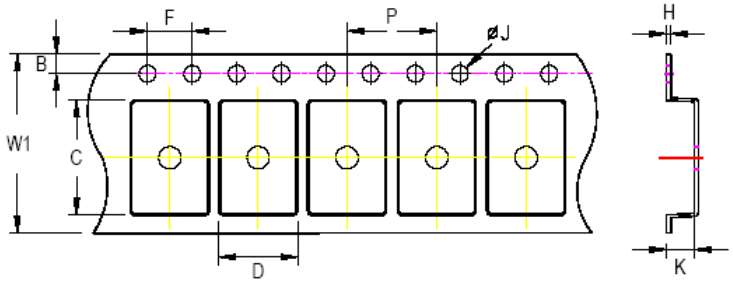
17.1 Tape and Reel Data







Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min/Max (mm)
			(mm)	(in)				
(V, W) QFN/DFN 4x4	12	8	180	7	1,500	160	600	12.4/14.4



C, D, and K are determined by component size. The clearance between the components and the cavity is as follows:

- For 12mm carrier tape: 0.5mm max.

Tape Size	W1	P		B		F		ØJ		K		H
	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Max
12mm	12.3mm	7.9mm	8.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	1.0mm	1.3mm	0.6mm

17.2 Tape and Reel Packing

Step	Photo/Description	Step	Photo/Description
1	 Reel 7”	4	 3 reels per inner box **Box A**
2	 HIC & Desiccant (1 Unit) inside	5	 12 inner boxes per outer box
3	 Caution label is on backside of Al bag	6	 Outer box **Carton A**

Container / Package	Reel		Box			Carton		
	Size	Units	Item	Reels	Units	Item	Boxes	Unit
(V, W) QFN/DFN 4x4	7”	1,500	Box A	3	4,500	Carton A	12	54,000
			Box E	1	1,500	For Combined or Partial Reel.		

17.3 Packing Material Anti-ESD Property

Surface Resistance	Aluminum Bag	Reel	Cover tape	Carrier tape	Tube	Protection Band
Ω/cm^2	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**

Richtek Technology Corporation
14F, No. 8, Tai Yuen 1st Street, Chupei City
Hsinchu, Taiwan, R.O.C.
Tel: (8863)5526789

18 Datasheet Revision History

Version	Date	Description	Item
01	2025/3/6	Modify	*General Description on page 1* - Added the description of temperature Features on page 1 - Updated TCPC Interface support *Ordering Information on page 1* - Added note *Typical Application Circuit on page 18, 19, 20* - Modified R1 value and added R15 *Application Information on page 21, 54* *- Updated Section 13.1* - Added thermal considerations and declaration *Packing Information on page 132, 133, 134* - Added packing information