Richtek 42V/60V Industrial and Automotive Buck Converters

Abstract

The RTQ2960/61/62/63/65 and RTQ6360/61/62/63/65 are flexible buck converter families for wide input and output voltage range applications. They can be used with input voltages from 4.5V up to 60V and the output can be adjusted from 0.8V up to VIN. The RTQ2960/61/62/63/65 and RTQ2940/41/42/43/49/49A/45/45A are Automotive Grade 1 buck converters that are suitable to be used in 12V car battery systems (42V rating) and 24V car battery systems (60V rating) and include the spread-spectrum feature. The RTQ6360/61/62/63/65 and RTQ6340/41/42/43/45 are Industrial Grade buck converters that are suitable to be used in applications requiring steady fixed frequency operation and industrial temperature range.

The buck converter ranges include parts that can deliver currents from 0.5A up to 5A output currents. This application note explains the design criteria and describes two wide input voltage step-down designs: A low power 3.3V/0.5A output using RTQ6360GQW and a high power 24V/3A output using RTQ6363GQW. External components are calculated using the RTQ29xx and RTQ63xx Excel based design tools, and results are verified with actual measurement results.

CONTENTS

1. INTRODUCTION

The RTQ2960/61/62/63/65, RTQ6360/61/62/63/65, RTQ2940/41/42/43/49/49A/45/45A and RTQ6340/41/42/43/45 are flexible asynchronous buck converter families for wide input and output voltage range applications. The parts can be used with input voltages from 4.5V up to 42V for RTQ2940/41/42/43/49/49A/45/45A and RTQ6340/41/42/43/45 and 4.5V to 60V for the RTQ2960/61/62/63/65 and RTQ6360/61/62/63/65 parts, and the output can be adjusted from 0.8V up to VIN , delivering up to 5A output currents, and use peak current mode topology with external compensation for optimal flexibility.
The RTQ2960/61/62/63/65 and RTQ2940/41/42/43/49/49A/45/45A are Automotive Grade 1 buck converters that include the spread-spectrum feature. The RTQ6360/61/62/63/65 and RTQ6340/41/42/43/45 are Industrial Grade buck converters without spread spectrum feature. All the IC families support enhanced light load efficiency and low dropout mode operation approaching 100% duty-cycle.

Part number	Vin range	Current rating	Programmable Frequency range	R_{DSON}	T_{ON_MIN}	External compensation	External soft-start	Power good	Spread Spectrum / AEC-Q100	Package
RTQ6360GSP	4.5 ~ 60V	0.5A	0.1 ~ 2.5MHz	170mΩ	100ns	Yes	No	No	No	PSOP-8
RTQ6360GQW	4.5 ~ 60V	0.5A	0.1 ~ 2.5MHz	170mΩ	100ns	Yes	Yes	Yes	No	DFN10L 3x3
RTQ6361GSP	4.5 ~ 60V	1.5A	0.1 ~ 2.5MHz	160mΩ	100ns	Yes	No	No	No	PSOP-8
RTQ6361GQW	4.5 ~ 60V	1.5A	0.1 ~ 2.5MHz	160mΩ	100ns	Yes	Yes	Yes	No	DFN10L 3x3
RTQ6362GSP	4.5 ~ 60V	2.5A	0.1 ~ 2.5MHz	150mΩ	100ns	Yes	No	No	No	PSOP-8
RTQ6362GQW	4.5 ~ 60V	2.5A	0.1 ~ 2.5MHz	150mΩ	100ns	Yes	Yes	Yes	No	DFN10L 3x3
RTQ6363GSP	4.5 ~ 60V	3.5A	0.1 ~ 2.5MHz	80mΩ	120ns	Yes	No	No	No	PSOP-8
RTQ6363GQW	4.5 ~ 60V	3.5A	0.1 ~ 2.5MHz	80mΩ	120ns	Yes	Yes	Yes	No	DFN10L 4x4
RTQ6365GSP	4.5 ~ 60V	5A	0.1 ~ 2.5MHz	70mΩ	120ns	Yes	No	No	No	PSOP-8
RTQ6365GQW	4.5 ~ 60V	5A	0.1 ~ 2.5MHz	70mΩ	120ns	Yes	Yes	Yes	No	DFN10L 4x4
RTQ2960GSP	4.5 ~ 60V	0.5A	0.1 ~ 2.5MHz	170mΩ	100ns	Yes	No	No	Yes	PSOP-8
RTQ2960GQW	4.5 ~ 60V	0.5A	0.1 ~ 2.5MHz	170mΩ	100ns	Yes	Yes	Yes	Yes	DFN10L 3x3
RTQ2961GSP	4.5 ~ 60V	1.5A	0.1 ~ 2.5MHz	160mΩ	100ns	Yes	No	No	Yes	PSOP-8
RTQ2961GQW	4.5 ~ 60V	1.5A	0.1 ~ 2.5MHz	160mΩ	100ns	Yes	Yes	Yes	Yes	DFN10L 3x3
RTQ2962GSP	4.5 ~ 60V	2.5A	0.1 ~ 2.5MHz	150mΩ	100ns	Yes	No	No	Yes	PSOP-8
RTQ2962GQW	4.5 ~ 60V	2.5A	0.1 ~ 2.5MHz	150mΩ	100ns	Yes	Yes	Yes	Yes	DFN10L 3x3
RTQ2963GSP	4.5 ~ 60V	3.5A	0.1 ~ 2.5MHz	80mΩ	120ns	Yes	No	No	Yes	PSOP-8
RTQ2963GQW	4.5 ~ 60V	3.5A	0.1 ~ 2.5MHz	80mΩ	120ns	Yes	Yes	Yes	Yes	DFN10L 4x4
RTQ2965GSP	4.5 ~ 60V	5A	0.1 ~ 2.5MHz	70mΩ	120ns	Yes	No	No	Yes	PSOP-8
RTQ2965GQW	4.5 ~ 60V	5A	0.1 ~ 2.5MHz	70mΩ	120ns	Yes	Yes	Yes	Yes	DFN10L 4x4
RTQ6340GSP	4.5 ~ 42V	0.5A	0.1 ~ 2.5MHz	170mΩ	100ns	Yes	No	No	No	PSOP-8
RTQ6340GQW	4.5 ~ 42V	0.5A	0.1 ~ 2.5MHz	170mΩ	100ns	Yes	Yes	Yes	No	DFN10L 3x3
RTQ6341GSP	4.5 ~ 42V	1.5A	0.1 ~ 2.5MHz	160mΩ	100ns	Yes	No	No	No	PSOP-8
RTQ6341GQW	4.5 ~ 42V	1.5A	0.1 ~ 2.5MHz	160mΩ	100ns	Yes	Yes	Yes	No	DFN10L 3x3
RTQ6342GSP	4.5 ~ 42V	2.5A	0.1 ~ 2.5MHz	150mΩ	100ns	Yes	No	No	No	PSOP-8
RTQ6342GQW	4.5 ~ 42V	2.5A	0.1 ~ 2.5MHz	150mΩ	100ns	Yes	Yes	Yes	No	DFN10L 3x3
RTQ6343GSP	4.5 ~ 42V	3.5A	0.1 ~ 2.5MHz	80mΩ	120ns	Yes	No	No	No	PSOP-8
RTQ6343GQW	4.5 ~ 42V	3.5A	0.1 ~ 2.5MHz	80mΩ	120ns	Yes	Yes	Yes	No	DFN10L 4x4
RTQ6345GSP	4.5 ~ 42V	5A	0.1 ~ 2.5MHz	70mΩ	120ns	Yes	No	No	No	PSOP-8
RTQ6345GQW	4.5 ~ 42V	5A	0.1 ~ 2.5MHz	70mΩ	120ns	Yes	Yes	Yes	No	DFN10L 4x4
RTQ2940GSP	4.5 ~ 42V	0.5A	0.1 ~ 2.5MHz	170mΩ	100ns	Yes	No	No	Yes	PSOP-8
RTQ2940GQW	4.5 ~ 42V	0.5A	0.1 ~ 2.5MHz	170mΩ	100ns	Yes	Yes	Yes	Yes	DFN10L 3x3
RTQ2941GSP	4.5 ~ 42V	1.5A	0.1 ~ 2.5MHz	160mΩ	100ns	Yes	No	No	Yes	PSOP-8
RTQ2941GQW	4.5 ~ 42V	1.5A	0.1 ~ 2.5MHz	160mΩ	100ns	Yes	Yes	Yes	Yes	DFN10L 3x3
RTQ2942GSP	4.5 ~ 42V	2.5A	0.1 ~ 2.5MHz	150mΩ	100ns	Yes	No	No	Yes	PSOP-8
RTQ2942GQW	4.5 ~ 42V	2.5A	0.1 ~ 2.5MHz	150mΩ	100ns	Yes	Yes	Yes	Yes	DFN10L 3x3
RTQ2949GSP	4.5 ~ 42V	3A	0.1 ~ 2.5MHz	150mΩ	100ns	Yes	No	No	Yes	PSOP-8
RTQ2949AGSP	4.5 ~ 42V	3A	0.1 ~ 2.5MHz	150mΩ	65ns	Yes	No	No	Yes	PSOP-8
RTQ2963GSP	4.5 ~ 42V	3.5A	0.1 ~ 2.5MHz	80mΩ	120ns	Yes	No	No	Yes	PSOP-8
RTQ2943GQW	4.5 ~ 42V	3.5A	0.1 ~ 2.5MHz	80mΩ	120ns	Yes	Yes	Yes	Yes	DFN10L 4x4
RTQ2945GSP	4.5 ~ 42V	5A	0.1 ~ 2.5MHz	70mΩ	120ns	Yes	No	No	Yes	PSOP-8
RTQ2945GQW	4.5 ~ 42V	5A	0.1 ~ 2.5MHz	70mΩ	120ns	Yes	Yes	Yes	Yes	DFN10L 4x4
RTQ2945AGSP	4.5 ~ 42V	5A	0.1 ~ 2.5MHz	70mΩ	65ns	Yes	No	No	Yes	PSOP-8

TABLE 1

Chapter 2 provides an overview of the application component selection and design considerations. Chapters 3 and 4 each describe a design with specific V_{IN}/V_{OUT} condition from low 3.3V MCU supply to industrial supply providing 24V output.

2. RTQ29XX AND RTQ63XX GENERAL DESIGN GUIDELINES

The general application schematic is shown in figure 1. The Current Mode loop compensation is set via the external compensation network. The switching frequency can be programmed by the Rt resistor and the soft start time can be adjusted via the external soft-start capacitor. Due to the asynchronous topology, an external Schottky freewheel diode is needed. The output can be set via a simple resistor divider. By connecting a resistor divider from Vin to Enable, the converter Vin start and stop voltages can be precisely adjusted. The DFN package versions have Soft-start and a Power Good function which can be used for MCU reset or power sequencing.

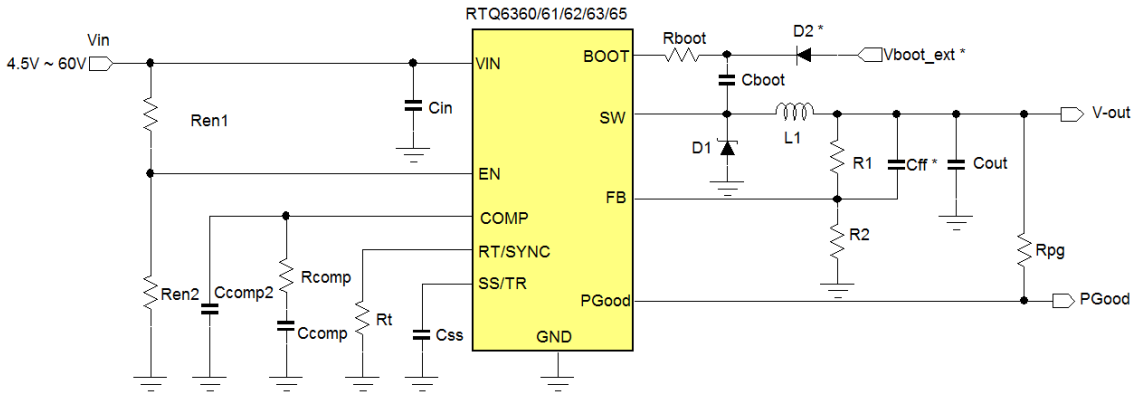


FIGURE 1 (PARTS WITH * ARE OPTIONAL, PGOOD AND SOFTSTART ARE ONLY AVAILABLE ON DFN PACKAGES)

The following guidelines can be used to calculate the various application components. For convenience, Richtek has developed an Excel calculation sheet which makes the design and component choice easy and quick. The RTQ29xx and RTQ63xx excel tools can be downloaded here and here.

- Switching frequency considerations:
  Since this family can work over a wide input voltage range, the converter switching frequency is an important parameter: For applications with input voltages higher than 24V, a moderate switching frequency (< 1MHz) is recommended to reduce switching losses. The RTQ29xx/RTQ63xx IC control circuit will start to reduce its frequency when the high-side switch minimum on-time or minimum off-time are reached, but in doing so, the converter output ripple will increase. If the application needs to work over a wide input voltage range with low output ripple, the switching frequency may need to be reduced to maintain the operation within the maximum and minimum duty-cycle limitations.
  The frequency can be set via the external R_T resistor: For RTQ6360/61/62: $R_T = \frac{140398}{F_{SW}^{1.03}}$; For RTQ6363/65: $R_T = \frac{120279}{F_{SW}^{1.033}}$

- Input and output voltage considerations:
  The RTQ29xx/RTQ63xx output voltage can be adjusted from 0.8V to V_{IN} by means of R1 and R2:
  $V_{OUT} = V_{REF}\left(1 + \frac{R1}{R2}\right)$ where V_{REF} = 0.8V
  The impedance of the feedback network is not critical, but it is recommended to avoid too high resistor values to reduce sensitivity to noise. It is recommended to keep the value of R2 below 80kΩ.
  RTQ29xx/RTQ63xx series has a typical minimum on-time of 100nsec, achieving minimum duty-cycle in CCM mode of 100nsec*F_{SW}.
  RTQ29xx/RTQ63xx series have typical minimum off-time of 130nsec, achieving maximum duty-cycle in CCM mode of 1-130nsec*F_{SW}. So a 1MHz switching frequency would give a minimum duty-cycle of 10% and a maximum duty-cycle of 87%. It is possible to run the converter outside its minimum and maximum duty-cycle range, at the expense of increased output ripple.
  When operating RTQ29xx/RTQ63xx series in high duty-cycles exceeding 65% or input voltage below 5.5V the external bootstrap supply via D2 should be added. The external bootstrap supply is recommended to be 5V, using a normal diode for D1. When lower bootstrap supply is used, D2 should preferably be a small Schottky diode)

- For Inductor value of L1 there are two main criteria that need to be considered: Inductor current ripple and slope compensation. For applications with duty-cycle lower than 50%, the inductor can be calculated to provide a ripple current

of 20 ~ 30% of the IC rated current: (so for 5A converter RTQ6365, ΔI_L would be around 0.3*5A = 1.5A even if the maximum application current is lower) $L = \frac{V_{OUT}}{F_{SW} \cdot \Delta I_L} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$.

In applications where the duty-cycle can exceed 50%, the inductor current falling slope dI/dt also needs to fit the converter internal slope compensation: L1 value needs to fulfill the following criteria: $L1 > \frac{V_{OUT}}{X_C \cdot F_{SW}}$ where slope compensation constant X_C is: 0.5 for RTQ6360, 1.3 for RTQ6361, 2.1 for RTQ6362, 2.9 for RTQ6363, 4 for RTQ6365. For high input voltage supplies, wire wound shielded ferrite inductors are recommended.

- For output capacitor selection, there are several considerations:
  a. Output ripple in CCM mode

     Output ripple in CCM mode can be calculated from $V_{RIPPLE\_CCM} = \Delta I_{L\_CCM} \left(ESR + \frac{1}{8 \cdot C_{OUT} \cdot F_{SW}}\right)$

     The CCM mode inductor ripple can be calculated from: $\Delta I_{L\_CCM} = \frac{V_{OUT}}{F_{SW} \cdot L} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$

     When using ceramic output capacitors in these low voltage supplies, output ripple voltage in CCM mode will be small. It should be noted that the output ripple in PSM mode would normally be higher than in CCM mode. Since PSM ripple is rather hard to calculate accurately, the designer needs to verify this behavior in the end-application at light loads.

  b. Voltage sag during load transients

     The voltage sag during a load transient in CCM mode depends on the load step, control loop speed and output capacitor. An approximate formula for voltage sag during a fast load step is shown below:

     $$V_{SAG\_CCM} = \Delta I_{STEP} \left(ESR + \frac{1}{2 \cdot \pi \cdot C_{OUT} \cdot F_{BW}}\right)$$

     where ΔI_{STEP} is the load step amplitude and F_{BW} is the converter control bandwidth. Note that load step transitions between PSM and CCM mode operation will show higher voltage sag, because there is around 1% DC voltage difference between PSM mode and CCM mode. Converter bandwidth is normally set around 1/5 ~ 1/10 of the switching frequency, but the absolute value should stay below 80kHz. The converter bandwidth can be set via compensation resistor R_{COMP}.

- Input capacitor considerations:

  The input capacitor will act as a storage buffer to provide the high frequency switching current peaks of the converter. The input capacitor should be chosen to provide adequate filtering of the converter input, to minimize the V_{IN} high frequency ripple. Low ESR ceramic input capacitors should be placed close to the converter VIN pin and the Schottky diode ground connection. At high input voltages, ceramic capacitors will have severely reduced capacitance, which should be considered when calculating the input ripple voltage. The peak-peak input ripple voltage can be approximated by:

  $\Delta V_{IN\ pp} = \frac{I_{OUTmax} \cdot D}{C_{IN} \cdot F_{SW}} (1\text{-}D) + ESR \cdot I_{OUT}$ where $D = \frac{V_{OUT}}{V_{IN} \cdot \eta}$ and C_{IN} is the effective capacitance at the DC input voltage.

  It is recommended to keep the input ripple voltage below 1.3Vpp.

  For higher than 50V input supply, normally one or several 2.2µF/100V 1206 size MLCC capacitors will be needed depending on application load current.

  For higher current converters the input capacitor RMS current rating should also be checked:

  $I_{IN\_RMS} = I_{OUTmax} \sqrt{\frac{V_{OUT}}{V_{IN}} \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}$ The maximum RMS current will happen when V_{OUT} is 50% of V_{IN}.

  If the converter requires hot-plugging into live input supplies, it is recommended to add an electrolytic capacitor (e.g. 47µF/100V) in parallel with the ceramic input capacitor.

- Calculation of compensation components:

  The RTQ29xx/RTQ63xx series compensation can use standard current mode type II compensation. The below simple formulas can be used:

  The compensator gain is set by R_{COMP}, and the value is calculated to provide a suitable converter crossover frequency (F_C around 0.05 ~ 0.1*F_{SW}). $R_{COMP} = \frac{2\pi\, C_O \cdot F_C}{G_{mEA} \cdot G_{CS}} \cdot \frac{V_{OUT}}{V_{REF}}$. Note that F_C should not exceed 80kHz.

For higher input voltage supplies and supplies using electrolytic output capacitors it is recommended to use moderate bandwidth values.

The value of C_{COMP} is selected to set the compensation zero $f_Z = \frac{1}{2\pi \, C_{COMP} \cdot R_{COMP}}$ a bit below the converter load pole $f_{P_{LOAD}} = \frac{1}{2\pi \, C_{OUT} \cdot R_{LOAD}}$ where $R_{LOAD} = V_{OUT} / I_{OUT}$.

The value for C_{COMP2} is chosen to set the high frequency pole at the output capacitor ESR zero: $C_{COMP2} = \frac{C_{OUT} \cdot R_{ESR}}{R_{COMP}}$

When ceramic output capacitors are used, the ESR zero will lie at very high frequencies, above the converter switching frequency. In this case, choose C_{COMP2} for a high frequency pole at half the switching frequency: $C_{COMP2} = \frac{1}{\pi \cdot F_{SW} \cdot R_{COMP}}$

The feed-forward capacitor C_{FF} in parallel with the upper feedback resistor is normally not needed for improving control loop response. But some small C_{FF} capacitor in parallel with the upper feedback resistor can sometimes improve the PSM operation; by injecting some extra ripple on the FB pin, PSM double pulsing can be reduced. This can be tested case by case. Be careful when adding C_{FF} as it can push the converter bandwidth to high values, reducing the gain margin and leading to unstable behavior.

- RTQ29xx/RTQ63xx are asynchronous buck converters and need an external Schottky diode to conduct the inductor current when the high-side MOSFET is off. The Schottky diode should have sufficient voltage rating (≥ V_{IN_MAX}) and the forward voltage drop should be low to minimize power loss. The forward voltage drop should also be low enough to avoid current flow in the IC internal small low-side MOSFET body diode. The RTQ29xx/RTQ63xx datasheets provide graphs with maximum allowed forward voltage drop over temperature. To minimize switching losses, the Schottky diode junction capacitance and reverse recovery effects should be minimized. Finally the Schottky diode reverse leakage current at maximum reverse voltage and maximum ambient temperature should be checked, as high leakage current can lead to excessive diode dissipation and potential thermal runaway.
- The soft-start capacitor (DFN packages only) sets the time t_{SS} from EN high to V_{OUT} reaching its final value which is defined by $t_{SS} = \frac{(C_{SS} \cdot 1.1V)}{I_{SS}}$. C_{SS} is the value of the soft-start capacitor and I_{SS} is the soft-start current (typically 6μA). V_{OUT} starts rising when the V_{SS} ramp passes 0.3V, and ends when V_{SS} ramp passes 1.1V.
  The V_{OUT} rise time can therefore be calculated by: $t_r = \frac{(C_{SS} \cdot 0.8V)}{I_{SS}}$.
  Supplies with high output voltage and/or large value output capacitors should use sufficient soft-start time to avoid high inrush currents. Generally the soft-start time should be long enough to ensure the output capacitor can be fully charged without hitting the converter current limit. For PSOP-8 package versions, the soft-start time is internally fixed at 2msec.
- The converter can be enabled by pulling high the EN pin. The EN rising threshold is typically 1.25V. A fixed 0.9μA internal current source will enable the converter in case of floating EN pin. When the EN pin passes the EN rising threshold, an additional 2.9μA internal current source will be enabled, and totally 3.8μA will flow out of the EN pin.
  By connecting the EN pin via a resistor divider R_{EN1} and R_{EN2} between V_{IN} and ground, the part can start and stop at specific V_{IN} values: $R_{EN1} = \frac{V_{START} - V_{STOP}}{2.9\mu A}$ $R_{EN2} = \frac{1.25V}{\frac{V_{START} - 1.25V}{R_{EN1}} + 0.9\mu A}$
  The EN pin is 60V tolerant.
- The PGOOD pin (DFN packages only) signal can be used to monitor the output voltage. It is an open drain output and can be pulled up to an external voltage or the output voltage. To minimize switching noise pick-up, it is recommended to use 1k ~ 10kΩ pull-up resistors to reduce the chance of switching noise pick-up. The PGOOD pin is 60V tolerant.

3. First Example Application: 3.3V/0.5A Output

In this first example we will design a low current 3.3V MCU supply with a wide input voltage range from 12V to 60V, with a nominal value of 48V. This is a typical industrial MCU power supply example. We will use the RTQ63xx excel tool to show the step by step design.

The 60V maximum input voltage and the 0.5A max load current makes RTQ6360 the obvious choice. To provide a supply ready signal (Pgood) for the MCU, we will choose the DFN version RTQ6360GQW for this design. We will set the start-up voltage at 10V and shut-down voltage at 8V. The CCM output ripple should be less than 1% of the output voltage, and voltage sag during 0.2A to 0.5A load transient less than 5% of Vout. Figure 2 shows the Excel design tool input parameter section.

Please select the part number	RT(Q)6360	
Power supply design requirements		
Nominal input voltage, Vin_nominal	48	V
Maximum input voltage, Vin_max	60	V
Minimum input voltage, Vin_min	12	V
Output voltage, Vout	3.3	V
Nominal output current, Iout	0.5	A
Desired startup input voltage (enable start-up level)	10	V
Desired shut-down input voltage (enable shut-down level)	8	V
peak-to-peak output voltage ripple (%) in CCM mode	1	%
peak-to-peak output ripple, ΔVOUT	0.03	V
maximum output current during load step	0.5	A
minimum output current during load step	0.2	A
allowed output voltage drop during load step (%)	5	%
allowed voltage drop during load step VSAG	0.17	V

FIGURE 2

The first step in the design is to select the switching frequency. The excel tool will calculate the maximum switching frequency based on maximum input voltage, output voltage and minimum on-time. It will also calculate the maximum switching frequency based on output short-circuit condition: This is related to the minimum duty-cycle that the converter is able to achieve in output short-circuit with frequency fold-back. For this design, we'll set the frequency at 400kHz which will satisfy both conditions. See figure 3.

Select switching frequency		
Maximum allowable switching frequency, limited by Ton_min	0.42	MHz
Output voltage at short circuit condition	0.1	V
Maximum allowable switching frequency, limited by frequency foldback function	1.03	MHz
Switching Frequency selection, Fsw	0.4	MHz
RT resistor value_calculation	293.25	kΩ
RT resistor value selection	294	kΩ
Switching Frequency at selected RT	0.399	MHz
Forward conduction voltage of the freewheel diode	0.4	V
DC resistance of inductor	0.5	Ω
Minimum input voltage for normal operation without pulse skipping	3.89	V
Maximum input voltage for normal operation without pulse skipping	60.00	V

FIGURE 3

Next step is the inductor value calculation: For this design we will set the inductor ripple current at 30% of the IC rated current. The design tool will calculate the inductor value based on this ripple current. It will also calculate the minimum required inductance to satisfy the converter slope compensation requirement. We will choose 47uH inductance, which should have a saturation current that is higher than 0.58A.

Inductor setting		
Ratio of inductor ripple current relative to the rated output current	30	%
Inductance_calculation	51.35	uH
Minimum Inductance requirement for D > 50% condition	16.54	uH
Inductance selection	47	uH
△IL_calculation	0.16	A
IL_PEAK _calculation	0.58	A

FIGURE 4

For this design, a Würth Electronic WE-LQS 74404052470 type was choosen. Figure 5 shows the specifications.

Properties		Test conditions	Value	Unit	Tol.
Inductance	L	100 kHz/ 1 V	47	µH	±20%
Rated Current	I_R	ΔT = 40 K	0.8	A	max.
Saturation Current	I_{SAT}	|ΔL/L| < 30 %	0.95	A	typ.
DC Resistance	R_{DC}	@ 20 °C	521	mΩ	±20%
Self Resonant Frequency	f_{res}		11	MHz	typ.

FIGURE 5

The next step is the input capacitor selection. The design tool will calculate the required effective input capacitance to keep the peak-peak input voltage ripple lower than 1.3Vpp at worst case input voltage and output current.

Input capacitor selection		
Minimum effective input capacitance	0.061560998	uF
Input capacitance selection (rated value)	2.2	uF
Capacitance decrease change based on DC bias at nominal input voltage (%)	63	%
Capacitance decrease change based on DC bias at minimum input voltage (%)	8	%
Capacitance decrease change based on DC bias at maximum input voltage (%)	71	%
Effective input capacitance at nominal input voltage	0.814	uF
Effective input capacitance at minimum input voltage	2.024	uF
Effective input capacitance at maximum input voltage	0.638	uF
Input ripple at nominal input voltage and maximum load	0.10	V
Input ripple at minimum input voltage and maximum load	0.04	V
Input ripple at maximum input voltage and maximum load	0.13	V
Input capacitor RMS current at nominal input voltage and maximum load	0.03	A
Input capacitor RMS current at minimum input voltage and maximum load	0.12	A
Input capacitor RMS current at maximum input voltage and maximum load	0.11	A

FIGURE 6

For this design, a single 2.2µF/100V MLCC capacitor HMK316AC7225KL-TE was chosen. Since the effective capacitance highly depends on input DC voltage, we should enter the capacitance decrease rate at nominal, minimum and maximum input voltage: The capacitance decrease over DC bias can be found from the capacitance characteristics datasheet, see figure 7 left side. The design tool will then calculate the effective input capacitance and the expected input voltage ripple at each input voltage. It will also calculate the maximum RMS current in the input capacitor. You can then check the temperature rise of the capacitor at this condition (figure 7 right side). In this design the RMS ripple current is very small and hardly leads to any dissipation in the capacitor.

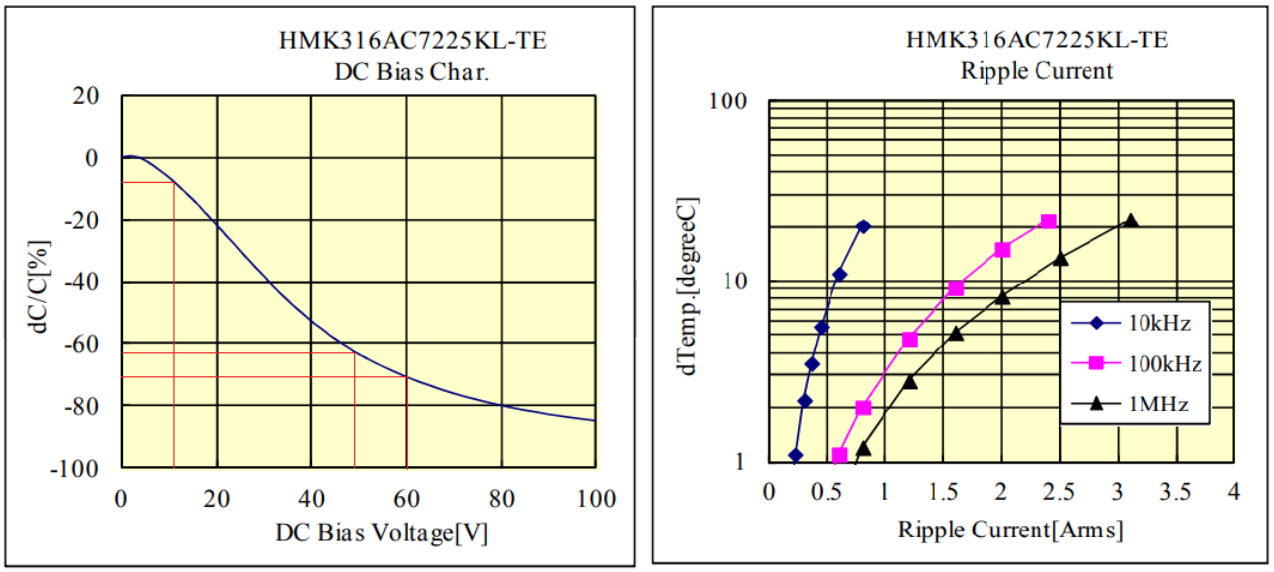


FIGURE 7

The next step is the output capacitor selection. Its value will determine the output voltage ripple and the voltage sag during load transient at a given load step and converter control bandwidth. For this design we'll set the control bandwidth at 10% of the switching frequency. The load step voltage sag requirement will now define the minimum required effective output capacitance value, which is 7.26µF.

Output capacitor selection		
crossover frequency setting, % of the switching frequency	10	%
crossover frequency setting	0.039898979	MHz
Minimum effective output capacitance for voltage ripple (No ESR consideration)	1.42	uF
Minimum effective output capacitance to meet output voltage transient requirement	7.26	uF
Output capacitance selection	20.00	uF
Capacitance decrease change rate based on DC bias (%)	35	%
Effective output capacitance value	13	uF
Maximum allowed ESR to meet the output ripple requirement, ESR_max	0.201369322	Ω
ESR of selected output capacitance	0.002	Ω
output ripple at effective output capacitance and selected ESR	4.277104398	mV
output voltage sag during load step with effective output capacitance and selected ESR	92.6993301	mV

FIGURE 8

For this design, two small size 10µF/16V X5R 0805 EMK212ABJ106KG capacitors were chosen. It is very important to include the capacitance decrease due to DC bias as well (see figure 9), as it will affect output ripple, voltage sag and converter stability. After the rated capacitance and capacitance % decrease at 3.3V DC bias has been entered in the design tool, it will calculate the effective total output capacitance, the minimum required ESR to meet the output ripple specification, and the actual output ripple and voltage sag.

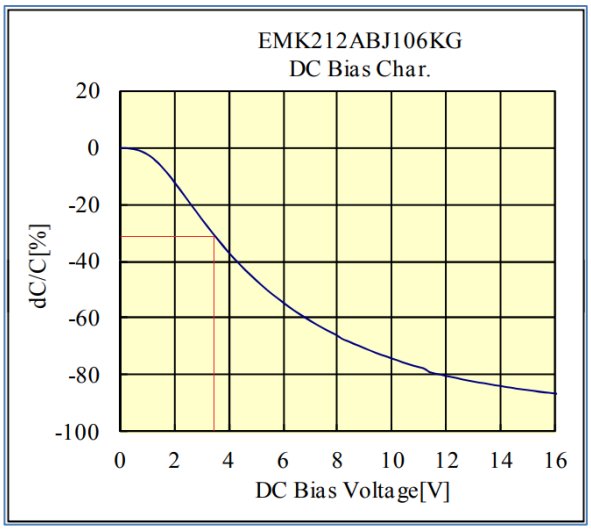


FIGURE 9

Next step is the Freewheel diode selection. The RTQ29xx/RTQ63xx series require an external Schottky diode to provide a current path for the inductor current when the high-side MOSFET is off. The forward drop of the Schottky diode should be low, to reduce the power loss in the diode, but also to avoid current flow in the IC internal small low-side MOSFET that is used for boot strap capacitor re-charge in light load. (see figure 10). This means that the forward voltage drop of the Schottky diode at maximum load current should be low compared to the body diode of the IC internal low side MOSFET. For Schottky diodes this is normally not a problem.

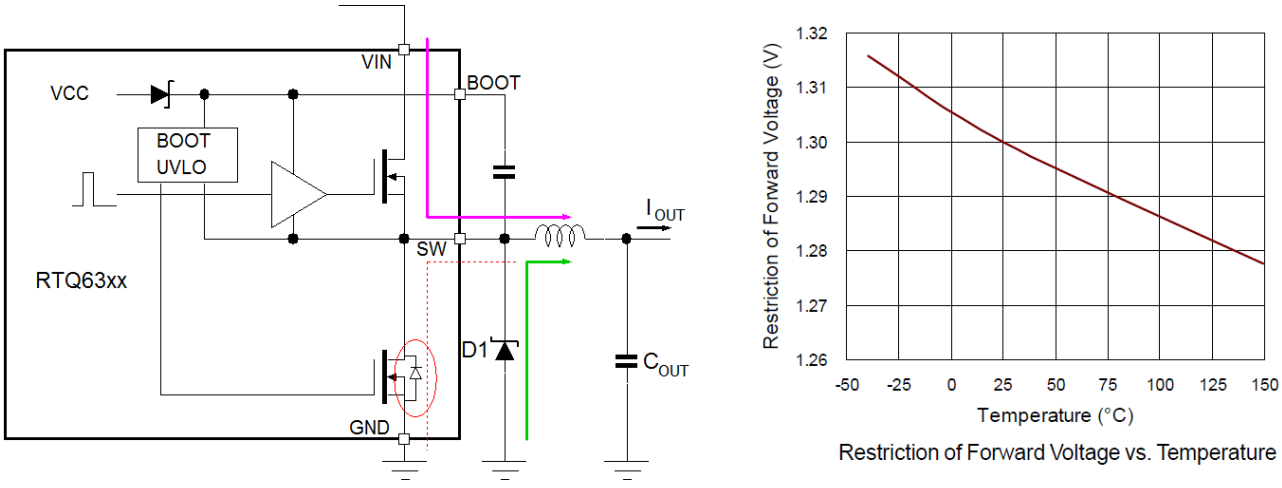
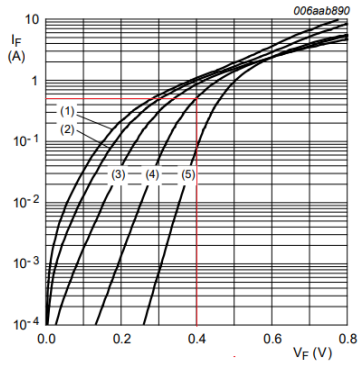


FIGURE 10

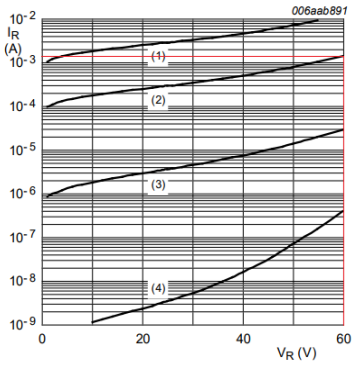
For this low current supply, switching losses will be a major part of the total losses. The Schottky diode capacitance and reverse recovery effects should be minimized. Finally, since this supply can work with input voltage up to 60V, the Schottky diode voltage rating should be sufficient, and reverse leakage current at maximum reverse voltage and maximum ambient temperature should be checked as well.

For this design a 60V/1A PMEG6010ER Schottky diode was chosen. The important parameters are shown in figure 11.



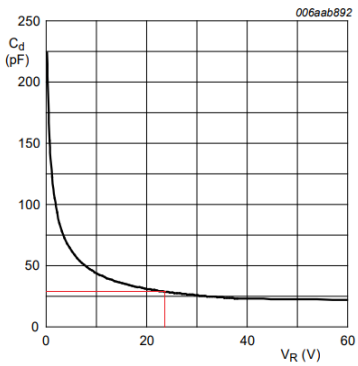
(1) T_j = 150 °C
(2) T_j = 125 °C
(3) T_j = 85 °C
(4) T_j = 25 °C
(5) T_j = −40 °C

Forward current as a function of forward voltage; typical values



(1) T_j = 125 °C
(2) T_j = 85 °C
(3) T_j = 25 °C
(4) T_j = −40 °C

Reverse current as a function of reverse voltage; typical values



f = 1 MHz; T_{amb} = 25 °C

Diode capacitance as a function of reverse voltage; typical values

FIGURE 11

The PMEG6010ER forward voltage at 25°C and 0.5A is 0.4V and the diode worst case forward voltage values will not come close to the limit values as shown in the RTQ6360 datasheet. At 85°C ambient and 60V reverse voltage, the reverse leakage current is 1.3mA. The power loss due to leakage current is $D*V_{IN}*I_{LEAKAGE}$ = 0.055*60*0.0013 = 4mW, which will not have much impact on the converter efficiency and will not cause thermal runaway. The Schottky diode junction capacitance is highly dependent on diode reverse voltage. This capacitance influences the IC internal high-side MOSFET switching losses, so lower capacitance Schottky diodes will reduce the switching losses, especially at higher input voltages.

The calculation of the feedback resistors is straightforward: the designer inputs the low-side feedback resistor and the tool calculates the high-side resistor.

Feedback resistor selection for output voltage programming		
Reference voltage	0.8	V
Low side feedback resistor selection	24	Kohm
High side feedback resistor_calculation	75	Kohm
High side feedback resistor selection	75	Kohm
output voltage at selected feedback resistors	3.3	V

FIGURE 12

The calculation of the compensation resistor R_{COMP} is based on the previously entered converter bandwidth, the effective output capacitance and the IC parameters. C_{COMP} is then calculated to set the compensation zero to coincide with the converter load pole. For low ESR ceramic output capacitors, the C_{COMP2} capacitors is calculated to set the compensator pole at half the switching frequency. Please note that RTQ6360 COMP pin internally has 5.7pF to ground, so the external C_{COMP2} value can be 5.7pF lower than the calculated one. See figure 13.

Compensation Circuit design		
Output capacitance selection	20.00	uF
Capacitance decrease change rate based on DC bias (%)	35.00	%
Effective output capacitance value	13	uF
Rcomp_calculation	69.44	Kohm
Rcomp selection	68	Kohm
RL	6.6	ohm
Ccomp_calculation	1.26	nF
Ccomp selection	1.2	nF
Ccomp2 (Option when using E-cap with high ESR)		
ESR of selected output capacitance	0.002	Ω
Ccomp2_calculation	0.000382353	nF
Ccomp2 selection		nF
Ccomp2 (Option when using MLCC output cap and enhance noise immunity)		
Ccomp2_calculation	11.70850506	pF
Ccomp2 selection	5.6	pF

FIGURE 13

The design can be finalized with the calculation of the Enable resistor divider and Soft-start capacitor: With the entered V_{IN} start and stop voltages, the design tool calculates the recommended upper R_{EN1} resistor, and after entering the actual value, it calculates the second R_{EN2} resistor and shows the actual start and stop levels based on the actual resistor values used.
The soft-start time for the 3.3V converter is not critical and we choose an arbitrary 3msec soft-start time, which requires a 10nF soft-start capacitor. The PGOOD pin is pulled up with a 4.7kΩ to V_{OUT}. See figure 14.

EN Pin for Start-Up and UVLO Adjustment		
VIN UVLO resistor REN1	689.6551724	Kohm
VIN UVLO resistor REN1 selection	680	Kohm
VIN UVLO resistor REN2	90.79256569	Kohm
VIN UVLO resistor REN2 selection	91	Kohm
Start-up input voltage with selected resistors	9.978659341	V
Shut-down input voltage with selected resistors	8.006659341	V
Soft start time		
Desired Soft start time	3	ms
Minimum Css limited by effective output capacitance at no load.	0.173590053	nF
CSS/TR calculation	9.38	nF
CSS/TR selection	10	nF
Soft start time with selected CSS capacitor	3.20	ms
PS: Only the RT(Q)636XGQW (DFN package) provides adjustable soft-start function.		
Power-Good Output		
It is recommended to use pull-up resistance between the values of 1 and 10kΩ to reduce the switching noise coupling to PGOOD pin.		

FIGURE 14

The complete application circuit and a PCB layout example is shown in figure 15.

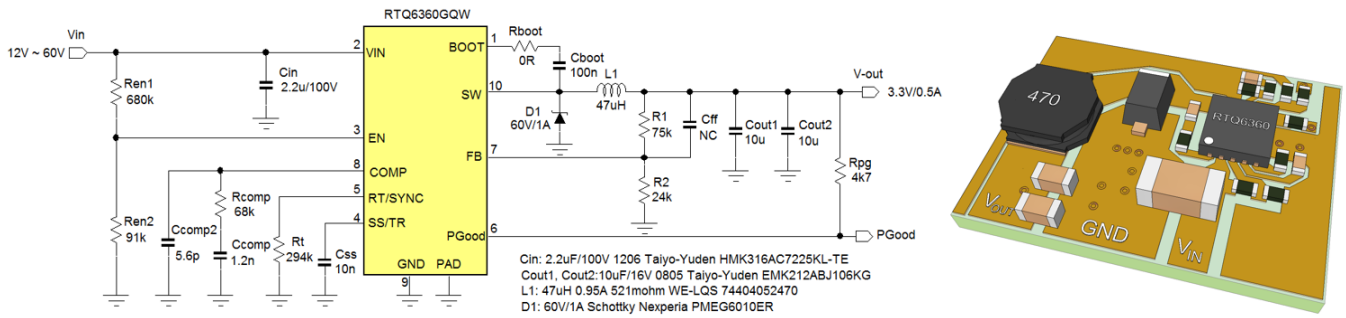


FIGURE 15

The circuit was built on the RTQ6360GQW evaluation board, and the all performance items were measured and compared with calculated values:

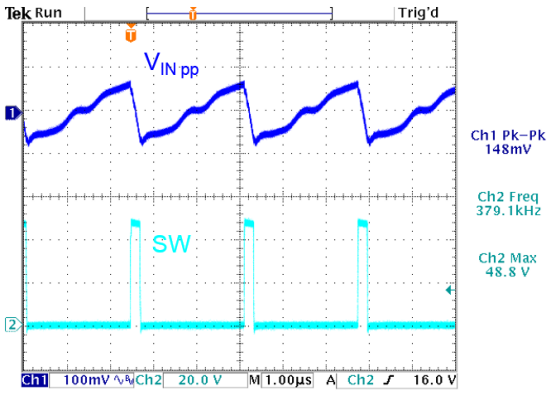


FIGURE 16

Measurement of input ripple at V_{IN} = 48V, V_{OUT} = 3.3V, 0.5A load
Calculated value: 100mVpp, measured value: 148mVpp

Output ripple in PSM mode V_{IN} = 48V, V_{OUT} = 3.3V, 1mA load

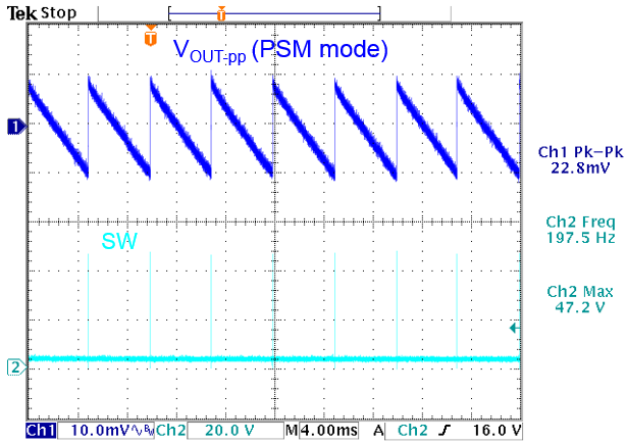
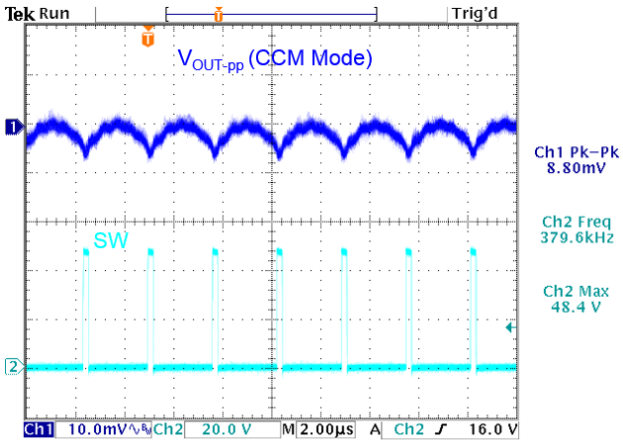


FIGURE 17

Measured value: 22.8mVpp

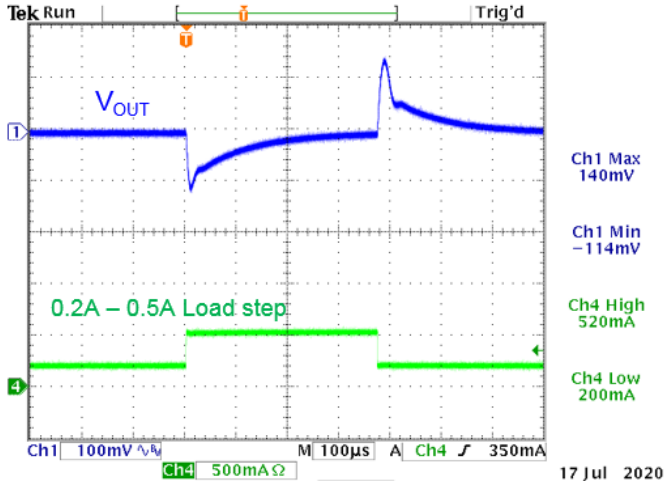
Output ripple in CCM mode V_{IN} = 48V, V_{OUT} = 3.3V, 0.5A load



Calculated value: 4.3mVpp, measured value: 8.8mVpp

The converter voltage sag during load step was measured by using the Richtek Fast Load transient Tool.

V_{IN} = 48V, 0.2A ~ 0.5A fast load step



V_{IN} = 24V, 0.2A ~ 0.5A fast load step

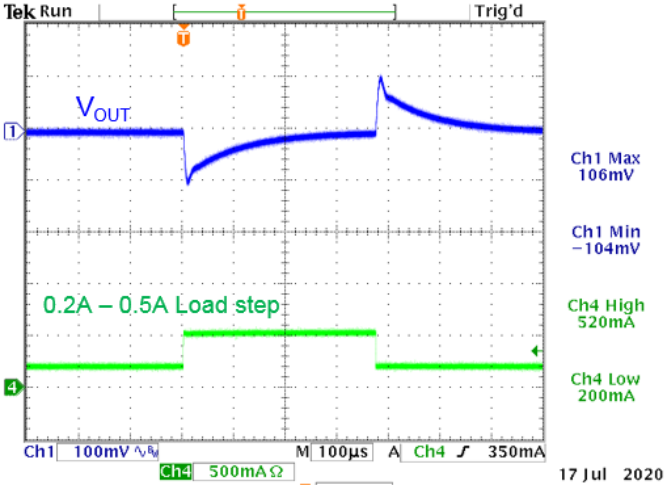


FIGURE 18

Calculated value:92mV; measured value: 114mV

Calculated value: 92mV, measured value: 104mV

The step load response at 48V input voltage in figure 18 left side is a bit different from the 24V input condition (figure 18 right side), especially the overshoot when load goes from 0.5A to 0.2A. During sudden load drop, the converter will try to quickly reduce its on-time. At 48V input, the converter is already working close to its minimum on time, so the headroom in on-time reduction is limited, hence resulting in larger overshoot. The step load in both cases shows a small ring, which points to lower phase margin.

A gain-phase measurement (figure 19) shows this more clearly:

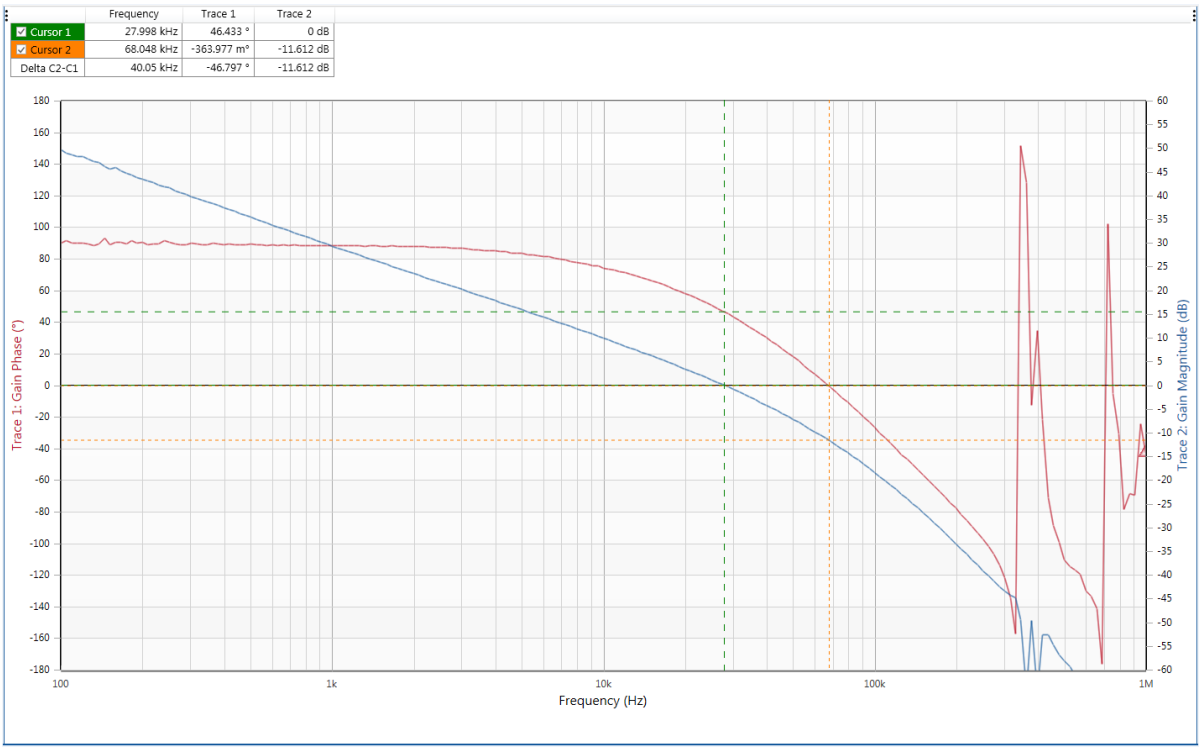


FIGURE 19 VIN = 48V, VOUT = 3.3V / 0.5A LOAD: BANDWIDTH = 28KHZ, PHASE MARGIN 46 DGS

The gain-phase Bode plot shows that the loop phase drops quite fast above the crossover frequency. This can be slightly improved by removing the C_{COMP2} capacitor of 5.6pF:

Figure 20 shows the gain-phase measurement result when C_{COMP2} is removed: The phase margin is slightly better.

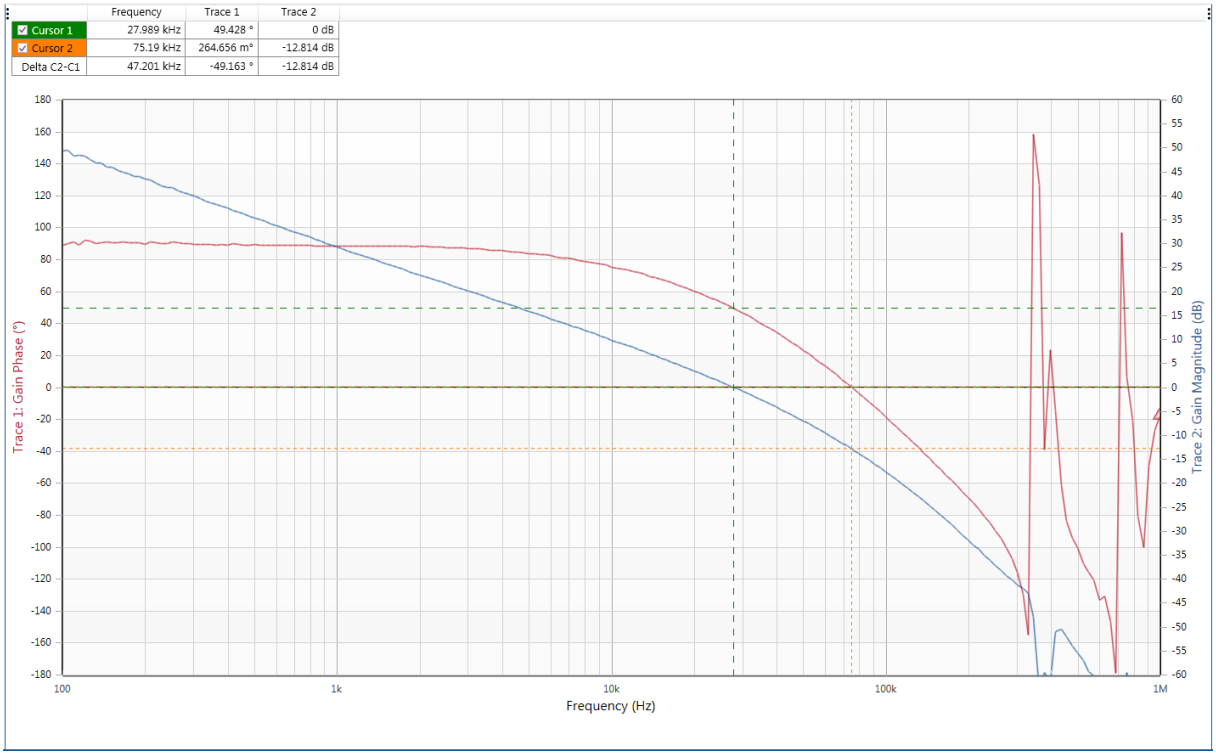
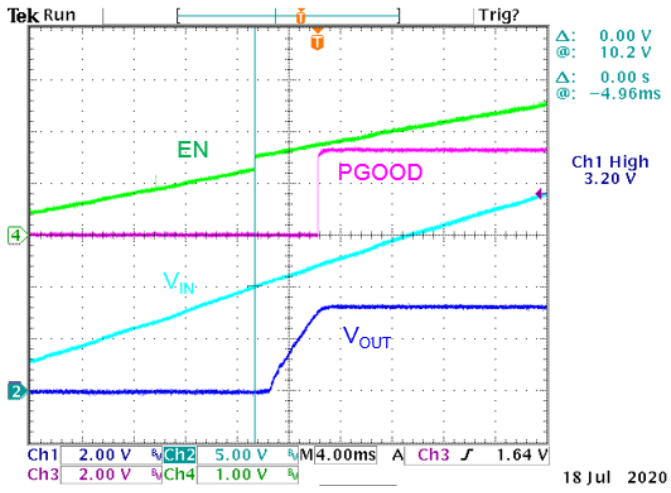


FIGURE 20 VIN = 48V, VOUT = 3.3V/0.5A LOAD AND REMOVED CCOMP2 CAPACITOR: BANDWIDTH = 28KHZ, PHASE MARGIN 49 DGS

If better phase margin is required, it is recommended to set the converter bandwidth frequency setting percentage at a lower value (e.g. 7% instead of 10% of F_{SW}) at the expense of slightly larger voltage sag during load steps and re-calculating the R_{COMP}, C_{COMP} and C_{COMP2} values.

The converter start-up from V_{IN} and Shut-down from V_{IN} was also measured. The measurement results match the calculated values quite well. The small hysteresis step in the Enable signal can be seen when it passes the threshold. See figure 21.

Start-up at rising V_{IN}:



Shut-down at falling V_{IN}:

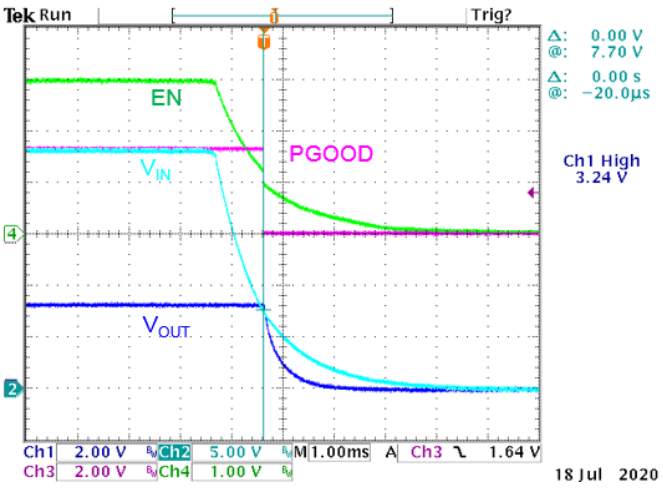


FIGURE 21

V_{START} calculated: 10V; V_{START} measured: 10.2V

V_{STOP} calculated: 8V; V_{STOP} measured: 7.7V

The converter efficiency was also measured at different input voltages: Figure 22 shows that the efficiency is highly dependent on the input voltage.

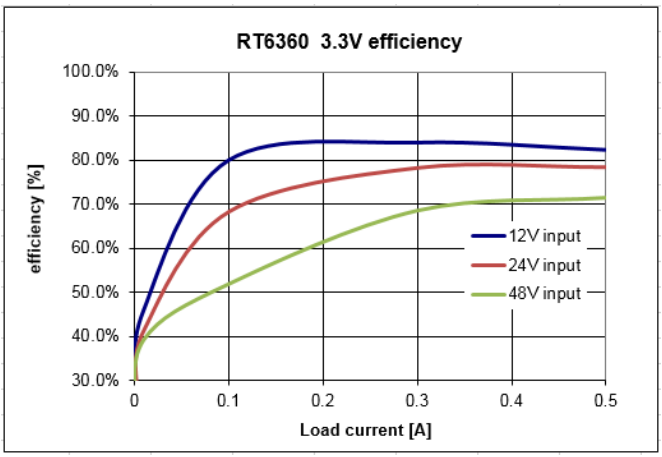


FIGURE 22

Since efficiency = P_{OUT} / (P_{OUT} + P_{LOSS}) it is useful to analyze the power losses of the converter.

Condition	Vin	Iin	Vout	Iout	efficiency	Ploss
12V-3.3V, 0.5A	12.3	0.1638	3.305	0.5	82.3%	0.356
24V-3.3V, 0.5A	24.2	0.08719	3.305	0.5	78.4%	0.456
48V-3.3V, 0.5A	48.1	0.04819	3.305	0.5	71.3%	0.665

As can be seen, the total power losses at 48V input are almost double of the losses in 12V input condition, which is mainly caused by the higher switching losses at higher input voltage.

4. SECOND EXAMPLE APPLICATION: 24V/3A (72W) OUTPUT

In this second example we will design a 24V/3A converter running from an industrial 48V supply. This is a high power design and correct component selection is quite important.

For the IC selection we can either choose the RTQ6363 (3.5A version) or the RTQ6365 (5A) version). The R_{DSON} of the 5A version is slightly better than the 3.5A version, but the 5A version has higher current limit, which means that an inductor with larger saturation current must be used. In this example, we will select the RTQ6363, and choose the DFN 4x4-package version RTQ6363GQW, which has better thermal resistance compared to the PSOP-8 package.

We will use the RTQ63xx excel design tool again to calculate the component values.

We will set the start-up voltage at 35V and shut-down voltage at 28V, which ensures clean start-up of the power supply. CCM output ripple should be less than 1% of the output voltage, and voltage sag during 1A to 3A load transient should be less than 5% of Vout. Figure 23 shows the Excel design tool input parameter section.

Power supply design requirements		
Nominal input voltage, Vin_nominal	48	V
Maximum input voltage, Vin_max	55	V
Minimum input voltage, Vin_min	44	V
Output voltage, Vout	24	V
Nominal output current, Iout	3	A
Desired startup input voltage (enable start-up level)	35	V
Desired shut-down input voltage (enable shut-down level)	28	V
peak-to-peak output voltage ripple (%) in CCM mode	1	%
peak-to-peak output ripple, ΔVOUT	0.24	V
maximum output current during load step	3	A
minimum output current during load step	1	A
allowed output voltage drop during load step (%)	5	%
allowed voltage drop during load step VSAG	1.20	V

FIGURE 23

The first step in the design is to select the switching frequency. The excel tool will calculate the maximum switching frequency based on maximum input voltage, output voltage and minimum on-time, as well as the maximum switching frequency based on output short-circuit condition. As the duty-cycle for this 48V ~ 24V design lies around 50%, the minimum on-time will not easily be reached, allowing higher switching frequencies. But it is not wise to choose high switching frequencies for 48V input supplies as the switching losses will increase considerably. To minimize the switching losses, we will set the frequency at 300kHz. See figure 24.

Select switching frequency		
Maximum allowable switching frequency, limited by Ton_min	3.23	MHz
Output voltage at short circuit condition	0.1	V
Maximum allowable switching frequency, limited by frequency foldback function	1.08	MHz
Switching Frequency selection, Fsw	0.3	MHz
RT resistor value_calculation	332.14	kΩ
RT resistor value selection	330	kΩ
Switching Frequency at selected RT	0.302	MHz
Forward conduction voltage of the freewheel diode	0.55	V
DC resistance of inductor	0.05	Ω
Minimum input voltage for normal operation without pulse skipping	25.74	V
Maximum input voltage for normal operation without pulse skipping	60.00	V

FIGURE 24

Next step is the inductor value calculation: With the selecting 30% ripple current, the design tool will calculate the inductor value based on this ripple current to be 38µH. The minimum required inductance to satisfy the converter slope compensation requirement is 27µH. We will choose 47µH inductance, which will give an 850mApp current ripple. The inductor saturation current should be higher than 3.4A and the RTQ6363GQW 5.5A peak current limit should also be considered when choosing the inductor saturation current.

Inductor setting		
Ratio of inductor ripple current relative to the IC rated output current	30	%
Inductance_calculation	38.10	uH
Minimum Inductance requirement for D > 50% condition	27.5862069	uH
Inductance selection	47	uH
△IL_calculation	0.85	A
IL_PEAK _calculation	3.43	A

FIGURE 25

For this design, a Würth Electronic WE-PD 7447709470 type was choosen which has 4.5A saturation current. Figure 26 shows the specifications. Slight saturation during over-current situations is allowed.

Properties		Test conditions	Value	Unit	Tol.
Inductance	L	1 kHz/ 250 mV	47	µH	±20%
Rated Current	I_R	ΔT = 40 K	3.8	A	max.
Saturation Current	I_{SAT}	|ΔL/L| < 10 %	4.5	A	typ.
DC Resistance	R_{DC}	@ 20 °C	46	mΩ	typ.
DC Resistance	R_{DC}	@ 20 °C	60	mΩ	max.
Self Resonant Frequency	f_{res}		6.5	MHz	typ.
Operating Voltage	V		120	V	max.

FIGURE 26

The next step is the input capacitor selection. The design tool will calculate the required effective input capacitance to keep the peak-peak input voltage ripple lower than 1.3Vpp at worst case input voltage and output current.

Input capacitor selection		
Minimum effective input capacitance	1.923076923	uF
Input capacitance selection (rated value)	6.6	uF
Capacitance decrease change based on DC bias at nominal input voltage (%)	61	%
Capacitance decrease change based on DC bias at minimum input voltage (%)	54	%
Capacitance decrease change based on DC bias at maximum input voltage (%)	70	%
Effective input capacitance at nominal input voltage	2.574	uF
Effective input capacitance at minimum input voltage	3.036	uF
Effective input capacitance at maximum input voltage	1.98	uF
Input ripple at nominal input voltage and maximum load	0.97	V
Input ripple at minimum input voltage and maximum load	0.82	V
Input ripple at maximum input voltage and maximum load	1.26	V
Input capacitor RMS current at nominal input voltage and maximum load	1.06	A
Input capacitor RMS current at minimum input voltage and maximum load	1.10	A
Input capacitor RMS current at maximum input voltage and maximum load	1.49	A

FIGURE 27

For this design, we will use three pieces 2.2µF/100V MLCC capacitors HMK316AC7225KL-TE in parallel to get sufficient capacitance at high input voltage. After we enter the capacitance decrease rate at nominal, minimum and maximum input voltage from the capacitor datasheet graph, the design tool will calculate the effective input capacitance and the expected input voltage ripple at each input voltage. It will also calculate the maximum RMS current in the input capacitor. As we use three capacitors in parallel, each capacitor will see 1/3 of the calculated RMS current so worst case RMS current in each capacitor is 0.5A. As you can see in figure 28 right side, the temperature rise of the capacitor at this condition is still small.

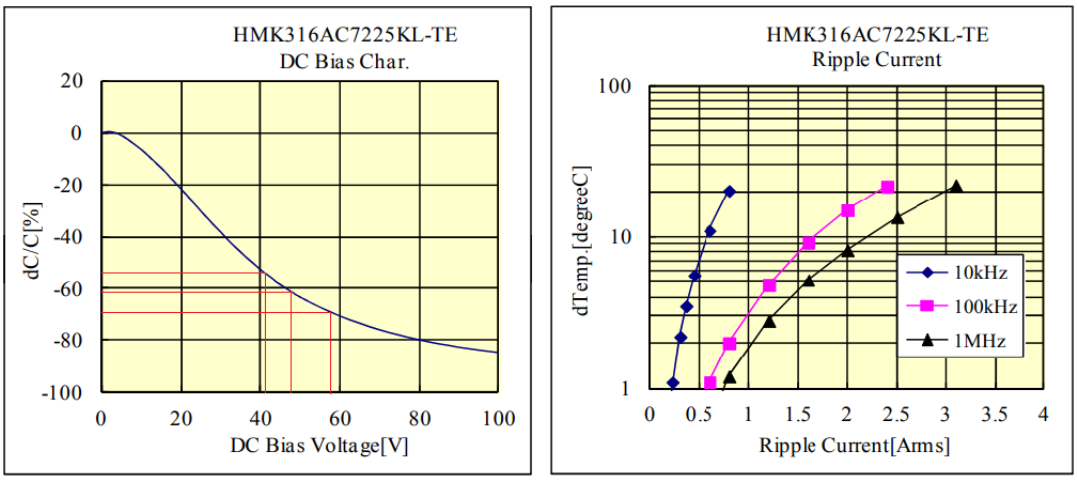


FIGURE 28

The next step is the output capacitor selection. Its value will determine the output voltage ripple and the voltage sag during load transient at a given load step and converter control bandwidth. For the high voltage and high power design moderate control bandwidth is recommended. We start with a control bandwidth of 10% of the switching frequency. The load step voltage sag requirement will now define the minimum required effective output capacitance value, which is 8.85µF.

Output capacitor selection		
crossover frequency setting, % of the switching frequency	10	%
crossover frequency setting	0.03	MHz
Minimum effective output capacitance for voltage ripple (No ESR consideration)	1.82	uF
Minimum effective output capacitance to meet output voltage transient requirement	8.85	uF
Output capacitance selection	20.00	uF
Capacitance decrease change based on DC bias (%)	40	%
Effective output capacitance value	12	uF
Maximum allowed ESR to meet the output ripple requirement, ESR_max	0.281999965	Ω
ESR of selected output capacitance	0.002	Ω
output ripple at effective output capacitance and selected ESR	31.25295508	mV
output voltage sag during load step with effective output capacitance and selected ESR	888.6426044	mV

FIGURE 29

For this design, two 1210 size 10µF/50V X7S UMR325AC7106KM capacitors in parallel were chosen. It is very important to include the capacitance decrease due to DC bias as well (see figure 30), to ensure correct compensation calculation results. This capacitor type drops around 40% at 24Vdc. After the rated capacitance and 40% decrease at 24V has been entered, the design tool will calculate the effective total output capacitance, the minimum required ESR to meet the output ripple specification, and the actual output ripple and voltage sag.

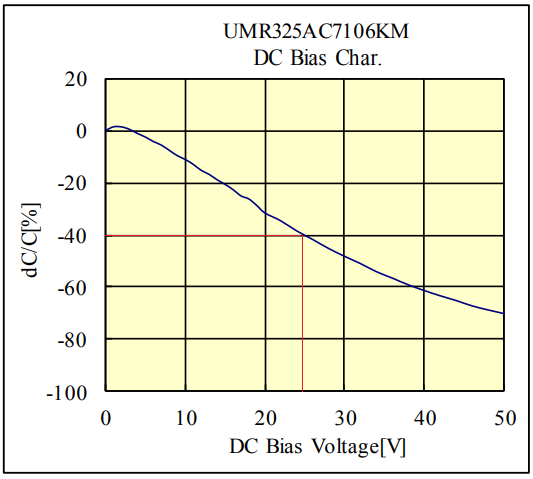


FIGURE 30

Next step is the freewheel diode selection. The total power dissipation in this design will be high, resulting in higher operation temperatures of the power components. It is therefore important to select parts that will operate reliably at high temperatures. With larger Schottky diodes, reverse leakage currents can be a critical parameter at high temperatures, and for this design we selected a Trench type 60V/5A PMEG060T050ELPE Schottky which exhibits lower reverse leakage current compared to normal planar Schottky diodes [1]. The important parameters are shown in figure 31.

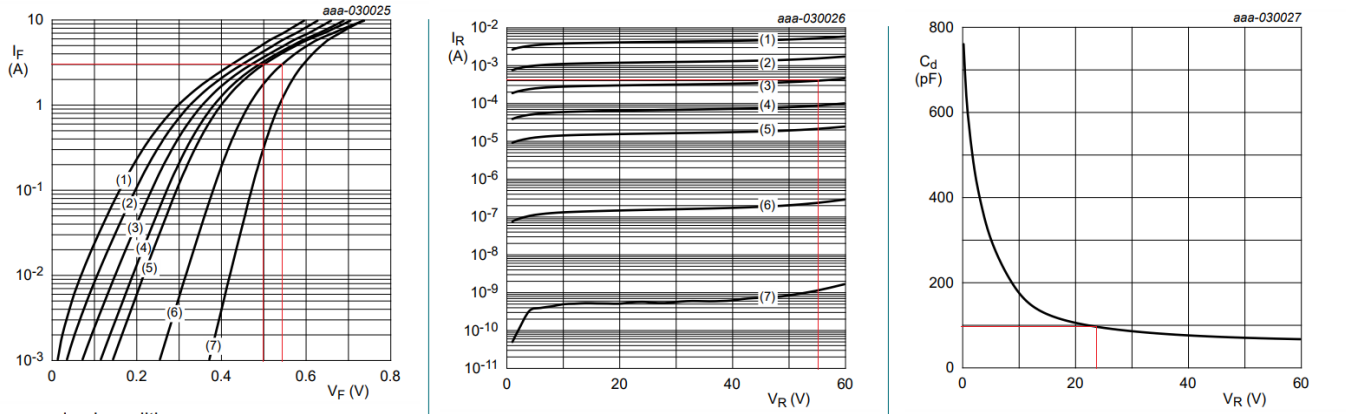


FIGURE 31

At 125°C ambient and 55V reverse voltage, the reverse leakage current is 0.4mA. The power loss due to leakage current is very low: $D*V_{IN}*I_{LEAKAGE}$ = 0.45*55*0.0004 = 9.9mW.
The junction capacitance is highly dependent on diode reverse voltage. As this capacitance influences the IC internal high side MOSFET switching losses, Schottky diodes with lower capacitance can help reduce switching losses, although the reverse recovery charge of the diode will also play a role [1].

The PMEG060T050ELPE forward voltage at 25°C and 3A is 0.54V and the diode worst case forward voltage values will not come close to the limit values as shown in the RTQ6363 datasheet, so there is no risk of current flow in the body diode of the RTQ6363 small low side MOSFET. See figure 32.

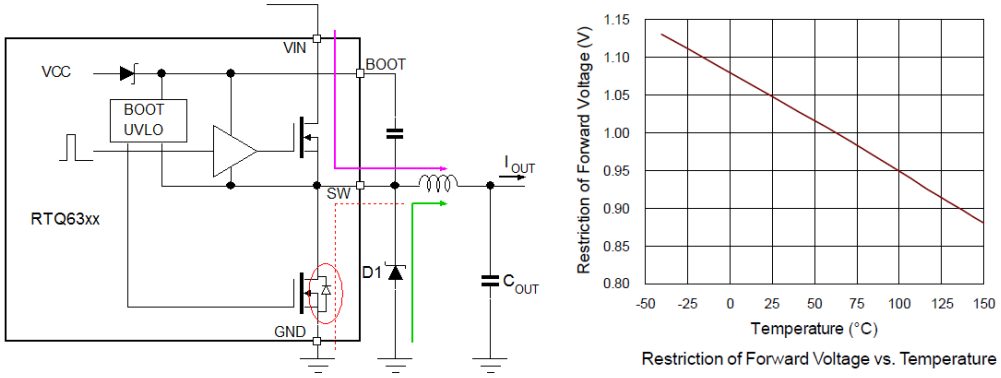


FIGURE 32

The calculation of the feedback resistors is straightforward: the designer inputs the low-side feedback resistor and the tool calculates the high-side resistor.

Feedback resistor selection for output voltage programming		
Reference voltage	0.8	V
Low side feedback resistor selection	4.7	Kohm
High side feedback resistor_calculation	136.3	Kohm
High side feedback resistor selection	137	Kohm
output voltage at selected feedback resistors	24.11914894	V

FIGURE 33

The calculation of the compensation resistor R_{COMP} is based on the previously entered converter bandwidth, the effective output capacitance and the IC parameters. C_{COMP} is then calculated to set the compensation zero to coincide with the converter load pole. For low ESR ceramic output capacitors, the C_{COMP2} capacitors is calculated to set the compensator pole at half the switching frequency. Please note that RTQ6363 COMP pin internally has 26pF to ground, so the external C_{COMP2} value can be 26pF lower than the calculated one. See figure 34.

Compensation Circuit design		
Output capacitance selection	20.00	uF
Capacitance decrease change rate based on DC bias (%)	40.00	%
Effective output capacitance value	12	uF
Rcomp_calculation	12.91	Kohm
Rcomp selection	13	Kohm
RL	8	ohm
Ccomp_calculation	7.38	nF
Ccomp selection	8.2	nF
Ccomp2 (Option when using E-cap with high ESR)		
ESR of selected output capacitance	0.002	Ω
Ccomp2_calculation	0.001846154	nF
Ccomp2 selection		nF
Ccomp2 (Option when using MLCC output cap and enhance noise immunity)		
Ccomp2_calculation	81.65931733	pF
Ccomp2 selection	56	pF

FIGURE 34

The 48V to 24V design duty-cycle does not reach 65%, so the external bootstrap charge circuit is not needed.

Bootstrap Driver Supply		
Dnom, nominal duty cycle	50	%
Dmin, minimum duty cycle	43.63636364	%
Dmax, maximum duty cycle	54.54545455	%

Please add an external bootstrap diode between an external 5V voltage supply and the BOOT pin to improve enhancement of the high-side MOSFET and improve efficiency when the input voltage is below 5.5V or duty cycle is higher than 65%.

The bootstrap diode can be a fast small signal diode with voltage rating of Vin_max, such as 1N4148.

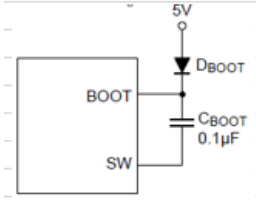


FIGURE 35

Finally the Enable resistor divider and Soft-start capacitor can be calculated. As the effective output capacitance (12µF) is relatively low the inrush current during soft-start is also low. We choose the 3msec soft-start time again, which requires a 10nF soft-start capacitor. See figure 36.

The PGOOD pin in this example is pulled up with a 10kΩ to V_{OUT}, but for power sequencing it could be pulled up to an external low voltage supply or apply a resistor divider from V_{OUT}.

EN Pin for Start-Up and UVLO Adjustment		
VIN UVLO resistor REN1	2058.823529	Kohm
VIN UVLO resistor REN1 selection	2000	Kohm
VIN UVLO resistor REN2	66.29834254	Kohm
VIN UVLO resistor REN2 selection	68	Kohm
Start-up input voltage with selected resistors	34.09411765	V
Shut-down input voltage with selected resistors	27.29411765	V

Soft start time		
Desired Soft start time	3	ms
Minimum Css limited by effective output capacitance at no load.	0.14771601	nF
CSS/TR calculation	7.97	nF
CSS/TR selection	10	nF
Soft start time with selected CSS capacitor	3.76	ms
PS: Only the RT(Q)636XGQW (DFN package) provides adjustable soft-start function.		

Power-Good Output

It is recommended to use pull-up resistance between the values of 1 and 10kΩ to reduce the switching noise coupling to PGOOD pin.

FIGURE 36

The complete application circuit and a PCB layout example is shown in figure 37.

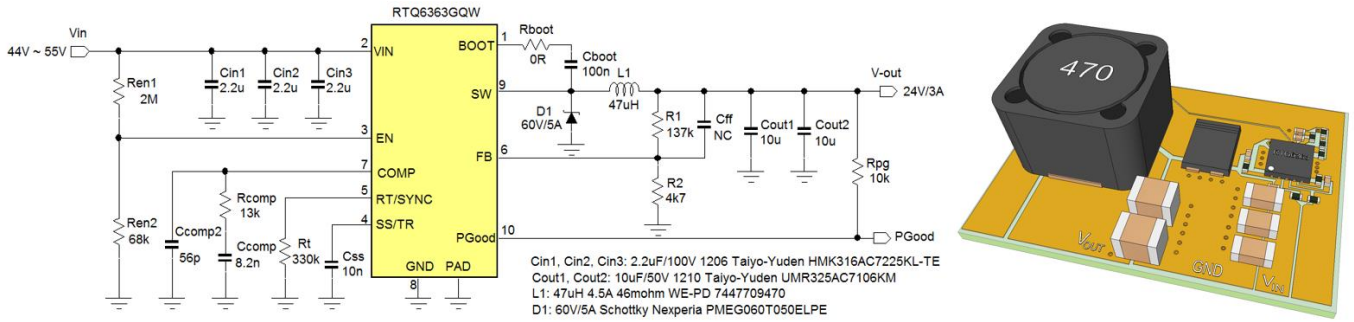
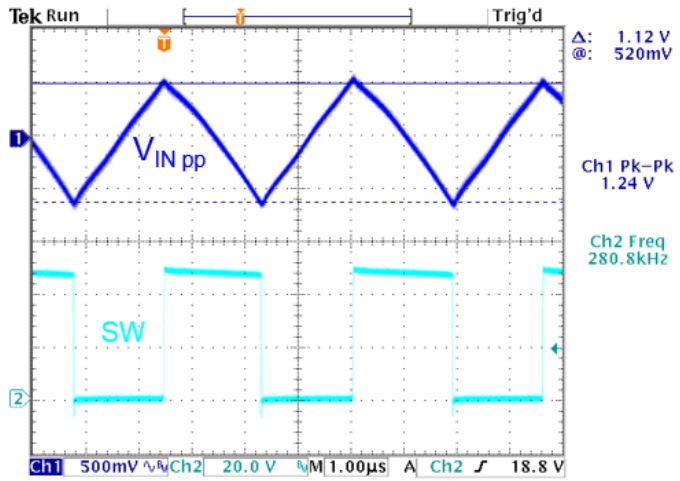


FIGURE 37

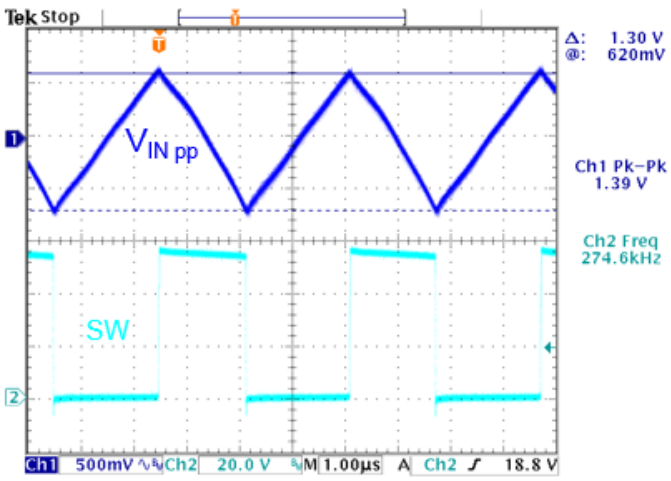
The circuit was built on the RTQ6363GQW evaluation board, and the all performance items were measured and compared with calculated values:

Input ripple measurement at V_{IN} = 48V, V_{OUT} = 24V, 3A load



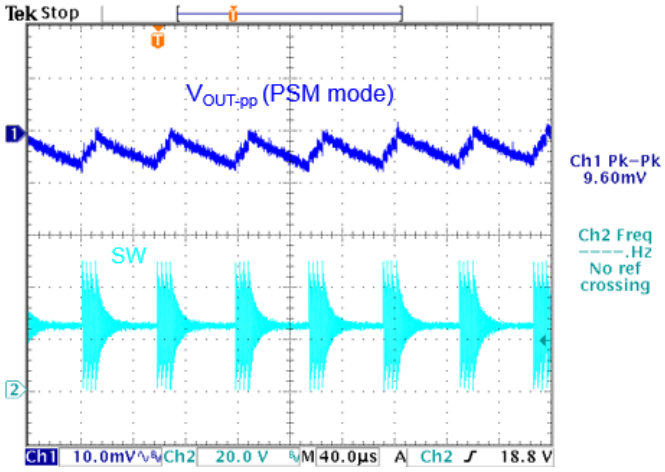
Calculated value: 0.97Vpp, measured value: 1.12Vpp

Input ripple measurement at V_{IN} = 55V, V_{OUT} = 24V, 3A load



Calculated value: 1.26Vpp, measured value: 1.30Vpp

Output ripple in PSM mode V_{IN} = 48V, V_{OUT} = 24V, 1mA load



Output ripple in CCM mode V_{IN} = 48V, V_{OUT} = 24V, 3A load

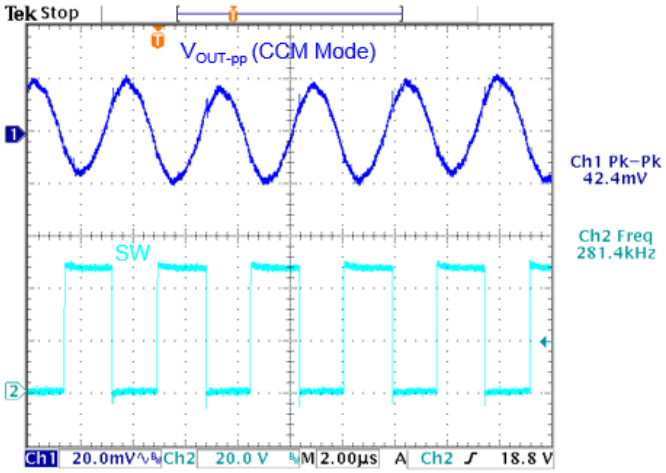


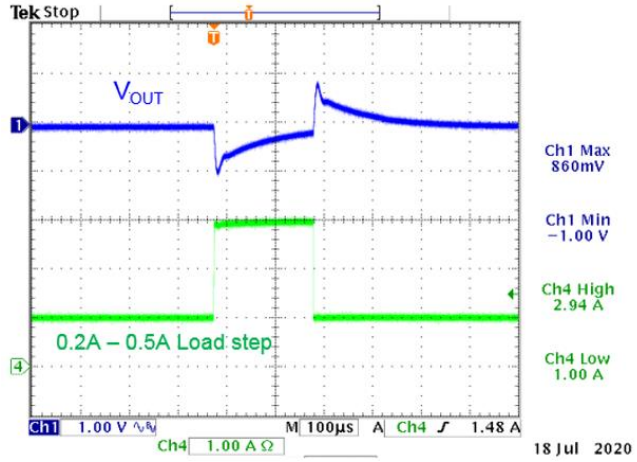
FIGURE 39

Measured value: 9.6mVpp

Calculated value: 32mVpp, measured value: 42mVpp

The converter voltage sag during load step was measured by using the [Richtek Fast Load transient Tool].

V_{IN} = 48V, 1A ~ 3A fast load step



V_{IN} = 48V, 1A ~ 3A fast load step estimate bandwidth:

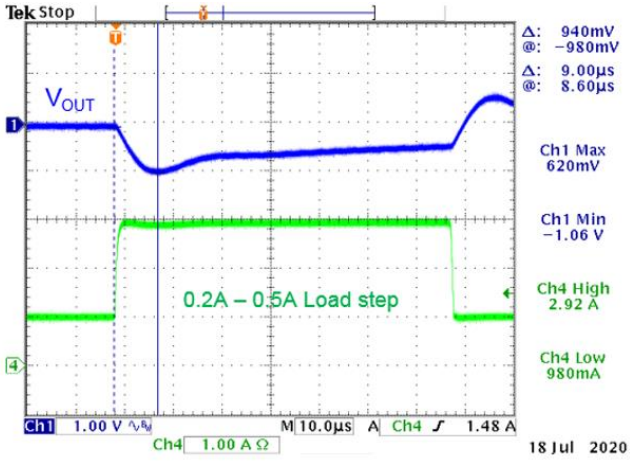


FIGURE 40

Vsag calculated value:0.88V; measured value: 1.0V

Response time = 9µsec. BW ≈ 0.3/9µsec = 33kHz

The step load shows a small ring, which points to lower phase margin. A gain-phase measurement (figure 41) shows this more clearly:

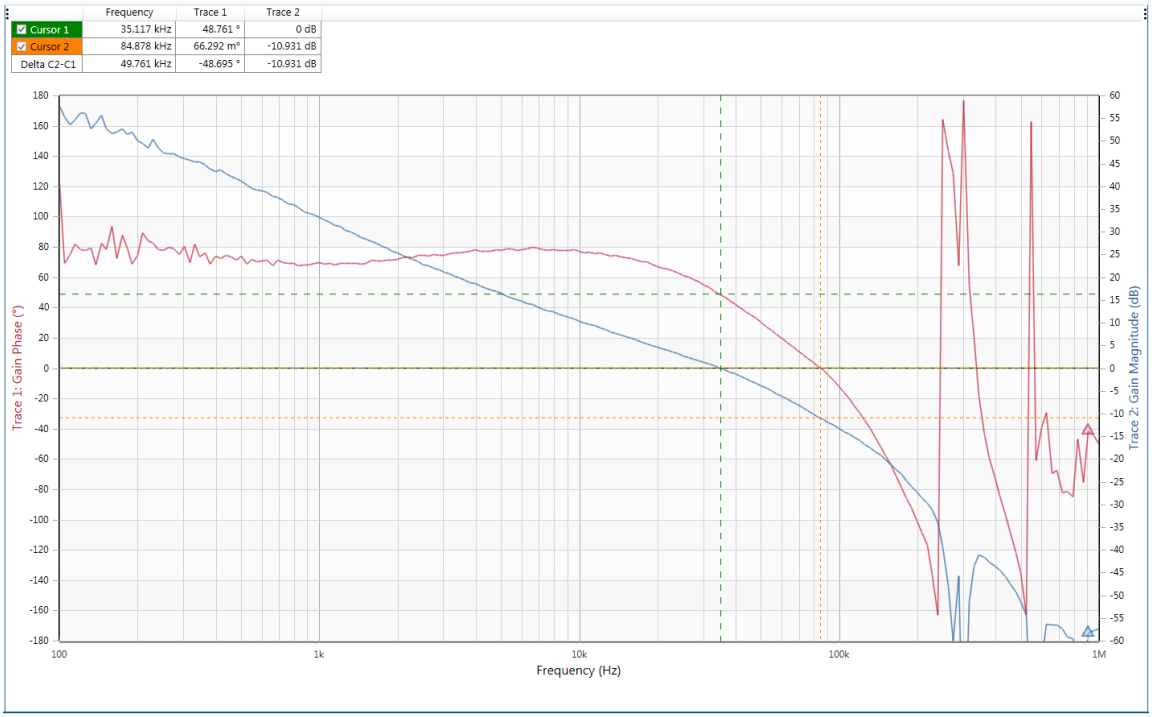


FIGURE 41

At V_{IN} = 48V, and 24V with 3A load, the bandwidth shows 35kHz and phase margin is 48dgs. Gain margin is 11dB.

But when measuring gain-phase at 1A load the phase margin became worse:

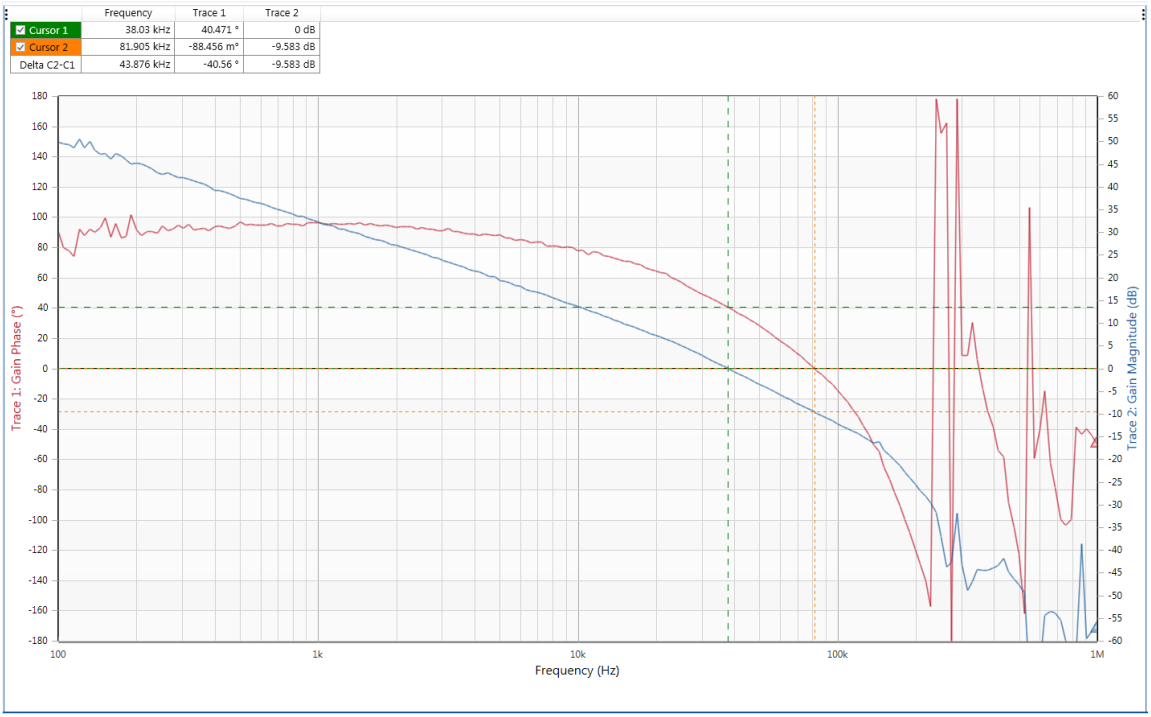


FIGURE 42

At V_{IN} = 48V, and 24V with 1A load, the bandwidth shows 38kHz and phase margin is 41dgs. Gain margin is 9.6dB.

This phase margin is not sufficient and should be improved. Adding a small feed-forward capacitor C_{FF} can boost the phase but it will also increase the bandwidth and lower the gain margin:
Figure 43 shows the gain-phase measurement result when 22pF C_{FF} is added in parallel with the upper feedback resistor.

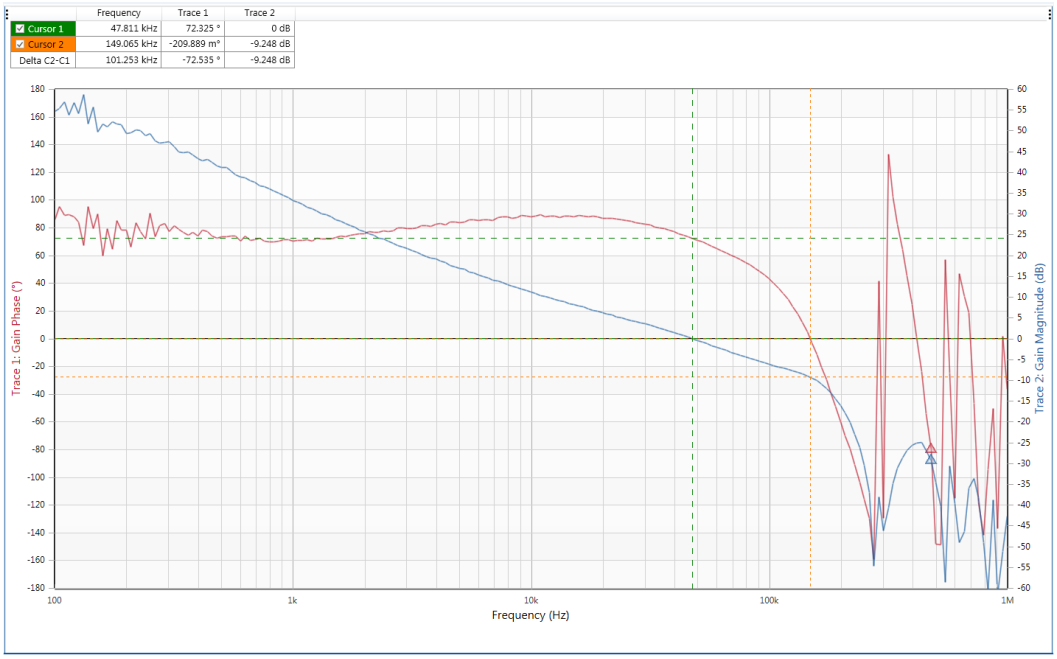


FIGURE 43

At V_{IN} = 48V, and 24V with 1A load and added 22pF C_{FF}, the bandwidth shows 48kHz and phase margin is 72dgs. But the Gain margin is only 9.2dB which is rather low.

A more stable design can be achieved by reducing the converter bandwidth; Figure 44 shows the gain-phase measurement when using a BW setting of 6% of the switching frequency. R_{COMP} = 7.5k, C_{COMP} = 12nF and C_{COMP2} = 100pF, and no C_{FF}.

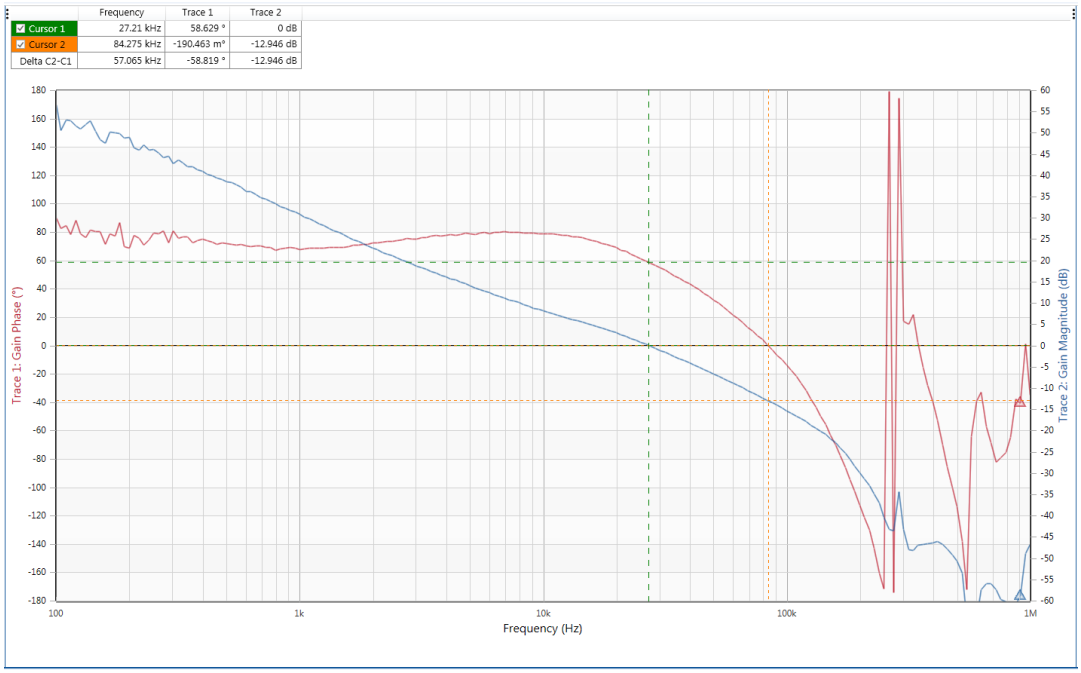
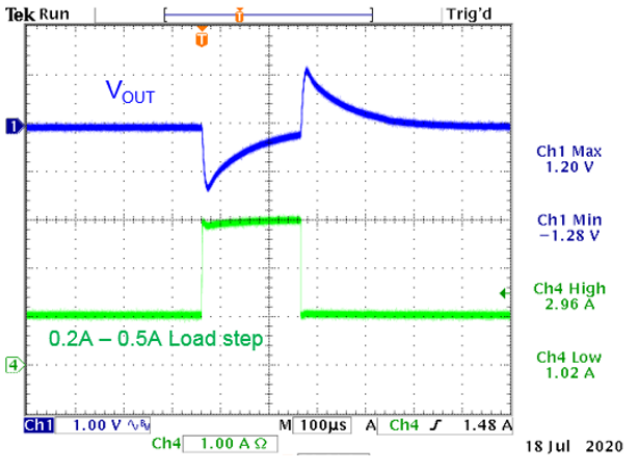


FIGURE 44

At V_{IN} = 48V, and 24V with 1A load and compensation for 6% BW setting, the bandwidth shows 27kHz and phase margin is 58dgs. Gain margin is 13dB. This is a more stable design.

Due to the lower bandwidth setting, the load step voltage sag will become larger, but the step load response is without ring.

V_{IN} = 48V, 0.2A ~ 0.5A fast load step



V_{IN} = 48V, 1A ~ 3A fast load step estimate bandwidth:

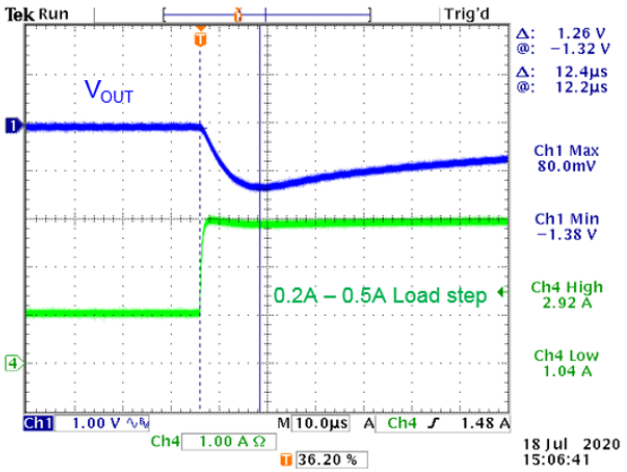


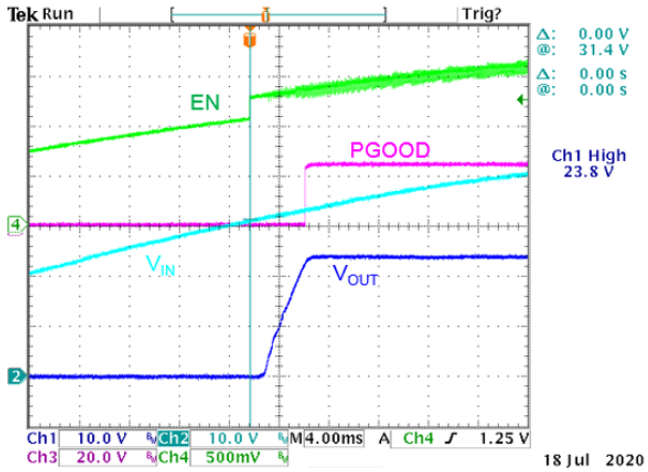
FIGURE 45

Calculated value:1.4V; measured value: 1.3V

Response time = 12.4µsec. BW ≈ 0.3/12.4µsec = 24kHz

The converter start-up from V_{IN} and Shut-down from V_{IN} were also measured. The small hysteresis step in the Enable signal can be seen when it passes the threshold. See figure 46.

Start-up at rising V_{IN}:



Shut-down at falling V_{IN}:

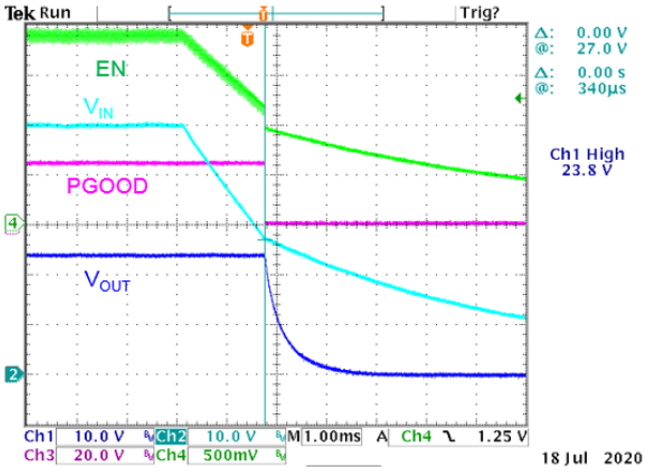


FIGURE 46

V_{START} calculated: 34V; V_{START} measured: 31.4V

V_{STOP} calculated: 27.2V; V_{STOP} measured: 27V

The converter efficiency and power loss was also measured, see figure 47.

RTQ6363V 24V application Fsw = 294kHz								
48V input	Vin	Iin	Vout	Iout	efficiency	Ploss	T-IC	T-Diode
48V-24V, 0.001A	48.4	0.002	24.23	0.001	29.3%	0.06		
48V-24V, 0.01A	48.4	0.011	24.13	0.01	45.7%	0.29		
48V-24V, 0.1A	48.3	0.057	24.13	0.1	88.0%	0.33		
48V-24V, 0.3A	48.3	0.165	24.13	0.3	91.1%	0.71		
48V-24V, 0.5A	48.2	0.269	24.12	0.5	93.1%	0.89		
48V-24V, 1A	48	0.527	24.11	1	95.3%	1.18	42°C	39°C
48V-24V, 2A	48.3	1.041	24.07	2	95.7%	2.14	55°C	51°C
48V-24V, 3A	48.3	1.569	24.05	3	95.2%	3.64	71°C	63°C

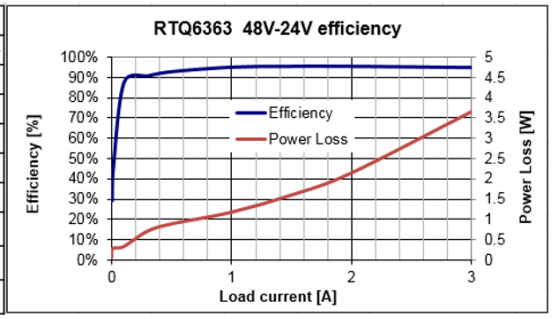


FIGURE 47

The total power loss at 3A load is 3.6W: Please note that the IC, Schottky diode and inductor all dissipate power so the heat is distributed as well. The IC however dissipates the majority of power and its thermal pad should be connected to sufficient copper on top layer and with thermal vias to inner layers and bottom layer.

5. SCHOTTKY DIODE SELECTION: REVERSE LEAKAGE CURRENT

In the original 48V – 24V/3A design, we had selected a special Trench type Schottky diode, which has greatly reduced reverse leakage current compared to standard Planar Schottky diodes [(1)]. With the Trench type Schottky diode, the power loss due to leakage is extremely small. To show the differences between these two types of diodes in this high power design, we will also test the Nexperia PMEG060V050EPDZ Planar Schottky diode. The reverse leakage current graphs of the Trench and Planar type Schottky diodes are shown in figure 48.

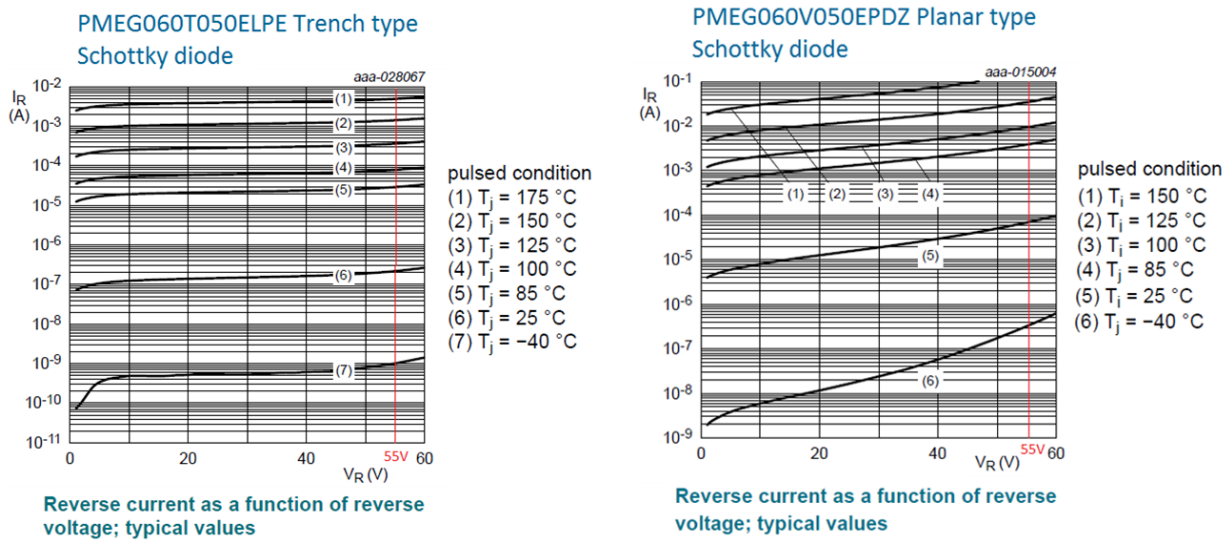


FIGURE 48

At maximum 55V input voltage and 100°C, the reverse leakage current is 80μA.

Reverse leakage Power loss = $D*V_{IN}*I_{LEAKAGE}$ = 0.5*55V*80μA = 2mW

At 125°C, the reverse leakage current is 350μA.

Reverse leakage Power loss = 0.5*55V*350μA = 10mW

At maximum 55V input voltage and 100°C, the reverse leakage current is 10mA.

Reverse leakage Power loss = $D*V_{IN}*I_{LEAKAGE}$ = 0.5*55V*10mA = 275mW

At 125°C, the reverse leakage current is 34mA. Reverse leakage Power loss = 0.5*55V*34mA = 0.935W

The calculations show that the reverse leakage current of a standard planar Schottky diodes can result in higher power loss in the diode at high temperatures.

This was verified by measurements: The two diodes were tested in the same 24V/3A application with 55V input, and the ambient temperature was gradually increased. Initially the Planar Schottky diode has slightly less power loss as its forward voltage is lower than the Trench type Schottky. But above 105°C, the power loss of the Planar Schottky increases rapidly, and at around 115°C it rises by itself and the diode fails at around 125°C due to excessive dissipation. See figure 49.

Schottky Diode:	PMEG060V050EPDZ					gradually increase T-ambient		
55V input	Vin	Iin	Vout	Iout	efficiency	Ploss	T-IC	T-Diode
55V-24V, 3A	55.1	1.377	24.020	3	95.0%	3.8127	72	71
55V-24V, 3A	55.1	1.378	23.940	3	94.6%	4.1078	105	98
55V-24V, 3A	55.1	1.382	23.940	3	94.3%	4.3282	113	106
55V-24V, 3A	55.1	1.394	23.940	3	93.5%	4.9894	116	116
55V-24V, 3A	55.1	1.412	23.940	3	92.3%	5.9812	120	126
Schottky Diode:	PMEG060T050ELP					gradually increase T-ambient		
55V input	Vin	Iin	Vout	Iout	efficiency	Ploss	T-IC	T-Diode
55V-24V, 3A	55.3	1.3735	24.020	3	94.9%	3.89455	75	71
55V-24V, 3A	55.3	1.3736	23.940	3	94.5%	4.14008	108	93
55V-24V, 3A	55.3	1.37375	23.910	3	94.4%	4.238375	110	100
55V-24V, 3A	55.3	1.3732	23.880	3	94.3%	4.29796	118	109
55V-24V, 3A	55.3	1.3732	23.870	3	94.3%	4.32796	130	125

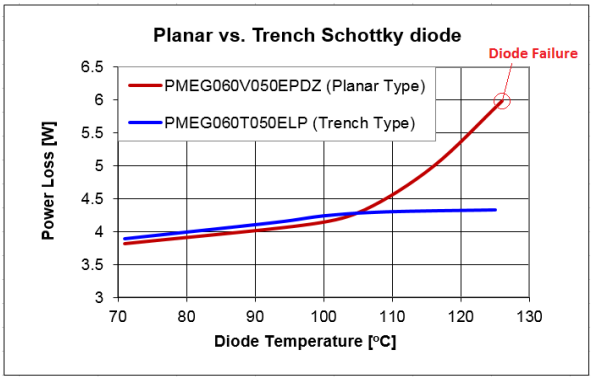


FIGURE 49

This example shows that Schottky diode reverse leakage current can be a critical parameter for application reliability.

6. CONCLUSION

The RTQ29xx/RTQ63xx family can be used successfully in a wide range of step-down converter applications. The RTQ29xx and RTQ63xx excel design tool makes it easy to calculate the external components, and the measured performance matches the calculated values quite well. It is recommended to check the stability by means of gain-phase analysis although a fast step load test can also be used to quickly check stability aspects. For higher duty-cycle and high input voltage applications, the Schottky diode capacitance, and reverse leakage current are important parameters that must be considered.

References:

(1)Benchmarking of a Novel SiGe Diode Technology for the Usage in High Frequency 48V/12V Converter applications by A. Aneissi, M.Meissner, K.F. Hoffmann, R. Behtash, J. Fisher, S. Fahlbusch

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