

1.5A, 24V, 1.4MHz Step-Down Converter

General Description

The RT8259A is a monolithic step-down switch mode converter with a built-in power MOSFET. It achieves 1.5A output current over a wide input supply range with excellent load and line regulation. Current Mode operation provides fast transient response and eases loop stabilization. The chip also provides protection functions such as cycle-by-cycle current limiting and thermal shutdown protection.

Ordering Information

RT8259A □ □

- Package Type
S : SOP-8
- Lead Plating System
G : Green (Halogen Free and Pb Free)

Note :

Richtek products are :

- ▶ RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- ▶ Suitable for use in SnPb or Pb-free soldering processes.

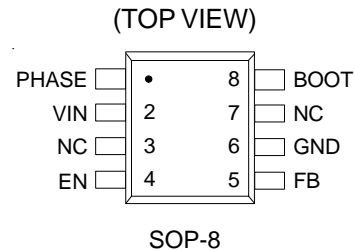
Features

- 1.5A Output Current
- 0.3Ω Internal Power MOSFET Switch
- Stable with Low ESR Output Ceramic Capacitors
- Up to 92% Efficiency
- Fixed 1.4MHz Frequency
- Thermal Shutdown
- Cycle-By-Cycle Over Current Protection
- Wide 4.5V to 24V Operating Input Range
- Output Adjustable from 0.8V to 15V
- Available in SOP-8 Package
- RoHS Compliant and Halogen Free

Applications

- Distributed Power Systems
- Battery Charger
- Pre-Regulator for Linear Regulators
- WLED Drivers

Pin Configurations



Typical Application Circuit

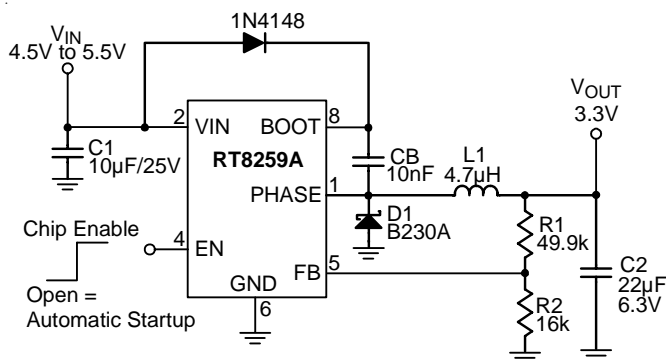


Figure 1. Input Voltage 4.5V to 5.5V

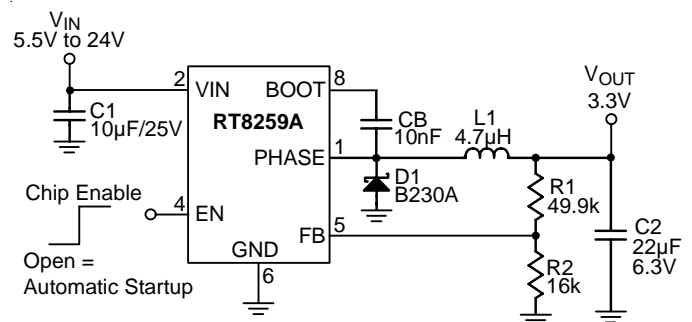


Figure 2. Input Voltage 5.5V to 24V

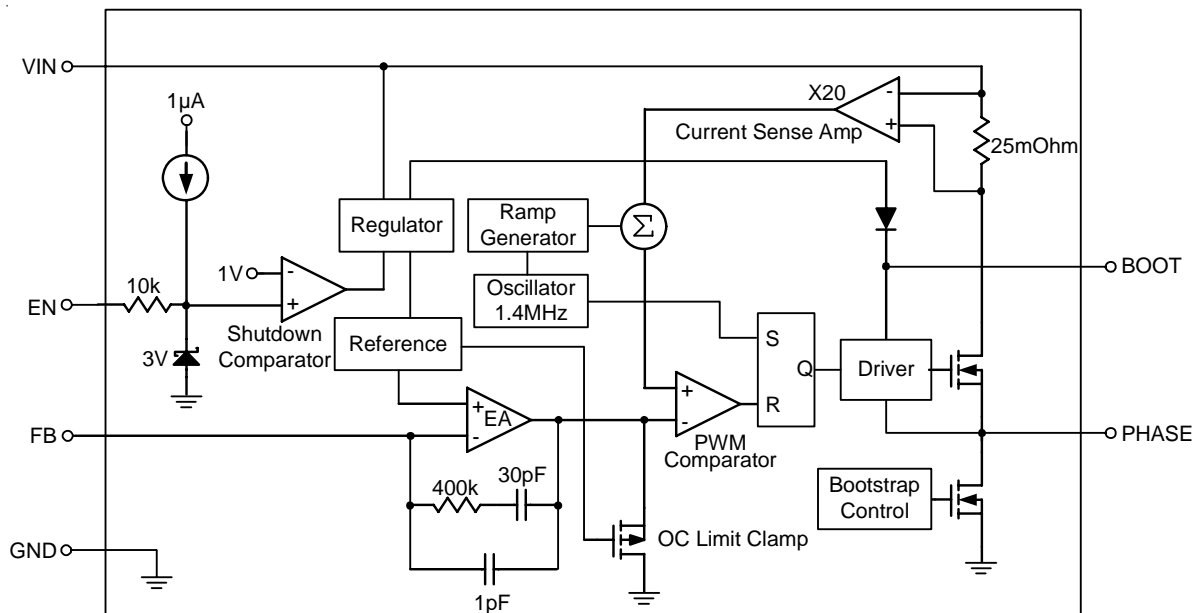
Recommended Component Selection

V _{OUT}	1.2V	1.8V	2.5V	3.3V	5V	8V	10V	15V
L1 (μH)	2	2	3.6	4.7	6.8	10	10	15
R2 (kΩ)	100	39	24	16	8.2	5.23	4.42	2.61
R1 (kΩ)	49.9	48.7	51	49.9	43	47	51	46.4

Functional Pin Description

Pin No.	Pin Name	Pin Function
1	PHASE	Switch Output.
2	VIN	Supply Voltage. The RT8259 operates from a 4.5V to 24V unregulated input. C1 is needed to prevent large voltage spikes from appearing at the input.
3, 7	NC	No Internal connection.
4	EN	Chip Enable (Active High). If the EN pin is open, it will be pulled to high by internal circuit.
5	FB	Feedback. An external resistor divider from the output to GND, tapped to the FB pins sets the output voltage.
6	GND	Ground. This pin is the voltage reference for the regulated output voltage. For this reason, care must be taken in its layout. This node should be placed outside of the D1 to C1 ground path to prevent switching current spikes from inducing voltage noise into the part.
8	BOOT	Bootstrap. A capacitor is connected between PHASE and BOOT pins to form a floating supply across the power switch driver. This capacitor is needed to drive the power switch's gate above the supply voltage.

Function Block Diagram



Absolute Maximum Ratings (Note 1)

- Supply Voltage, V_{IN} ----- 26V
- PHASE Voltage ----- $-0.3V$ to $(V_{IN} + 0.3V)$
- BOOT Voltage ----- $V_{PHASE} + 6V$
- All Other Pins ----- 0.3V to 6V
- Output Voltage ----- $-0.3V$ to 15V
- Power Dissipation, P_D @ $T_A = 25^\circ C$
 - SOP-8 ----- 0.833W
- Package Thermal Resistance (Note 2)
 - SOP-8, θ_{JA} ----- $120^\circ C/W$
- Junction Temperature ----- $150^\circ C$
- Lead Temperature (Soldering, 10 sec.) ----- $260^\circ C$
- Storage Temperature Range ----- $-65^\circ C$ to $150^\circ C$
- ESD Susceptibility (Note 3)
 - HBM (Human Body Mode) ----- 2kV
 - MM (Machine Mode) ----- 200V

Recommended Operating Conditions (Note 4)

- Supply Voltage, V_{IN} ----- 4.5V to 24V
- Output Voltage, V_{OUT} ----- 0.8V to 15V
- EN Voltage, V_{EN} ----- 0V to 5.5V
- Junction Temperature Range ----- $-40^\circ C$ to $125^\circ C$
- Ambient Temperature Range ----- $-40^\circ C$ to $85^\circ C$

Electrical Characteristics

($V_{IN} = 12V$, $T_A = 25^\circ C$ unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Feedback Voltage	V_{FB}	$4.5V \leq V_{IN} \leq 24V$	0.784	0.8	0.816	V
Feedback Current	I_{FB}	$V_{FB} = 0.8V$	--	0.1	0.3	μA
Switch On Resistance	$R_{DS(ON)}$		--	0.3	--	Ω
Switch Leakage		$V_{EN} = 0V$, $V_{SW} = 0V$	--	--	10	μA
Current Limit	I_{LIM}	$V_{BOOT} - V_{PHASE} = 4.5V$	1.8	2.4	--	A
Oscillator Frequency	f_{SW}		1.2	1.4	1.6	MHz
Maximum Duty Cycle			--	80	--	%
Minimum On-Time	t_{ON}		--	100	--	ns
Under Voltage Lockout Threshold		Rising	3.9	4.2	4.5	V
Under Voltage Lockout Threshold Hysteresis			--	200	--	mV
EN Input Low Voltage			--	--	0.4	V
EN Input High Voltage			1.4	--	5.5	V
EN Pull Up Current			--	1	--	μA

To be continued

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Shutdown Current	I_{SHDN}	$V_{EN} = 0V$	--	25	--	μA
Quiescent Current	I_Q	$V_{EN} = 2V, V_{FB} = 1V$ (Not Switching)	--	0.55	1	mA
Thermal Shutdown	T_{SD}		--	150	--	$^{\circ}C$

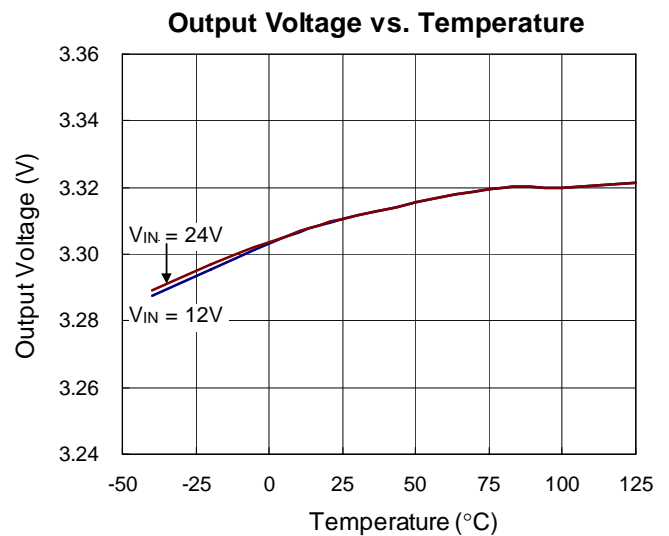
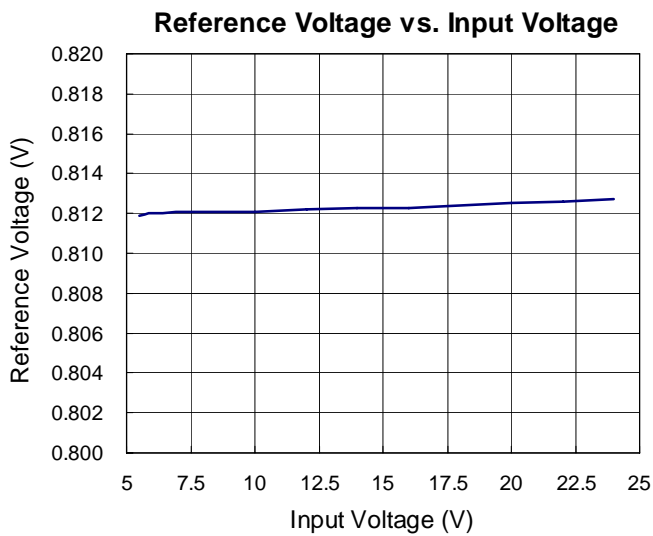
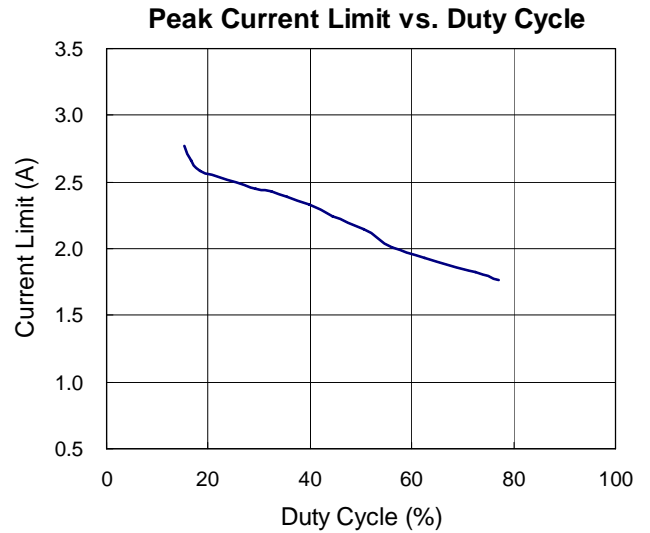
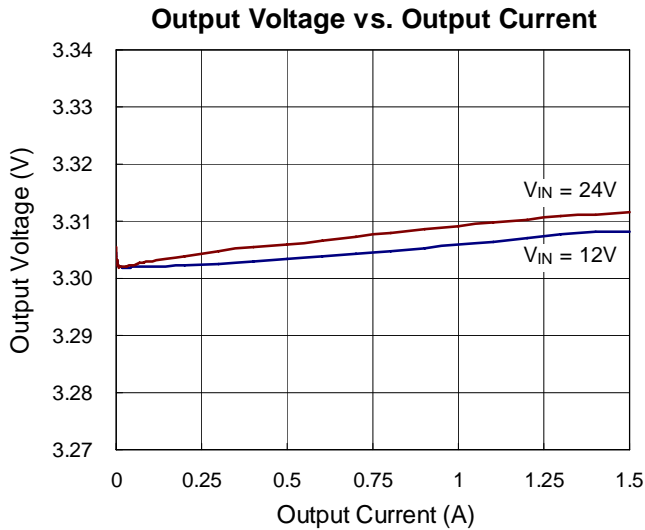
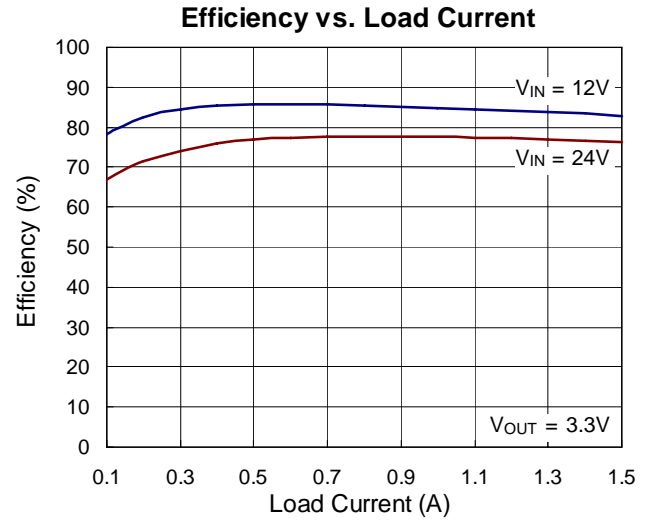
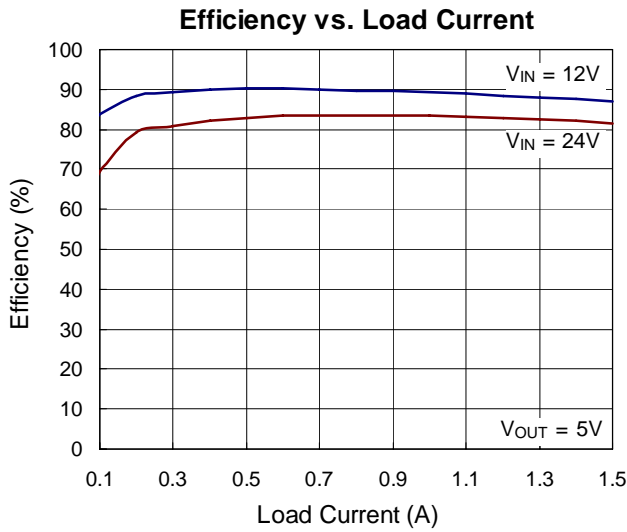
Note 1. Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2. θ_{JA} is measured in the natural convection at $T_A = 25^{\circ}C$ on a high effective four layers thermal conductivity test board of JEDEC 51-7 thermal measurement standard.

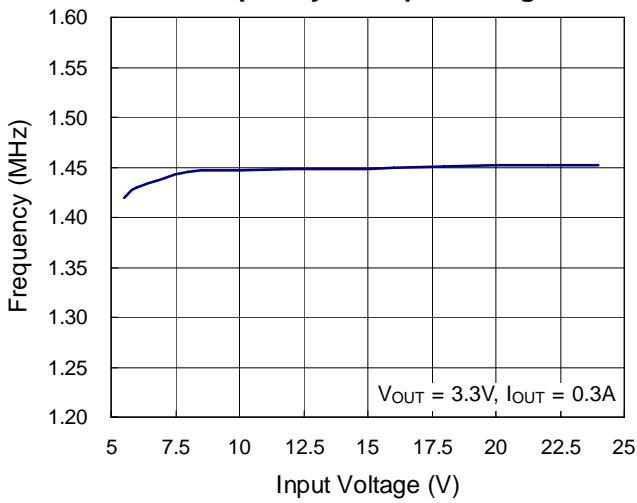
Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

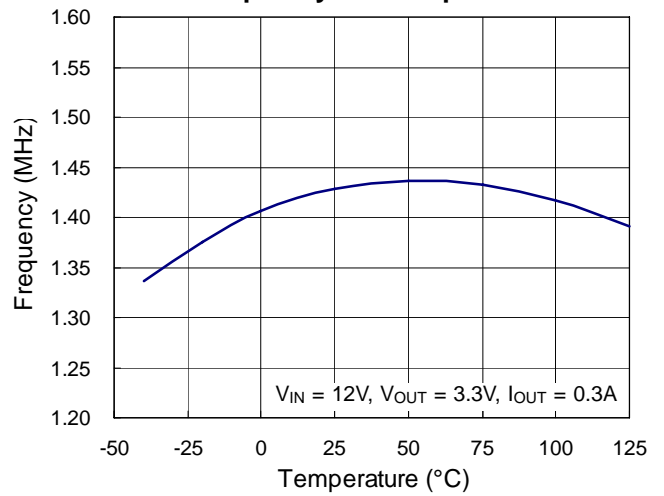
Typical Operating Characteristics



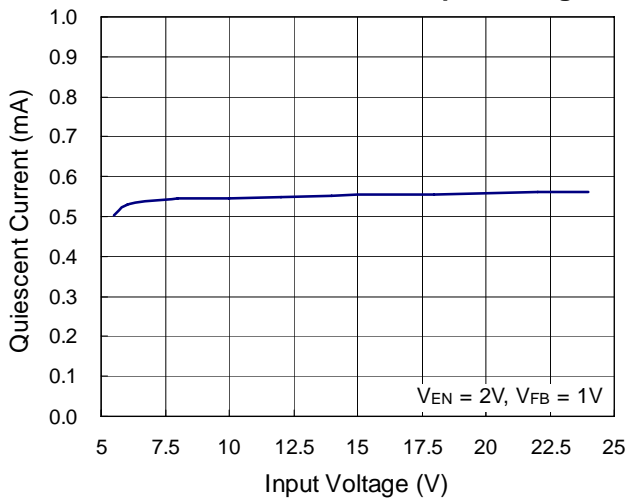
Frequency vs. Input Voltage



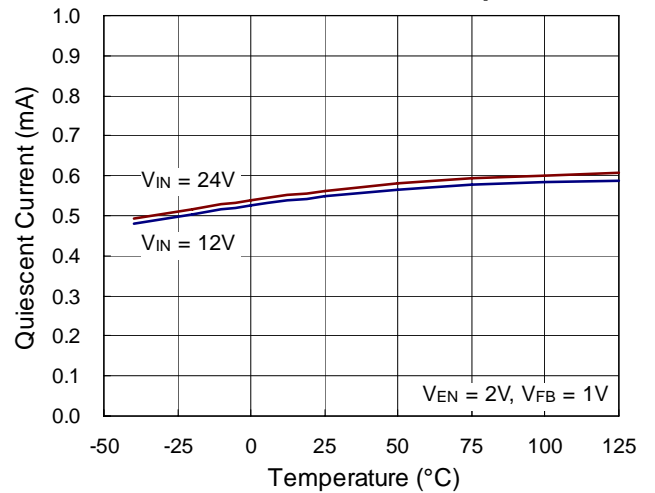
Frequency vs. Temperature



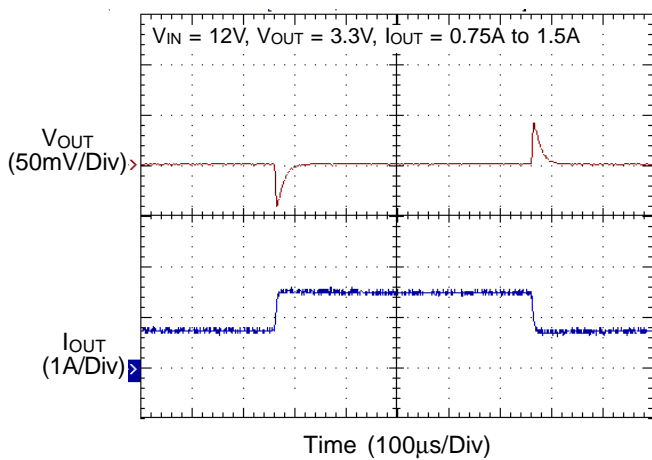
Quiescent Current vs. Input Voltage



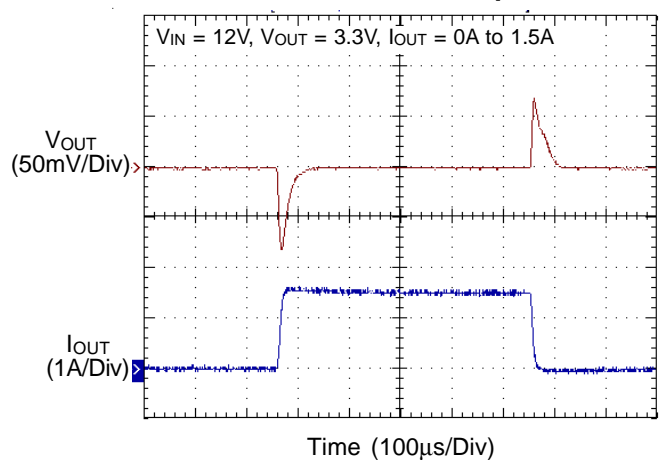
Quiescent Current vs. Temperature



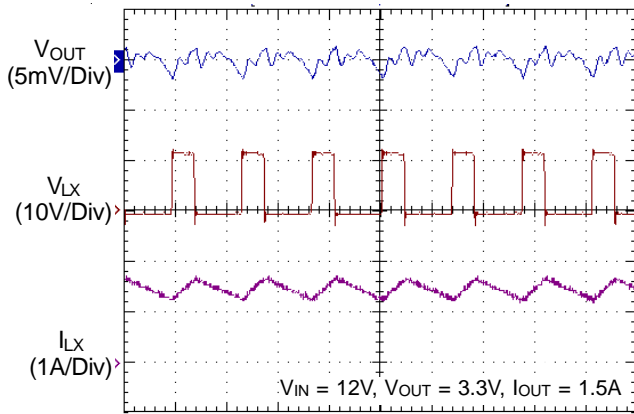
Load Transient Response



Load Transient Response

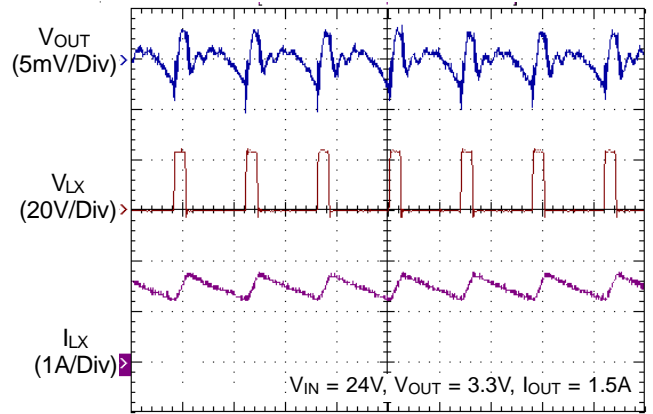


Output Ripple



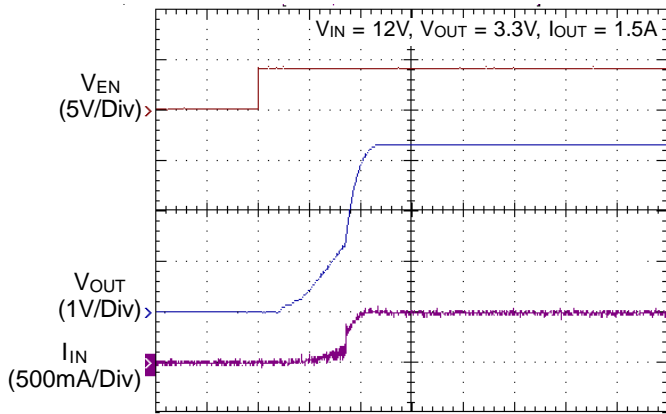
Time (500ns/Div)

Output Ripple



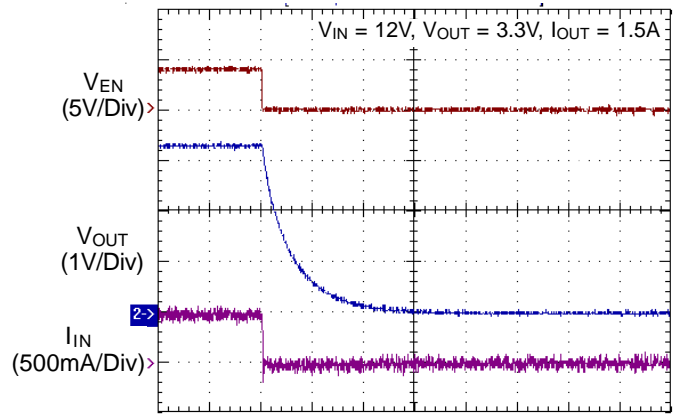
Time (500ns/Div)

Power On from EN



Time (250 μ s/Div)

Power Off from EN



Time (100 μ s/Div)

Application Information

The Typical Application Circuit shows the basic RT8259A application circuit. External component selection is determined by the maximum load current and begins with the selection of the inductor value and operating frequency followed by C_{IN} and C_{OUT} .

Inductor Selection

The inductor value and operating frequency determine the ripple current according to a specific input and output voltage. The ripple current ΔI_L increases with higher V_{IN} and decreases with higher inductance.

$$\Delta I_L = \left[\frac{V_{OUT}}{f \times L} \right] \times \left[1 - \frac{V_{OUT}}{V_{IN}} \right]$$

Having a lower ripple current reduces not only the ESR losses in the output capacitors but also the output voltage ripple. High frequency with small ripple current can achieve highest efficiency operation. However, it requires a large inductor to achieve this goal.

For the ripple current selection, the value of $\Delta I_L = 0.4(I_{MAX})$ will be a reasonable starting point. The largest ripple current occurs at the highest V_{IN} . To guarantee that the ripple current stays below the specified maximum, the inductor value should be chosen according to the following equation :

$$L = \left[\frac{V_{OUT}}{f \times \Delta I_L(MAX)} \right] \times \left[1 - \frac{V_{OUT}}{V_{IN(MAX)}} \right]$$

Inductor Core Selection

The inductor type must be selected once the value for L is known. Generally speaking, high efficiency converters can not afford the core loss found in low cost powdered iron cores. So, the more expensive ferrite or mollypermalloy cores will be a better choice.

The selected inductance rather than the core size for a fixed inductor value is the key for actual core loss. As the inductance increases, core losses decrease. Unfortunately, increase of the inductance requires more turns of wire and therefore the copper losses will increase.

Ferrite designs are preferred at high switching frequency due to the characteristics of very low core losses. So, design goals can focus on the reduction of copper loss and the saturation prevention.

Ferrite core material saturates "hard", which means that inductance collapses abruptly when the peak design current is exceeded. The previous situation results in an abrupt increase in inductor ripple current and consequent output voltage ripple.

Do not allow the core to saturate!

Different core materials and shapes will change the size/current and price/current relationship of an inductor.

Toroid or shielded pot cores in ferrite or permalloy materials are small and do not radiate energy. However, they are usually more expensive than the similar powdered iron inductors. The rule for inductor choice mainly depends on the price vs. size requirement and any radiated field/EMI requirements.

C_{IN} and C_{OUT} Selection

The input capacitance, C_{IN} , is needed to filter the trapezoidal current at the source of the top MOSFET. To prevent large ripple current, a low ESR input capacitor sized for the maximum RMS current should be used. The RMS current is given by :

$$I_{RMS} = I_{OUT(MAX)} \frac{V_{OUT}}{V_{IN}} \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief.

Choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet size or height requirements in the design.

The selection of C_{OUT} is determined by the required Effective Series Resistance (ESR) to minimize voltage ripple.

Moreover, the amount of bulk capacitance is also a key for C_{OUT} selection to ensure that the control loop is stable. Loop stability can be checked by viewing the load transient response as described in a later section.

The output ripple, ΔV_{OUT} , is determined by :

$$\Delta V_{OUT} \leq \Delta I_L \left[ESR + \frac{1}{8fC_{OUT}} \right]$$

The output ripple will be highest at maximum input voltage since ΔI_L increases with input voltage. Multiple capacitors placed in parallel may be needed to meet the ESR and

RMS current handling requirement. Dry tantalum, special polymer, aluminum electrolytic and ceramic capacitors are all available in surface mount packages. Special polymer capacitors offer very low ESR value. However, it provides lower capacitance density than other types. Although Tantalum capacitors have the highest capacitance density, it is important to only use types that pass the surge test for use in switching power supplies. Aluminum electrolytic capacitors have significantly higher ESR. However, it can be used in cost-sensitive applications for ripple current rating and long term reliability considerations. Ceramic capacitors have excellent low ESR characteristics but can have a high voltage coefficient and audible piezoelectric effects. The high Q of ceramic capacitors with trace inductance can also lead to significant ringing.

Higher values, lower cost ceramic capacitors are now becoming available in smaller case sizes. Their high ripple current, high voltage rating and low ESR make them ideal for switching regulator applications. However, care must be taken when these capacitors are used at input and output. When a ceramic capacitor is used at the input and the power is supplied by a wall adapter through long wires, a load step at the output can induce ringing at the input, V_{IN} . At best, this ringing can couple to the output and be mistaken as loop instability. At worst, a sudden inrush of current through the long wires can potentially cause a voltage spike at V_{IN} large enough to damage the part.

External Bootstrap Diode

When the operating input voltage is lower than 5.5V, it is recommended to add an external bootstrap diode for efficiency improvement. The bootstrap diode can be a low cost one such as IN4148 or BAT54. For higher operating input voltage between 5.5V and 24V, the external diode must be removed.

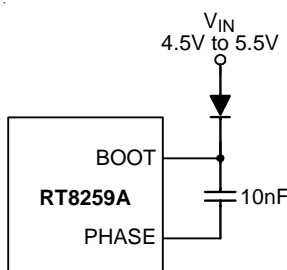


Figure 3

Output Voltage Setting

The resistive divider allows the FB pin to sense a fraction of the output voltage as shown in Figure 4.

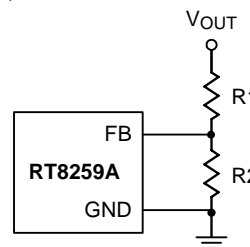


Figure 4. Setting the Output Voltage

For adjustable voltage mode, the output voltage is set by an external resistive divider according to the following equation :

$$V_{OUT} = V_{REF} \left(1 + \frac{R1}{R2} \right)$$

Where V_{REF} is the internal reference voltage (0.8V typ.).

Checking Transient Response

The regulator loop response can be checked by looking at the load transient response. Switching regulators take several cycles to respond to a step in load current. When a load step occurs, V_{OUT} immediately shifts by an amount equal to ΔI_{LOAD} (ESR) also begins to charge or discharge C_{OUT} generating a feedback error signal for the regulator to return V_{OUT} to its steady-state value. During this recovery time, V_{OUT} can be monitored for overshoot or ringing that would indicate a stability problem.

Thermal Considerations

For continuous operation, do not exceed the maximum operation junction temperature 125°C. The maximum power dissipation depends on the thermal resistance of IC package, PCB layout, the rate of surroundings airflow and temperature difference between junction to ambient. The maximum power dissipation can be calculated by following formula :

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

where $T_{J(MAX)}$ is the maximum operation junction temperature 125°C, T_A is the ambient temperature and the θ_{JA} is the junction to ambient thermal resistance.

For recommended operating conditions specification of RT8259A, where $T_{J(MAX)}$ is the maximum junction temperature of the die (125°C) and T_A is the maximum

ambient temperature. The junction to ambient thermal resistance θ_{JA} is layout dependent. For SOP-8 package, the thermal resistance θ_{JA} is 120°C/W on standard JEDEC 51-7 four-layers thermal test board. The maximum power dissipation at $T_A = 25^\circ\text{C}$ can be calculated by following formula :

$$P_{D(MAX)} = (125^\circ\text{C} - 25^\circ\text{C}) / 120^\circ\text{C/W} = 0.833\text{W (SOP-8)}$$

The maximum power dissipation depends on operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance θ_{JA} . For RT8259A packages, the Figure 5 of derating curves allows the designer to see the effect of rising ambient temperature on the maximum power allowed.

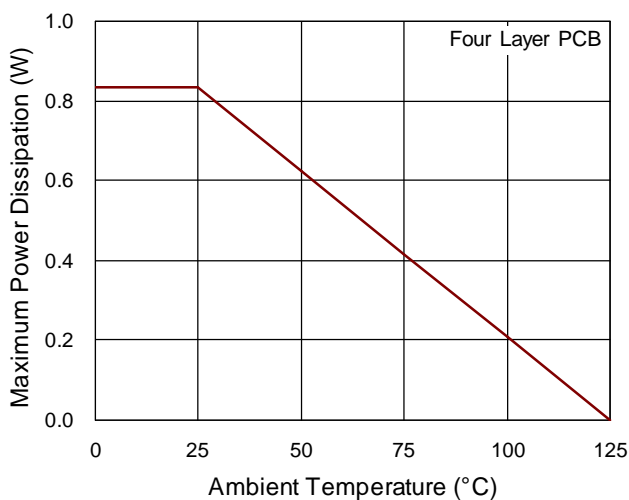


Figure 5. Derating Curves for RT8259A Packages

Layout Consideration

Follow the PCB layout guidelines for optimal performance of RT8259A

- } Keep the traces of the main current paths as short and wide as possible.
- } Put the input capacitor as close as possible to the device pins (VIN and GND).
- } LX node is with high frequency voltage swing and should be kept small area. Keep analog components away from LX node to prevent stray capacitive noise pick-up.
- } Connect feedback network behind the output capacitors. Keep the loop area small. Place the feedback components near the RT8259A.
- } Connect all analog grounds to a common node and then connect the common node to the power ground behind the output capacitors.
- } An example of PCB layout guide is shown in Figure 6 for reference.

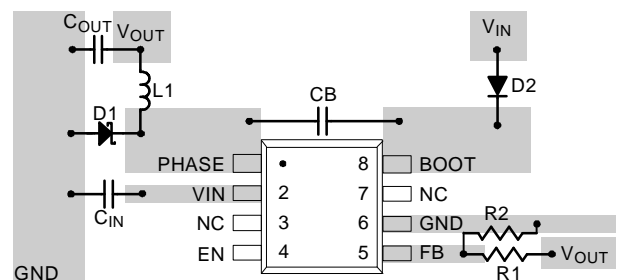


Figure 6

Table 1. Suggested Inductors for L1

Component Supplier	Series	Inductance (mH)	DCR (mW)	Current Rating (A)	Dimensions (mm)
TDK	SLF7045	4.7	30	2	7x7x4.5
TAIYO YUDEN	NR8040	4.7	18	4.7	8x8x4
GOTERND	GTSD53	4.7	45	1.87	5x5x2.8
GOTERND	GSSR2	4.7	18	5.7	10x10x3.8

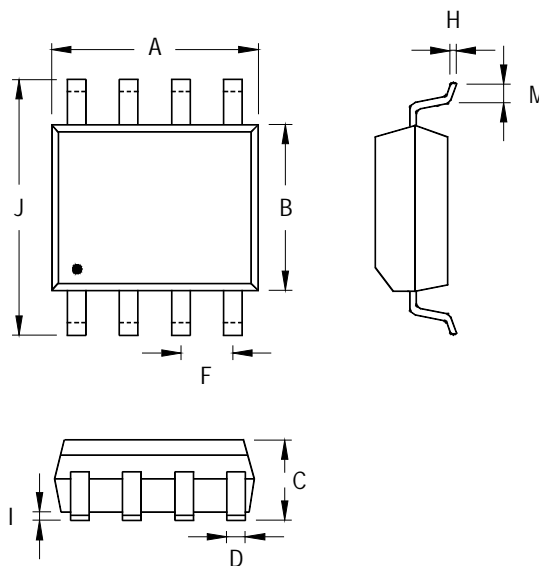
Table 2. Suggested Capacitors for CIN and COUT

Component Supplier	Part No.	Capacitance (mF)	Case Size
MURATA	GRM31CR61E106K	10	1206
TDK	C3225X5R1E106K	10	1206
TAIYO YUDEN	TMK316BJ106ML	10	1206
MURATA	GRM31CR61C226M	22	1206
TDK	C3225X5R1C226M	22	1206
TAIYO YUDEN	EMK316BJ226ML	22	1206

Table 3. Suggested Diode for D1

Component Supplier	Series	V_{RRM} (V)	I_{OUT} (A)	Package
DIODES	B230A	30	2	DO-214AC
DIODES	B330A	30	3	DO-214AC
PANJIT	SK23	30	2	DO-214AC
PANJIT	SK33	30	3	DO-214AB

Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	4.801	5.004	0.189	0.197
B	3.810	3.988	0.150	0.157
C	1.346	1.753	0.053	0.069
D	0.330	0.508	0.013	0.020
F	1.194	1.346	0.047	0.053
H	0.170	0.254	0.007	0.010
I	0.050	0.254	0.002	0.010
J	5.791	6.200	0.228	0.244
M	0.400	1.270	0.016	0.050

8-Lead SOP Plastic Package

Richtek Technology Corporation

Headquarter
 5F, No. 20, Taiyuen Street, Chupei City
 Hsinchu, Taiwan, R.O.C.
 Tel: (8863)5526789 Fax: (8863)5526611

Richtek Technology Corporation

Taipei Office (Marketing)
 5F, No. 95, Minchiuan Road, Hsintien City
 Taipei County, Taiwan, R.O.C.
 Tel: (8862)86672399 Fax: (8862)86672377
 Email: marketing@richtek.com

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