Wide Input and Ultra-Low Quiescent Current Boost Converter with High Efficiency

General Description

The RT4823 integrates built-in power transistors, synchronous rectification, and low supply current to provide a compact solution for systems using advanced Li-Ion battery chemistries. The RT4823 is capable of supplying significant energy when the battery voltage is lower than the required voltage for system power ICs.

The RT4823 is a boost regulator designed to provide a minimum output voltage from a single-cell Li-Ion battery, even when the battery voltage is below system minimum. In boost mode, output voltage regulation is guaranteed to a maximum load current of 1500mA. Quiescent current in shutdown mode is less than 1μA, which maximizes the battery life. The regulator transitions smoothly between bypass and normal boost mode. The device can be forced into bypass mode to reduce quiescent current.

The RT4823 is available in the WL-CSP-9B 1.3x1.2 (BSC) package.

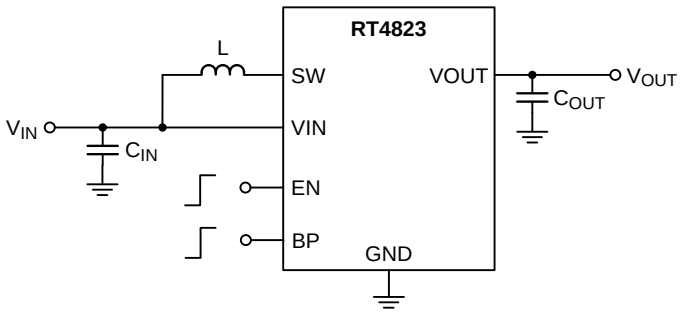
Applications

- NFC Device Power Supply
- USB Charging Ports
- PC Accessory Application (Keyboard, Mouse...etc.)
- TWS (True Wireless Stereo) Hall Sensor
- Gaming Device Sensor

Features

- **Ultra-Low Operating Quiescent Current**
- **Quickly Start-Up Time (< 400μsec)**
- **3 Few External Components : 1μH Inductor, 0402 Case Size Input and 0603 Case Size Output Case Size Capacitors**
- **Input Voltage Range : 1.8V to 5.5V**
- **Support V_{IN} > V_{OUT} Operation**
- **Default Boost Output Voltage Setting : V_{OUT} = 5V**
- **Maximum Continuous Load Current : 1.3A at V_{IN} > 3.6V Boosting V_{OUT} to 5V**
- **Up to 93% Efficiency**
- **EN(H) : Boost Mode**
- **EN(L), BP(H) : Bypass Mode**
- **EN(L), BP(L) : Shutdown Mode**
- **Internal Synchronous Rectifier**
- **Over-Current Protection**
- **Cycle-by-Cycle Current Limit**
- **Over-Voltage Protection**
- **Short-Circuit Protection**
- **Over-Temperature Protection**
- **Small WL-CSP-9B 1.3x1.2 (BSC) Package**

Simplified Application Circuit



Copyright © 2022 Richtek Technology Corporation. All rights reserved. RICHTEK is a registered trademark of Richtek Technology Corporation.

Ordering Information

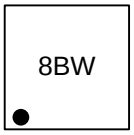
RT4823 □
└Package Type
WSC : WL-CSP-9B 1.3x1.2 (BSC)

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

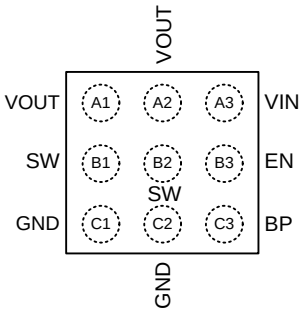
Marking Information



8B : Product Code
W : Date Code

Pin Configuration

(TOP VIEW)



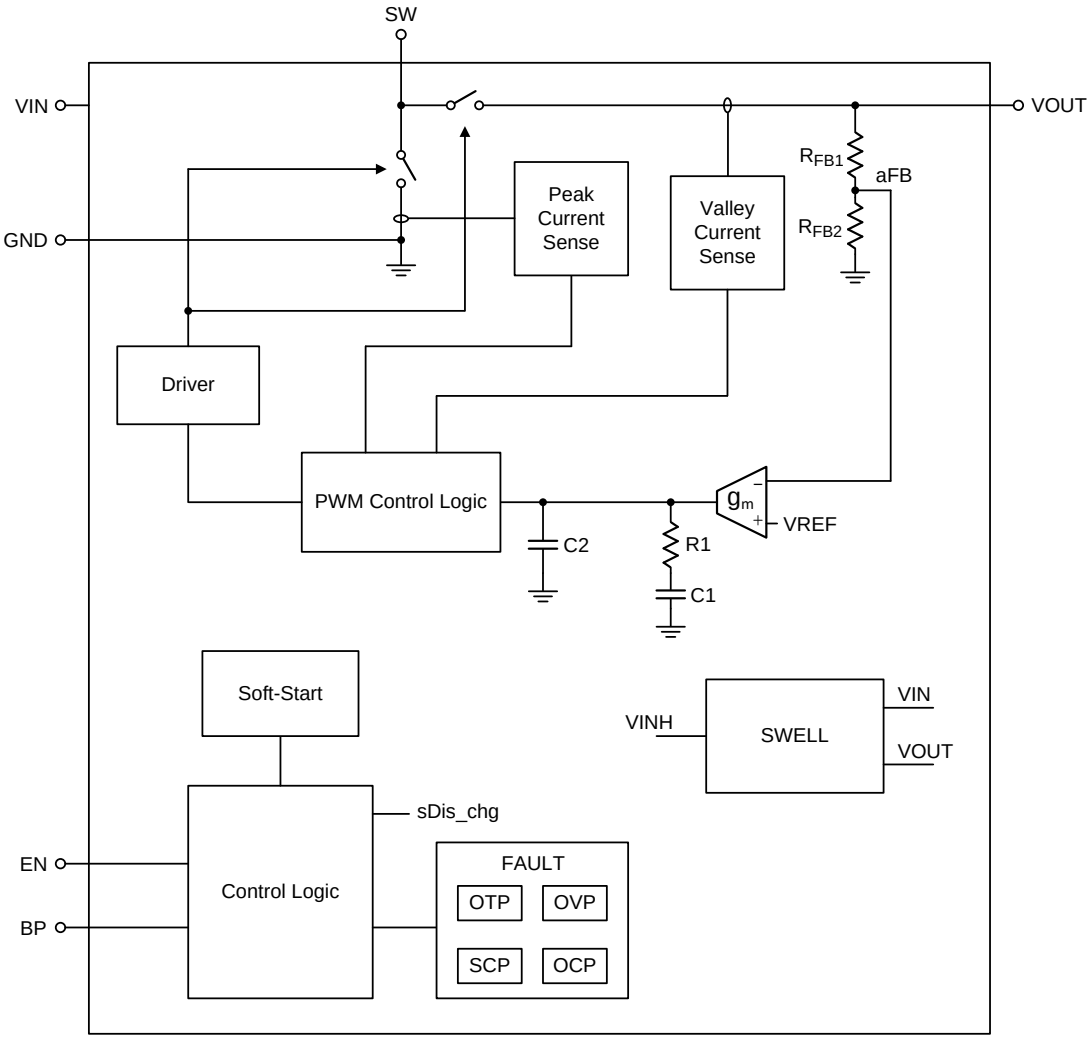
WL-CSP-9B 1.3x1.2 (BSC)

Functional Pin Description

Pin No.	Pin Name	Pin Function
A1, A2	VOUT	Output voltage. Place C_{OUT} as close as possible to the device.
A3	VIN	Input voltage. This pin has to connect to input power to supply chip internal power.
B1, B2	SW	Switching node. The power inductor should be connected between SW and power input.
B3	EN	Enable. When this pin is set to HIGH, the circuit is enabled. Do not leave this pin floating.
C1, C2	GND	Ground. This is the power and signal ground reference for the chip. The C_{OUT} bypass capacitor should be returned with the shortest path possible to these pins.
C3	BP	Bypass mode. This pin is used to control the converter into bypass mode. (Detailed configuration is shown in Table 1.)

Copyright © 2022 Richtek Technology Corporation. All rights reserved. RICHTEK is a registered trademark of Richtek Technology Corporation.

Functional Block Diagram



Operation

The RT4823 combines built-in power transistors, synchronous rectification, and low supply current, and it provides a compact solution for system using advanced Li-Ion battery chemistries.

In boost mode, output voltage regulation is guaranteed to maximum load current of 1.5A. Quiescent current in Shutdown mode is less than 1μA, which maximizes the battery life.

Power-On Reset

If input voltage is lower than POR, the internal digital and analog circuit are disabled. If input voltage is higher than POR, the Boost converter behavior is shown as follows :

1. IC Digital circuit will be activated.
2. Internal register will be loaded in default value.
3. Boost converter will enter free-running mode (detailed information is shown in free-running mode section).
4. If V_{OUT} > 2.2V (or V_{IN} > 2.2V), Boost converter will enter closed loop control and load in E-fuse value to the internal register.

Copyright © 2022 Richtek Technology Corporation. All rights reserved. RICHTEK is a registered trademark of Richtek Technology Corporation.

Free-Running Mode

If both voltages of V_{IN} and V_{OUT} are lower than 2.2V, the Boost converter will into free-running mode. In this mode, switching frequency operation is 1.5MHz and duty cycle of Boost converter is 25%. It is translation of power-on stage, and there is implemented current limit function for converter soft-start. The current limit level should be lower than 900mA.

EN and BP

As Table 1 shows, there are three device states in the RT4823. When EN and BP pull low, it is shutdown mode, and the quiescent current is less than 1μA. If EN pulls high (BP do not care), the RT4823 is in boost mode and it is with low quiescent operation. If BP pulls high and EN pulls low, the RT4823 is in bypass mode. There should be a delay time (< 250μs) from EN pull-high to power ready, to guarantee normal operation.

Table 1. Pin Configuration for Converter

EN Input	BP Input	Mode Define	Device State
0	0	Shutdown Mode	The device is shut down. The device shutdown current is approximately 1μA (max).
1	Do not care	Boost Mode	The device is active in Boost PFM low quiescent mode. The supply current is approximately 4μA (typ.).
0	1	Bypass Mode	The device is in forced bypass mode.

Enable

The boost can be enabled or disabled by the EN pin. When the EN pin is higher than the threshold of logic-high, the device starts operating as shown in Figure 1 operation diagram. In shutdown mode, the converter stops switching, and the internal control circuit is turned off. The output voltage is discharged by component consumption (such as Cap ESR) since there is no discharge function in this state.

Soft-Start State

During soft-start state, if VOUT reaches 99% V_{OUT_Target}, the RT4823 will enter boost operation. When system powers on with heavy loading (higher than pre-charge current), the RT4823 is in pre-charge state until loading release.

Boost/Auto Bypass Mode

There are two normal operation modes, the boost mode, and the auto bypass mode. In the boost mode (V_{IN} – 0.3V < V_{OUT_Target}), the converter boosts output voltage to V_{OUT_Target}, and delivers power to loading by internal synchronous switches after the soft-start state. In the auto bypass mode (V_{IN} – 0.3V ≥ V_{OUT_Target}), input voltage will deliver to the output terminal loading directly. That can provide maximum current capacity with the RT4823. Detailed information is shown in the Boost Mode section.

Boost Mode (Auto PFM/PWM Control Method)

In order to save power and improve efficiency at low loads, the Boost converter operates in PFM (Pulse Frequency Modulation) as the inductor drops into DCM (Discontinuous Current Mode). The switching frequency is proportional to loading to reach output voltage regulation. When loading increases and inductor current is in continuous current mode, the Boost automatically enters PWM mode.

Copyright © 2022 Richtek Technology Corporation. All rights reserved. RICHTEK is a registered trademark of Richtek Technology Corporation.

Table 2. The RT4823 Start-Up Description

Mode	Description	Condition
LIN	Linear startup	V_{IN} - 200mV ≥ V_{OUT}
Soft-Start	Boost soft-start	0.99 x V_{OUT_Target} > V_{OUT} ≥ V_{IN} - 200mV
Boost	Boost mode	V_{OUT_Target} ≥ 0.99 x V_{OUT_Target}
If V_{IN} increases higher than V_{OUT}		
Auto Bypass	Auto bypass mode	V_{IN} ≥ V_{OUT} Control loop auto transfer between auto bypass mode and boost mode.

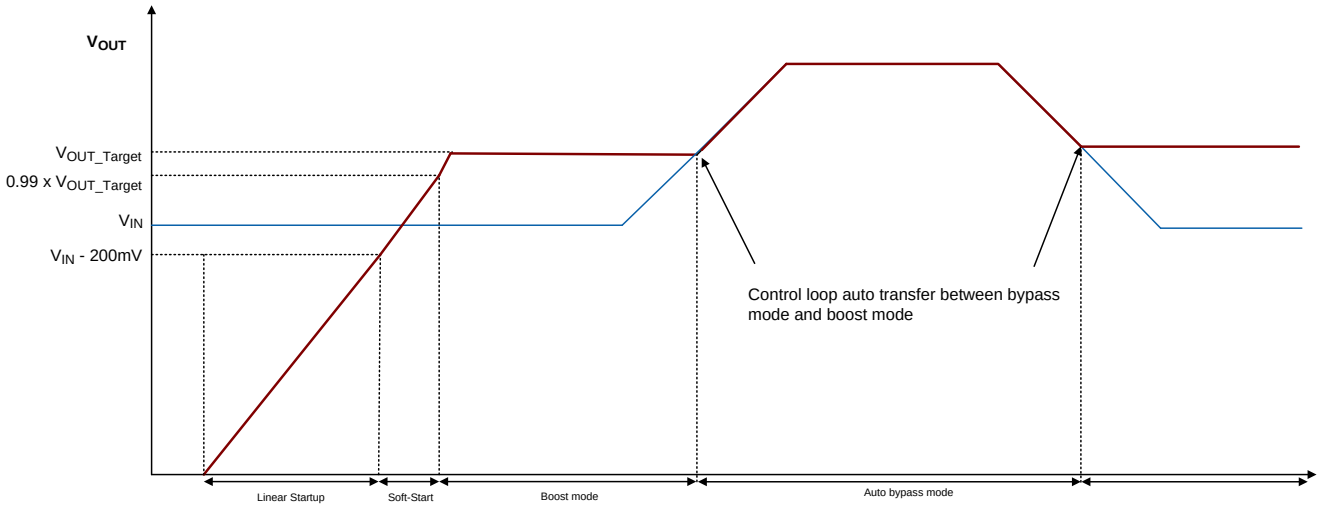


Figure 1. V_{OUT} Mode Transition Diagram with EN L to H and V_{IN} Variation (I_{OUT} = 0A)

Protection

The RT4823 features protections listed in the table below. It describes the protection behaviors.

Protection Type	Fault Event Trigger	Fault Deglitch Time	Protection Method	Fault Protection Latch Time	Reset Method
OCP_IL5A	I_{L_peak} > 5A	No delay	Turn off UG, LG	20ms, Auto-recovery	I_{L_peak} < 5A
OCP	I_{L_peak} > 3.6A	No delay	Stop LG switching	N/A	I_{L_valley} < 3.3A
OVP	V_{OUT} > 6V	100ns	Turn off UG, LG	N/A	V_{OUT} < 6V
SCP	V_{OUT} < 0.7V	No delay	Turn off UG, LG	20ms, Auto-recovery	V_{OUT} > 0.7V
OTP	TEMP > 150°C	170μs	Turn off UG, LG	Turn off UG, LG	TEMP < 130°C
SCP_SS	V_{IN} - V_{OUT} > 0.2V	2ms	UG OCP = 0.3A	N/A	V_{IN} - V_{OUT} < 0.2V
OCP_BYP	I_L > 0.3A	2ms	Turn off UG	20ms, Auto-recovery	I_L < 0.3A
SCP_BYP	V_{IN} - V_{OUT} > 0.7V	No delay	Turn off UG, LG	20ms, Auto-recovery	V_{IN} - V_{OUT} < 0.7V

Copyright © 2022 Richtek Technology Corporation. All rights reserved. RICHTEK is a registered trademark of Richtek Technology Corporation.

Absolute Maximum Ratings (Note 1)

- VIN, VOUT, SW, EN, BP ---------- –0.3V to 6.5V
- Power Dissipation, P_D @ T_A = 25°C
- WL-CSP-9B 1.3x1.2 (BSC) ---------- 1.54W
- Package Thermal Resistance (Note 2)
- WL-CSP-9B 1.3x1.2 (BSC) ---------- 64.9°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)

  HBM (Human Body Model) ---------- 2kV

Recommended Operating Conditions (Note 4)

- Input Voltage Range (Boost Mode) ---------- 1.8V to 5.5V
- Input Voltage Range (Bypass Mode) ---------- 2.2V to 5.5V
- Output Voltage Range ---------- 5V
- Input Capacitor, CIN ---------- 4.7µF
- Output Capacitor, COUT ---------- 3.5µF to 50µF
- Inductance, L ---------- 0.7µH to 2.2µH
- Input Current (Average current into SW) ---------- 1.8A
- Input Current (Peak current into SW) ---------- 4A
- Ambient Temperature Range ---------- –40°C to 85°C
- Junction Temperature Range ---------- –40°C to 125°C

Electrical Characteristics

(V_{IN} = 3.6V, C_{IN} = 4.7µF, C_{OUT} = 10µF, L1 = 1µH. All typical (TYP) limits apply for T_A = 25°C, unless otherwise specified. All minimum (MIN) and maximum (MAX) apply over the full operating ambient temperature range (–40°C ≤ T_A ≤ 85°C).

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Supply						
VIN Operation Range	V_{IN}		1.8	--	5.5	V
Into VIN Operating Quiescent Current	$I_{Q(non-switching)}$	I_{OUT} = 0mA, V_{IN} = 3.6V, EN = BP = GND	--	0.1	0.5	µA
Into VOUT Standby Mode Quiescent Current	$I_{Q(non-switching)}$	V_{OUT} = 5V BP = GND, EN = 5V	--	4	6	µA
VIN Quiescent Current (Device Normal Switching)	$I_{Q(switching)}$	V_{IN} = 3.6V, V_{OUT} = 5V, BP = EN = GND	--	--	1	µA
		V_{IN} = 3.6V, V_{OUT} = 5V, BP = GND, EN = VIN	--	6	--	
		V_{IN} = 3.6V, V_{OUT} = 5V, BP = VIN, EN = GND	--	16	25	
		V_{IN} = 3.6V, V_{OUT} = 5V, BP = EN = VIN	--	6	--	

Copyright © 2022 Richtek Technology Corporation. All rights reserved. RICHTEK is a registered trademark of Richtek Technology Corporation.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Power-On Reset	V_{POR}		1.2	1.5	--	V
Enable, FPWM						
Low-Level Input Voltage	V_{IL}		--	--	0.4	V
High-Level Input Voltage	V_{IH}		1.2	--	--	V
Input Leakage Current	I_{lkg}	Input connected to GND or VIN	--	--	0.5	μA
OUTPUT						
Regulated DC Output Voltage	V_{OUT}	1.8V ≤ V_{IN} ≤ 4.8V, I_{OUT} = 0mA, PFM operation	5.04	5.06	5.08	V
		V_{IN} = 3.6V, I_{OUT} = 1A, PWM operation	4.95	5	5.05	V
Output Ripple Performance	V_{OUT_Ripple}	V_{IN} = 3.6V, V_{OUT} = 5V, C_{OUT} = 10μF, I_{OUT} = 0A to 1A	--	60	120	mV
Power Switch						
High-Side MOSFET	r_{DS_H}		--	80	--	mΩ
Low-Side MOSFET	r_{DS_L}		--	80	--	mΩ
Minimum On-Time	t_{ON_MIN}	V_{IN} = 1.8V to 4.8V, V_{OUT} = 5V	20	--	60	ns
Maximum Duty Cycle	D_{MAX}	V_{IN} = 1.8V, V_{OUT} = 5V, I_L = 400mA	68.8	--	--	%
Switch Peak Current Limit (V_{IN} or V_{OUT} > 2.2V)	$I_{LIM(Peak)}$	V_{IN} = 3.6V, V_{OUT} = 5V	--	2450	--	mA
Switch Valley Current Limit (V_{IN} or V_{OUT} > 2.2V)	$I_{LIM(Valley)}$	V_{IN} = 3.6V, V_{OUT} = 5V	--	2150	--	mA
Pass-Through Current Limit	$I_{LIM(Pass)}$	V_{IN} = 3.6V	250	300	350	mA
Negative OCP	$I_{LIM(Neg)}$		–3000	–2000	–1000	mA
Oscilator						
Oscillator Frequency	f_{OSC}	V_{IN} = 3.6V	3	3.5	4	MHz
		V_{IN} < 2.5V → start to reduce frequency	2	--	--	
Soft-Start						
Start-Up Time	t_{START_BST}	V_{IN} = 3.6V, BP = GND, I_{OUT} = 0mA. Time from active EN to VOUT	100	400	500	μs
Pre-Charge Current Limit	$I_{LIM(Start)}$	V_{IN} = 3.6V, EN = 0 → 1.8V	250	300	350	mA
Protection						
Short-Circuit Protection	V_{SCP}		0.3	0.5	0.7	V
Over-Temperature Protection	T_{OTP}		140	150	160	°C
Over-Temperature Protection Hysteresis	T_{OTP_HYS}		--	20	--	°C
Over-Current Protection	$I_{LIM(5A)}$	V_{IN} = 5V	4	5	5.5	A
Over-Voltage Protection	V_{OVP}	V_{IN} = 3.6V	--	6	--	V

Copyright © 2022 Richtek Technology Corporation. All rights reserved. RICHTEK is a registered trademark of Richtek Technology Corporation.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Efficiency						
Efficiency	Eff	V_{OUT} = 5V, V_{IN} = 3.6V, Load = 10μA	--	72	--	%
		V_{OUT} = 5V, V_{IN} = 3.6V, Load = 10mA	--	90	--	
		V_{OUT} = 5V, V_{IN} = 3.6V, Load = 600mA	--	93	--	
		V_{OUT} = 5V, V_{IN} = 3.6V, Load = 1000mA	--	91	--	

Note 1. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. θ_{JC} is measured at the exposed pad of the package.

Note 3. Devices are ESD sensitive. Handling precautions are recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

Copyright © 2022 Richtek Technology Corporation. All rights reserved. RICHTEK is a registered trademark of Richtek Technology Corporation.

Typical Application Circuit

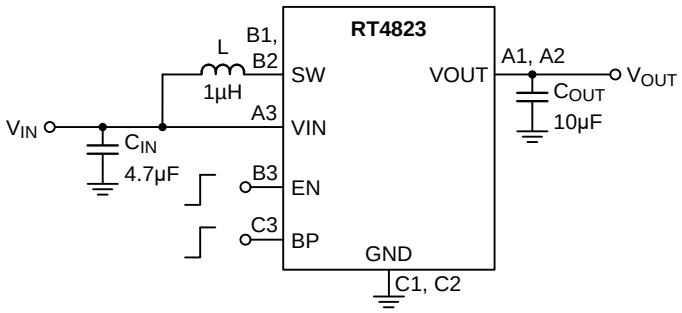


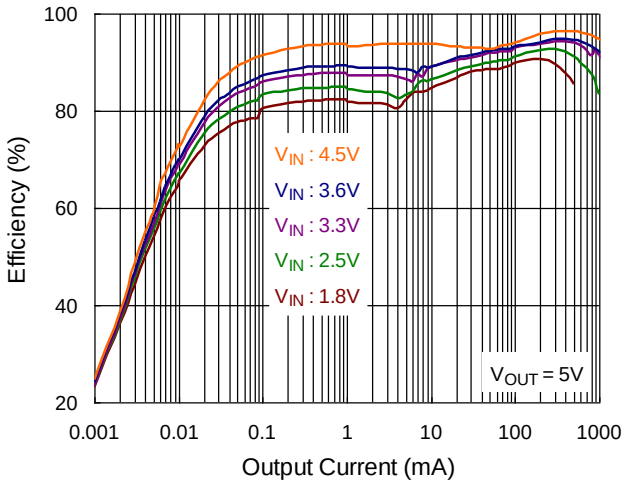
Table 3. Recommended Components Information

Reference	Part Number	Description	Package	Manufacturer
CIN	GRM155R60J475ME47D	4.7µF/6.3V/X5R	0402	Murata
COUT	GRM188R60J106ME47D	10µF/6.3V/X5R	0603	Murata
L	DFE252012F-1R0M=P2	1.0µH/3.3A	2.5x2.0x1.2mm	Murata

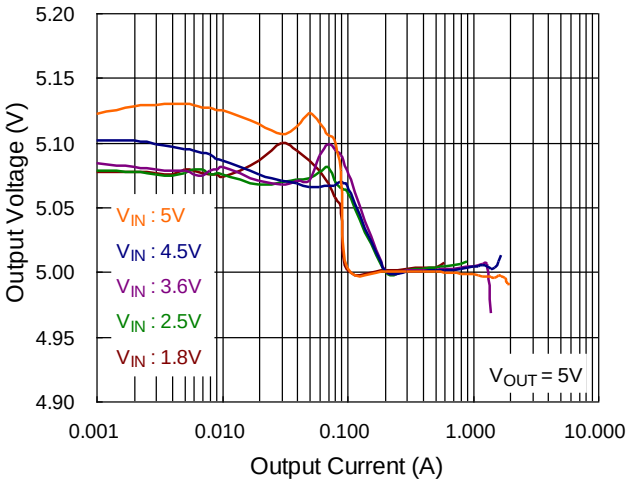
Copyright © 2022 Richtek Technology Corporation. All rights reserved. RICHTEK is a registered trademark of Richtek Technology Corporation.

Typical Operating Characteristics

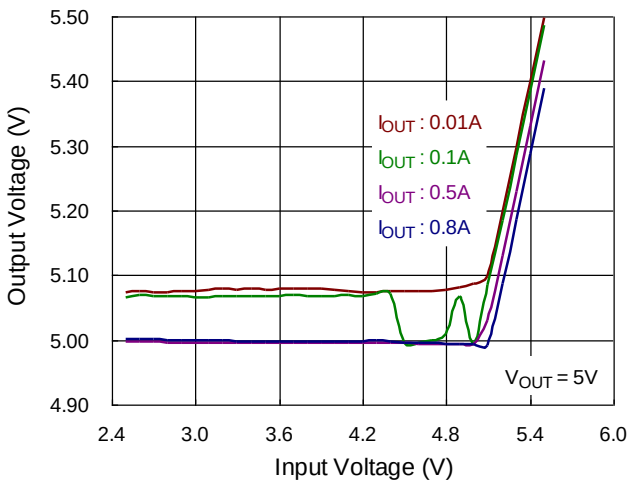
Efficiency vs. Output Current



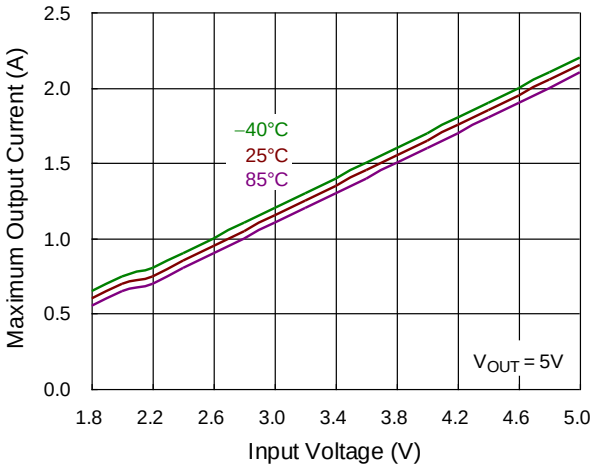
Boost Load Regulation



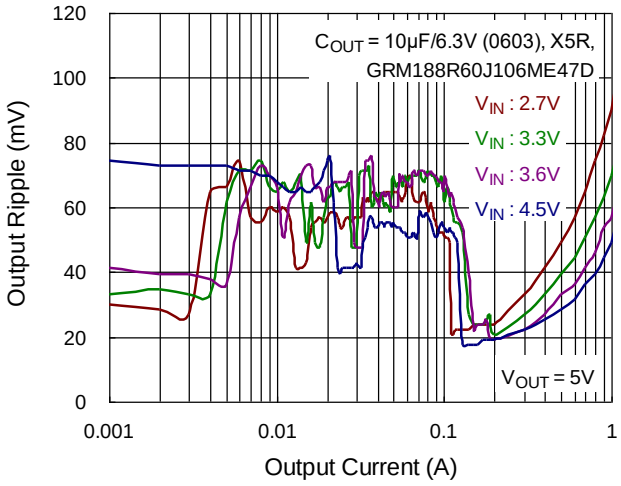
Boost Line Regulation



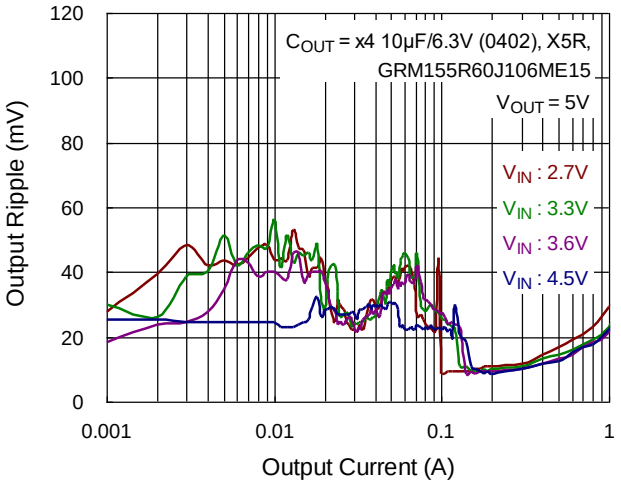
Maximum Output Current vs. Input Voltage



Output Ripple vs. Output Current

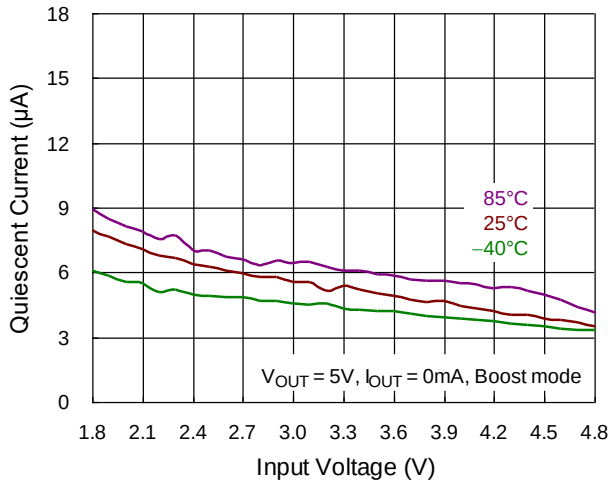


Output Ripple vs. Output Current

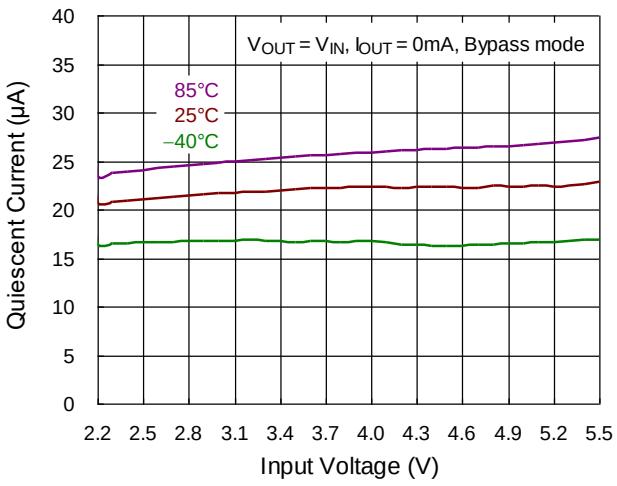


Copyright © 2022 Richtek Technology Corporation. All rights reserved. RICHTEK is a registered trademark of Richtek Technology Corporation.

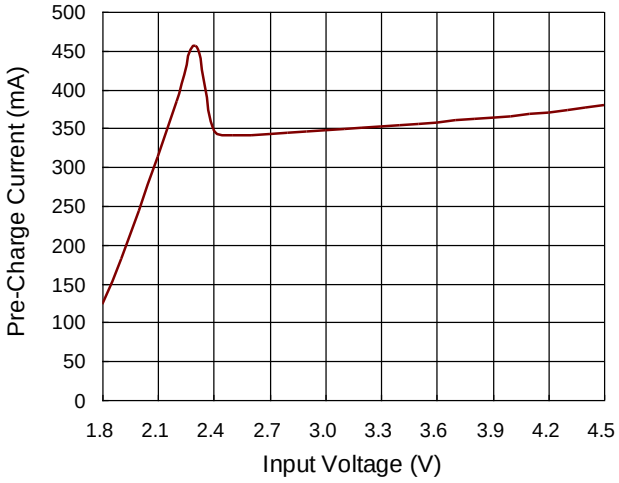
Quiescent Current vs. Input Voltage



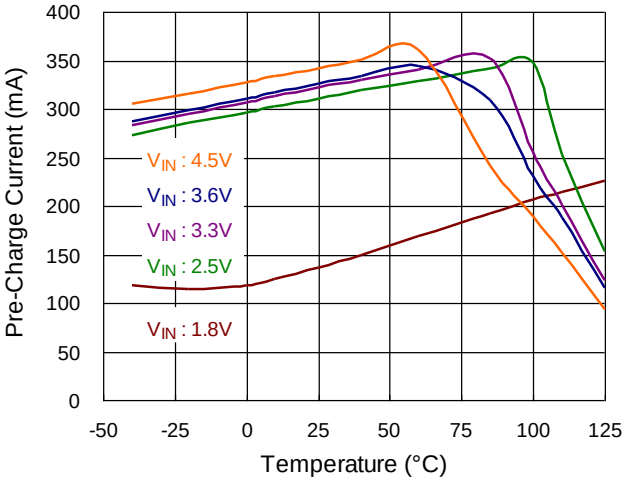
Quiescent Current vs. Input Voltage



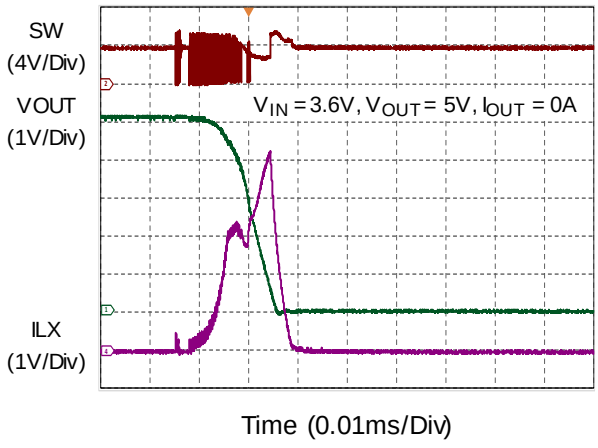
Pre-Charge Current vs. Input Voltage



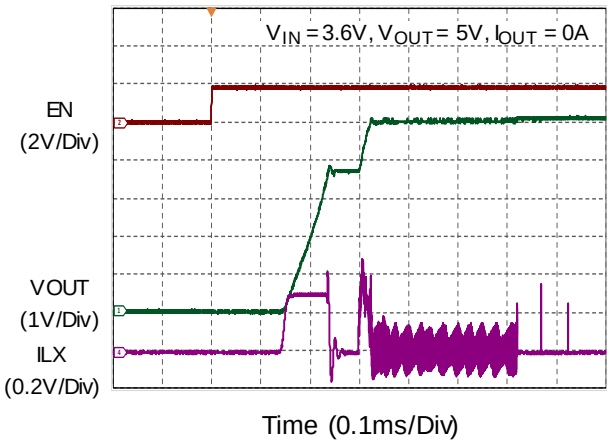
Pre-Charge Current vs. Temperature



Boost Short Circuit

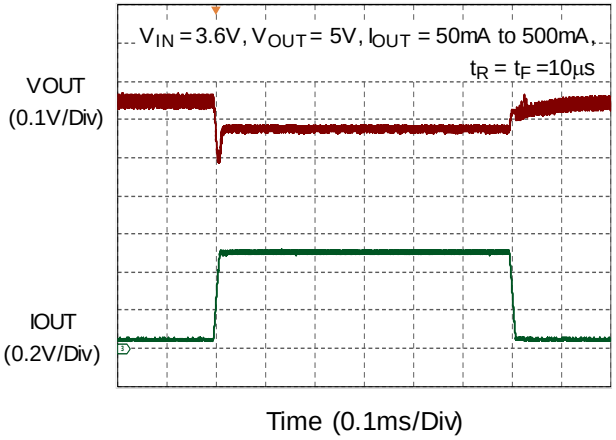


Power-On

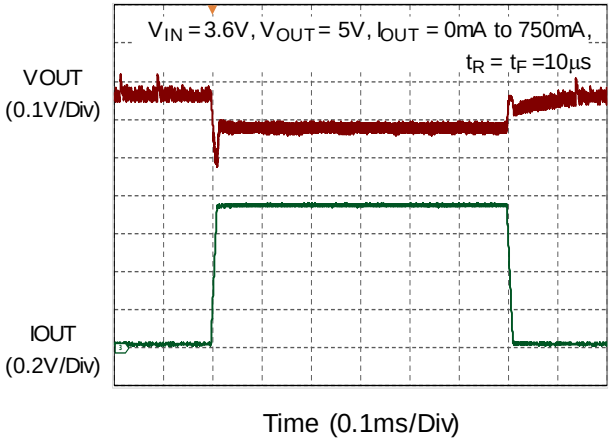


Copyright © 2022 Richtek Technology Corporation. All rights reserved. RICHTEK is a registered trademark of Richtek Technology Corporation.

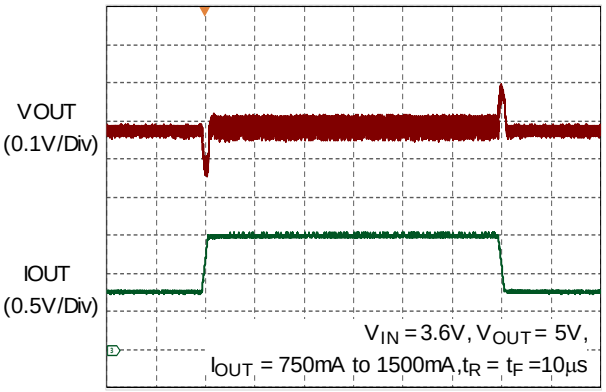
Load Transient



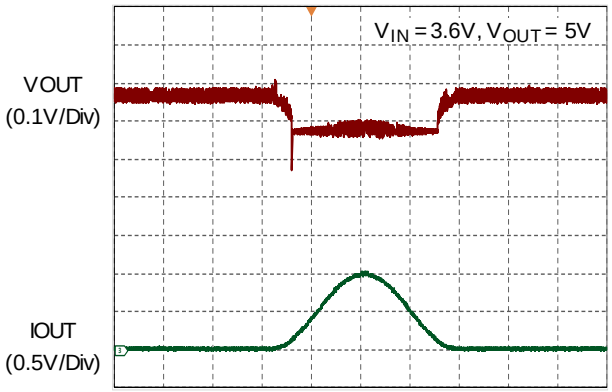
Load Transient



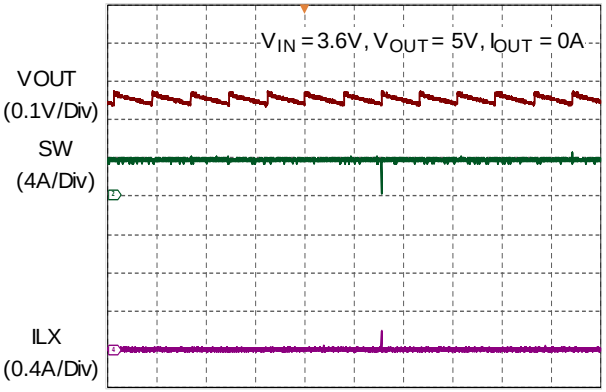
Load Transient



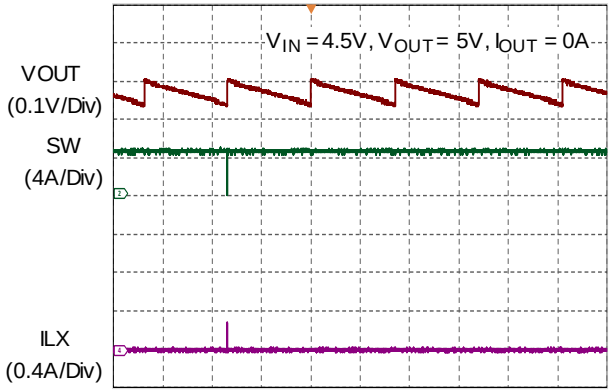
Sine Waveform Stability



PFM Output Ripple

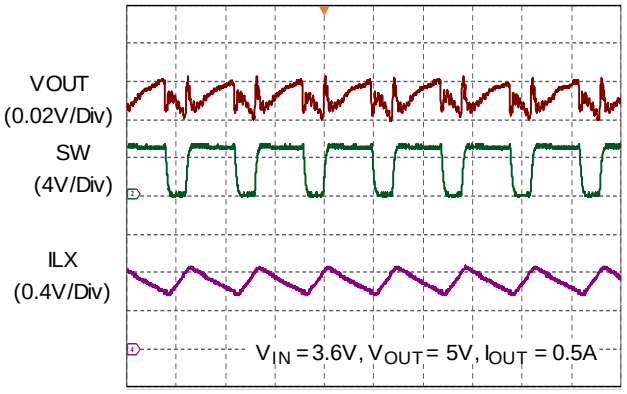


PFM Output Ripple



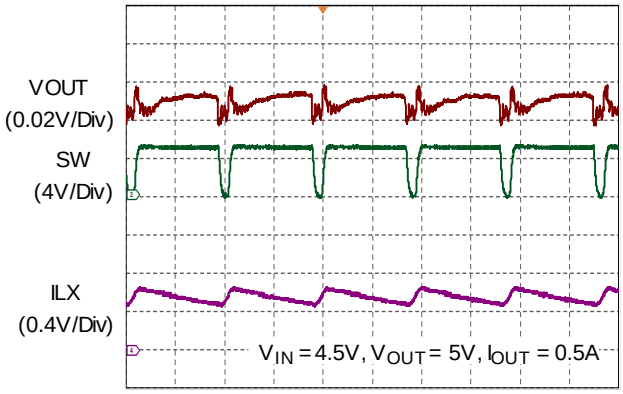
Copyright © 2022 Richtek Technology Corporation. All rights reserved. RICHTEK is a registered trademark of Richtek Technology Corporation.

PWM Output Ripple



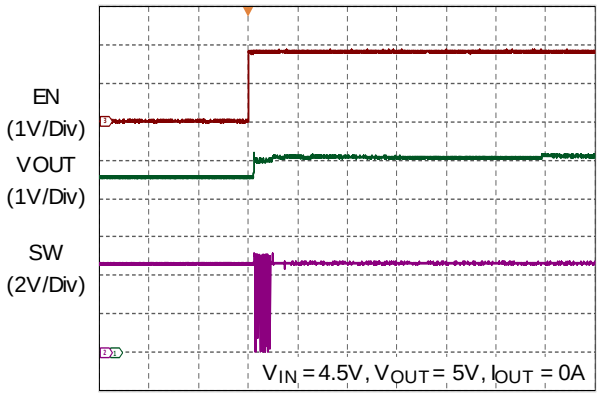
Time (0.0002ms/Div)

PWM Output Ripple



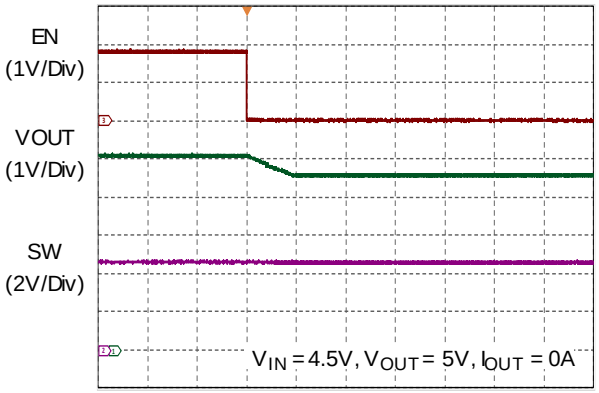
Time (0.0002ms/Div)

Bypass Mode into Boost Mode



Time (1ms/Div)

Boost Mode into Bypass Mode



Time (1ms/Div)

Copyright © 2022 Richtek Technology Corporation. All rights reserved. RICHTEK is a registered trademark of Richtek Technology Corporation.

Application Information

Enable

The device can be enabled or disabled by the EN pin. When the EN pin is higher than the threshold of logic-high, the device starts operating with soft-start. Once the EN pin is set at low, the device will be shut down. In shutdown mode, the converter stops switching, internal control circuitry is turned off, and the load is disconnected from the input. This also means that the output voltage can drop below the input voltage during shutdown.

Power Frequency Modulation (PFM)

PFM is used to improve efficiency at light load. When the output voltage is lower than a set threshold voltage, the converter will operate in PFM. It raises the output voltage with several pulses until the loop exits PFM.

Thermal Shutdown

The device has a built-in temperature sensor which monitors the internal junction temperature. If the temperature exceeds the threshold, the device stops operating. As soon as the IC temperature decreases below the threshold with a hysteresis, it starts operating again. The built-in hysteresis is designed to avoid unstable operation at IC temperatures near the over temperature threshold.

Inductor Selection

The primary concern of inductor selection is the maximum loading of the application. The example is given by the application condition and equations below.

Application condition:

V_{IN} = 3.6V, V_{OUT} = 5V, I_{OUT} = 1.3A, converter efficiency = 90.2%, Frequency = 3.5MHz, L = 1μH.

Step 1 : To calculate input current (I_{IN}).

$$I_{IN} = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times Eff} = 2.001A$$

Step 2 : To calculate duty cycle of boost converter.

$$D = 1 - \frac{V_{IN}}{V_{OUT}} = 0.28$$

Step 3 : To calculate peak current of inductor.

$$I_{L(Peak)} = I_{IN} + 0.5 \times \frac{V_{IN} \times D}{L \times Freq.} = 2.145A$$

The recommended nominal inductance value is 1μH. It is recommended to use inductor with dc saturation current ≥ 2200mA.

Input Capacitor Selection

At least an input capacitor of 4.7μF and the rate voltage of 6.3V for DC bias is recommended to improve transient behavior of the regulator and EMI behavior of the total power supply circuit for SW. And input capacitor placed as close as possible to the VIN and GND pins of the IC is recommended.

Output Capacitor Selection

At least a 10μF capacitors is recommended to improve V_{OUT} ripple.

Output voltage ripple is inversely proportional to C_{OUT}.

Output capacitor is selected according to output ripple which is calculated as :

$$V_{RIPPLE(P-P)} = t_{ON} \times \frac{I_{LOAD}}{C_{OUT}}$$

and

$$t_{ON} = t_{SW} \times D = t_{SW} \times \left(1 - \frac{V_{IN}}{V_{OUT}}\right)$$

therefore :

$$C_{OUT} = t_{SW} \times \left(1 - \frac{V_{IN}}{V_{OUT}}\right) \times \frac{I_{LOAD}}{V_{RIPPLE(P-P)}}$$

and

$$t_{SW} = \frac{1}{f_{SW}}$$

The maximum V_{RIPPLE} occurs at minimum input voltage and maximum output load.

Copyright © 2022 Richtek Technology Corporation. All rights reserved. RICHTEK is a registered trademark of Richtek Technology Corporation.

Boost Converter Sleeping Mode Operation

The PFM mode and PWM mode are implemented in the RT4823. PFM mode is designed for power saving operation when the system operates at light load.

There is a mode transition between PFM and PWM mode. When system loading is increasing, the operating mode transitions from PFM mode to PWM mode. Please note that, within this small loading current range, the mode changed causes output ripple to increase.

Current Limit

The RT4823 employs a valley-current limit detection scheme to sense inductor current during the off-time. When the loading current is increased such that the loading is above the valley current limit threshold, the off-time is increased until the current is decreased to valley-current threshold. Next on-time begins after current is decreased to valley-current threshold. On-time is decided by (V_{OUT} – V_{IN}) / V_{OUT} ratio. The output voltage decreases when further loading current increases. The current limit function is implemented by the scheme, refer to Figure 2.

OCP ($I_{LIM(5A)}$) Shutdown Protection

The RT4823 implements OCP shutdown protection. When the converter operates in boost mode, peak current limit and valley current limit function cannot protect the IC from short circuit or the huge loading. The RT4823 implements truth disconnection function. When peak current is > 5A (Typ.), the boost converter will turn off high-side MOSFET (UG) and low-side MOSFET (LG).

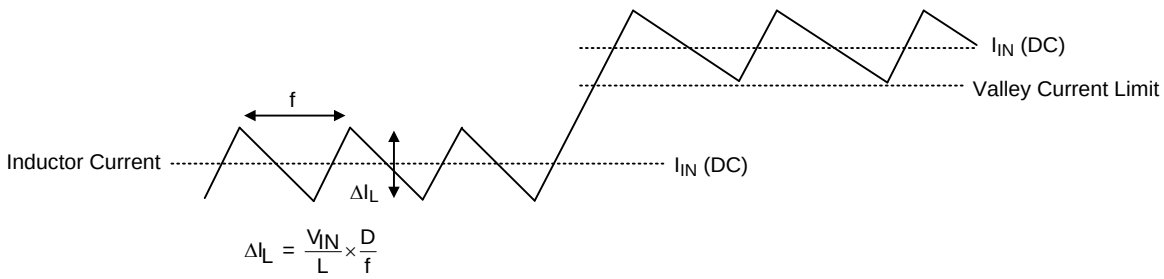


Figure 2. Inductor Currents in Current Limit Operation

Copyright © 2022 Richtek Technology Corporation. All rights reserved. RICHTEK is a registered trademark of Richtek Technology Corporation.

Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where TJ(MAX) is the maximum junction temperature, TA is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a WL-CSP-9B 1.3x1.2 (BSC) package, the thermal resistance, θ_{JA}, is 64.9°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below :

$P_{D(MAX)}$ = (125°C - 25°C) / (64.9°C/W) = 1.54W for a WL-CSP-9B 1.3x1.2 (BSC) package.

The maximum power dissipation depends on the operating ambient temperature for the fixed TJ(MAX) and the thermal resistance, θ_{JA}. The derating curves in Figure 3 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

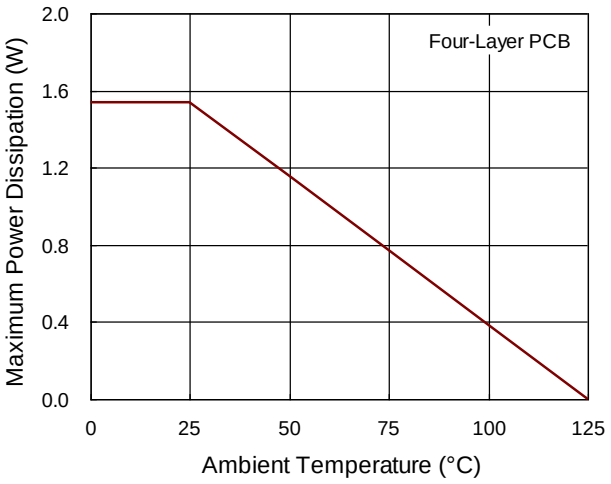


Figure 3. Derating Curve of Maximum Power Dissipation

Layout Considerations

The PCB layout is an important step to maintain the high performance of the RT4823.

Both the high current and the fast switching nodes demand full attention in the PCB layout to save the robustness of the RT4823. Improper layout might show the symptoms of poor line or load regulation, ground and output voltage shifts, stability issues, unsatisfying EMI behavior or worsened efficiency. For the best performance of the RT4823, the following PCB layout guidelines must be strictly followed.

- Place the input and output capacitors as close as possible to the input and output pins respectively for good filtering.
- For thermal consideration, it is needed to maximize the pure area for power stage area besides the SW.

Copyright © 2022 Richtek Technology Corporation. All rights reserved. RICHTEK is a registered trademark of Richtek Technology Corporation.

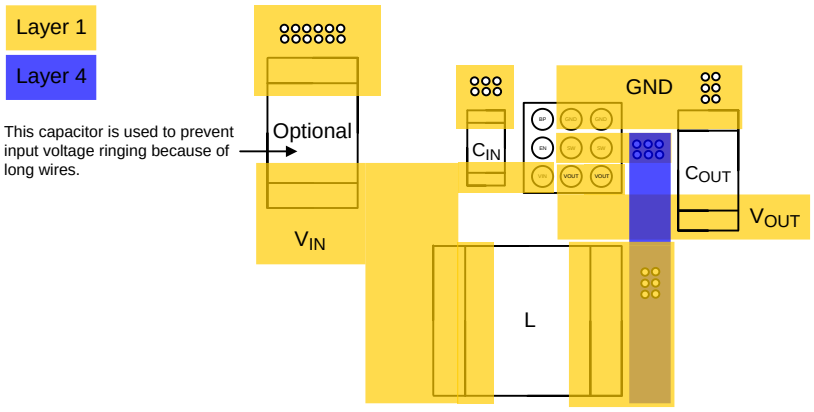
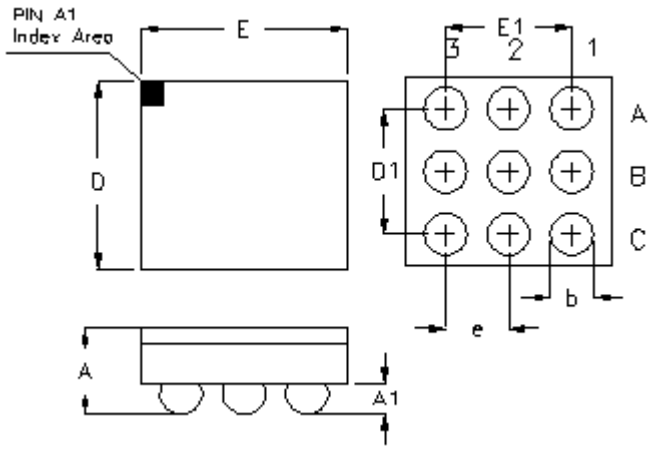


Figure 4. PCB Layout Guide

Copyright © 2022 Richtek Technology Corporation. All rights reserved. RICHTEK is a registered trademark of Richtek Technology Corporation.

Outline Dimension

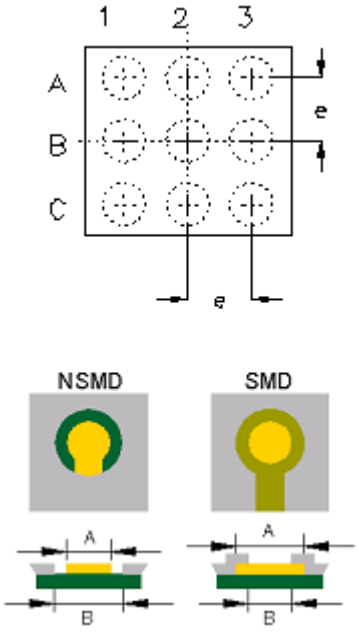


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.500	0.600	0.020	0.024
A1	0.170	0.230	0.007	0.009
b	0.240	0.300	0.009	0.012
D	1.160	1.240	0.046	0.049
D1	0.800		0.031	
E	1.260	1.340	0.050	0.053
E1	0.800		0.031	
e	0.400		0.016	

9B WL-CSP 1.3x1.2 Package (BSC)

Copyright © 2022 Richtek Technology Corporation. All rights reserved. RICHTEK is a registered trademark of Richtek Technology Corporation.

Footprint Information



Package	Number of Pin	Type	Footprint Dimension (mm)			Tolerance
			e	A	B	
WL-CSP1.3x1.2-9(BSC)	9	NSMD	0.400	0.240	0.340	±0.025
		SMD		0.270	0.240	

Richtek Technology Corporation
14F, No. 8, Tai Yuen 1st Street, Chupei City
Hsinchu, Taiwan, R.O.C.
Tel: (8863)5526789

RICHTEK
Richtek products are sold by description only. Richtek reserves the right to change the circuitry and/or specifications without notice at any time. Customers should obtain the latest relevant information and data sheets before placing orders and should verify that such information is current and complete. Richtek cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Richtek product. Information furnished by Richtek is believed to be accurate and reliable. However, no responsibility is assumed by Richtek or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Richtek or its subsidiaries.

Copyright © 2022 Richtek Technology Corporation. All rights reserved. RICHTEK is a registered trademark of Richtek Technology Corporation.

Datasheet Revision History

Version	Date	Description	Item
00	2022/8/3	Final	Application Information on P15
01	2022/9/19	Modify	Electrical Characteristics on P6 Typical Operating Characteristics on P11

Copyright © 2022 Richtek Technology Corporation. All rights reserved. RICHTEK is a registered trademark of Richtek Technology Corporation.